Single switch Z-source/quasi Z-source DC-DC converters

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ABSTRACT

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Keywords:

DC-DC power conversion Photovoltaic Voltage boosting ability Voltage gain Z-source converter This paper analyzes a family of high step up single switch switched capacitor boost converters and Z-source/quasi Z-source dc-dc converters to provide high output dc voltage gain with single stage conversion having low voltage stress on active switches, capacitors, and diodes. The operating principles, parameters design guideline of these converters are presented along with simulation results. The discussed topologies in this paper are aimed to increase the conversion system reliability and efficiency with decreased cost, volume, and weight. These power converter topologies are used for various applications such as photovoltaic (PV) systems, wind energy conversion, fuel cells, uninterruptible power systems, motor drives, energy storage systems, electric vehicle and power factor correction. Simulations are carried out in MATLAB/Simulink environment.

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1. INTRODUCTION

Photovoltaic (PV) applications, low voltage DC grid systems, fuel cell systems, grid connected inverters, electric vehicles, motor drives and electronic loads requires a desired DC link voltage either at the point of coupling or at the subsequent power converter arrangements, which should have constant or regulated DC voltage. However in reality, output DC voltages derived out from these DC sources such as PV systems are not uniform due to various reasons like source variability, intermittency and absence of appropriate power converter topologies. To avoid these issues, various DC power converter topologies are developed by various authors having the features of regulated voltage with adequate voltage gain are illustrated as mentioned in [1-7]. They had realized these necessities with the help of isolated/non-isolated, conventional boost/buck-boost, resonant converter topologies having high step up DC gains, when operated at certain duty ratio. However it produces a large current ripple in the inductor leading to higher conduction and switching loss. DC-DC converters having high step up voltage gain experiences variety of problems like voltage stress, power losses due to interfacing transformers. Switching losses in the diode and voltage unbalance on the output capacitors affect the performance of these converters with low efficiency in the form of reverse recovery/electromagnetic interference problems [8-17]. In this paper, switched capacitor ZSI and QZSI converter family based topologies are deliberated for the application of DC-DC conversion. The comparative key factors influencing the use of the proposed topologies are: continuous input current and voltage gain, connection of source and load at the common ground point, voltage stress across the capacitor and quantity of diode and switching devices. By employing a single active switch (MOSFET or IGBT), these converters can realize better DC-DC voltage conversion at duty cycle of value ranging from 0.1 to 0.9. Also the buck and boost features of this converters subjected to duty ratio.

2. BASIC SWITCHED CAPACITOR BOOST CONVERTER TOPOLOGIES

A third order boost DC-DC converter is presented in Figure 1, which contains of single switch S_W , diodes (D₁ and D₂), capacitors (C₁ and C₂), an inductor L and resistive load R_L. Following equations associated with boost converter are briefed in [18].

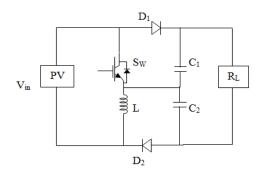


Figure 1. Third order boost DC-DC converter

The boost conversion factor, M is given by:

$$M = \frac{2-D}{1-D} \tag{1}$$

Voltage stress on active switch, V_s is given by:

$$Vs = \frac{Vin}{1 - D}$$
(2)

Voltage stress across diodes, V_d is given by:

$$V_d = \frac{V_{in}}{1 - D} \tag{3}$$

Figures 2 and 3 are examples of switched capacitor boost converter topologies. To obtain a better voltage gain, switched capacitors (C_1 and C_2) are connected in series to supply the load. When the switch S_W is turned on, input voltage source is connected to C_1 in series and load is connected to C_2 load. Following equations associated with switched capacitor DC-DC converter are briefed [19, 20]. The boost conversion factor, M is given by:

$$M = \frac{2}{1 - D} \tag{4}$$

Voltage stress on active switch, V_s and voltage stress across diodes, V_d is given by:

$$Vs = Vd = \frac{Vout}{2}$$
(5)

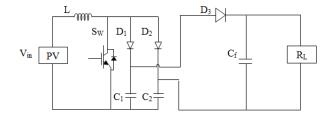


Figure 2. Switched capacitor DC-DC converter (topology 1) [16]

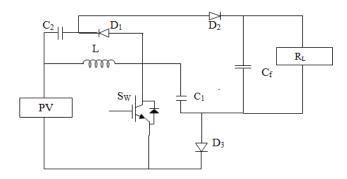


Figure 3. Switched capacitor DC-DC converter (topology 2)

3. Z-SOURCE DC-DC CONVERTER TOPOLOGIES

According to Figure 4, the Z-source converter is operating as a DC-DC boost operation, which consists of diode D₁, two identical inductors (L₁ and L₂) and (C₁ and C₂) are coupled to attain the Z-source operation. Switch (S_W) is active switch and L_f and C_f are second order low pass filters. The converter supplies power to the resistive load (R_L). By the symmetry of Z network, inductor L₁ and L₂ ranges are selected equal to L; capacitor C₁ and C₂ ranges are selected equal to C, therefore $i_{L1} = i_{L2} = i_{L}$, $V_{L1} = V_{L2} = V_{L}$ and $V_{C1} = V_{C2} = V_{C}$. The circuit has a higher input to output DC voltage boost conversion factor and isolates the source and load in case of a short circuit at the load side. MOSFET is switched at a switching frequency of $f_s = 1/T_s$ and duty cycle of the switch D is given by D = Ton/Ts, where Ton is pulse width and Ts is the switching period of PWM (pulse width modulation) signal. Following equations associated with Z-source DC-DC converter are briefed [21, 22].

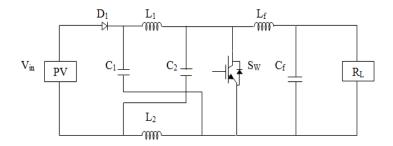


Figure 4. Z-source DC-DC converter (topology 1)

The boost conversion factor, M is given by:

$$M = \frac{1 - D}{1 - 2D} \qquad \text{for } D < 0.5 \tag{6}$$

Voltage stress on active switch, V_s is given by:

$$Vs = \frac{Vin}{1 - 2D} \tag{7}$$

Voltage stress across diodes, Vd is given by:

$$Vd = \frac{Vin}{1 - 2D} \tag{8}$$

Voltage stress across diodes, V_d is given by:

$$Vc = \frac{1 - D}{1 - 2D} Vin \tag{9}$$

The modified version of Z source DC-DC converter as shown in Figure 5 consists of Z-source network (L_1 , L_2 , C_1 , and C_2), a switch S_W , two diodes D_1 and D_2 , a filter capacitor C_f and a load resistance R_L [23]. Both from Figures 5 and 6, the input source and load are located on the same side of the Z-source network, which share the same ground to produce high voltage gain with no additional components and low voltage stresses on the switch and diodes [24]. The other modified versions of Z-source DC-DC converter are shown in Figure 7 with additional diodes and capacitors. The Z-source network is consist of "D₁, L₁, L₂, C₁, C₂" and the switched capacitor network is consist of C₃, C₄, C₅, D₂, D₃, and D₄.

The boost conversion factor, M is given by:

$$M = \frac{2(1-D)}{1-2D} \qquad \text{for } D < 0.5 \tag{10}$$

Voltage stress on capacitors, Vc of C_1 , C_2 can be expressed as:

$$Vc = \frac{1-D}{1-2D} Vin \tag{11}$$

Output voltage V_{out} is given by:

$$Vout = \frac{2(1-D)}{1-2D} Vin \tag{12}$$

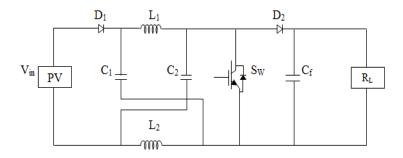


Figure 5. Z-source DC-DC converter (topology 2)

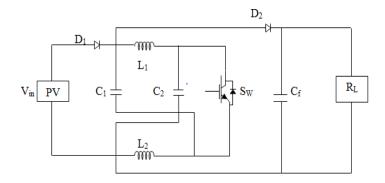


Figure 6. Z-source DC-DC converter (topology 3)

Single switch Z-source/quasi Z-source DC-DC converters (V. Saravanan)

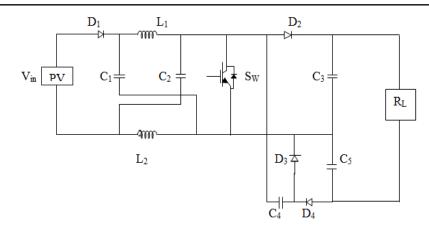


Figure 7. Z-source DC-DC converter (topology 4)

4. QUASI Z-SOURCE DC-DC CONVERTER TOPOLOGIES

The quasi Z-source converter is an exclusive Z-source network. It is connected between the input power source and switching circuit for the purpose of increase the DC output voltage of the converter by adjusting the shoot through (ST) duty ratio as illustrated in Figure 8 [25]. During the traditional operation state, only DC current goes through the inductors. During shoot through (ST) mode and non-shoot through mode, inductor current increases and decreases respectively. The other modified versions of quasi Z-source DC-DC converter topologies are exposed in Figures 9 and 10.

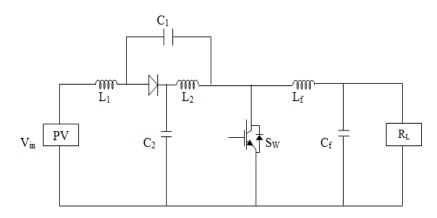


Figure 8. Quasi Z-source DC-DC converter (topology 1)

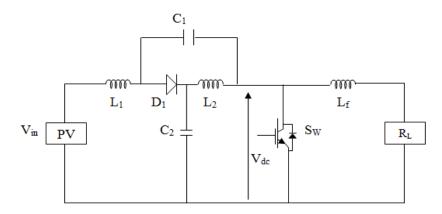


Figure 9. Quasi Z-source DC-DC converter (topology 2)

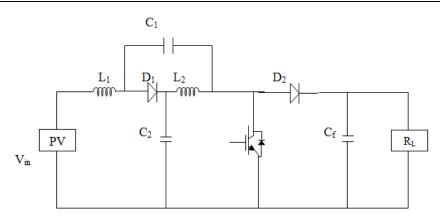


Figure 10. Quasi Z-source DC-DC converter (topology 3)

By the symmetry of Z network, inductor L1 and L2 ranges are selected equal to L; capacitor C1 and C2 ranges are selected equal to C. Then the value of i_{L1} and i_{L2} are equal to i_{L} , V_{L1} and V_{L2} are equal to V_L , V_{C1} and V_{C2} are equal to V_C . The system state equation is given by:

$$IL1 = IL2 = \frac{(1-D)^2}{(1-2D)^2 RL} Vin$$

$$VC1 = \frac{D}{(1-2D)} Vin$$

$$VC2 = \frac{1-D}{(1-2D)} Vin$$

$$IL = \frac{(1-D)}{(1-2D) RL} Vin$$

$$Vdc = \frac{1}{(1-2D)} Vin$$
(13)

Inductor current (IL) is

$$IL = \frac{P}{Vin}$$
(14)

when the converter is operating at shoot through state mode, the maximum current ripple occurs due to the nature of the inductor. The range of current ripple (δ) is calculated according to (15):

$$\Delta IL = 2 \,\delta\% \,IL \tag{15}$$

The value of the inductor is calculated according to (16):

$$L = \frac{VLDTS}{\Delta IL}$$
(16)

where D and Ts are the duty cycle at shoot through state and total switching time duration respectively.

In shoot through state operation mode, the ripple current of the converter is reduces because the inductor current (I_L) and capacitor current (IC) become equal. The voltage ripple of the converter is depends on Vc δ V%, the range of the capacitor is calculated according to (17). Quasi Z-source DC-DC converter topologies with switched capacitor network are shown in Figure 11 and Figure 12. The quasi Z-source network is included " L_1 , D_1 , L_2 , C_1 and C_2 " and the switched capacitor network is included C₃, D_4 , C_4 , D_5 , C_5 and D_3 [26, 27]. Some of the very interesting Z-source DC-DC converter topologies of different configurations, better features with scaled down verifications are also presented in [28-30].

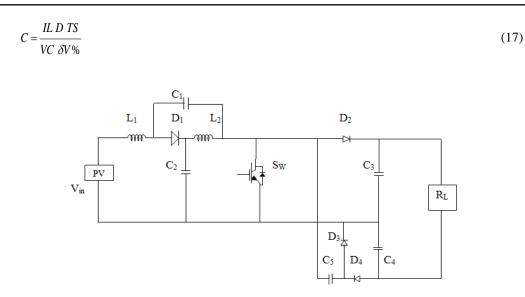


Figure 11. Quasi Z-source DC-DC converter (topology 4)

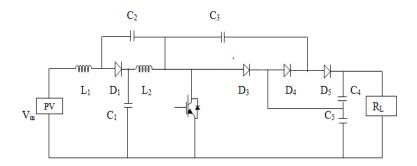


Figure.12. Quasi Z-source DC-DC converter (topology 5)

The boost conversion factor, M is given by:

$$M = \frac{2}{1 - 2D} \qquad \text{for } D < 0.5 \tag{18}$$

Voltage stress on capacitors, Vc of C_1 to C_5 can be expressed as:

$$Vc1 = \frac{1-D}{2} Vout$$

$$Vc2 = \frac{D}{2} Vout$$

$$Vc3 = Vc4 = Vc5 = \frac{Vout}{2}$$
(19)

The inductor value of the Z-source network is calculated by using (20), ΔI_L is a maximum value of the current ripple.

$$L1 = L2 = \frac{D(1-D)Vin}{(1-2D)\,\Delta IL\,f}$$
(20)

The capacitor value of the Z-source network is calculated by using (21), ΔI_C is a maximum value of the voltage ripple.

(21)

$$C1 = \frac{2 D Iout}{(1-2D) \Delta VC f}$$

$$C2 = \frac{2 D^2 Iout}{(1-2D) \Delta VC f}$$

$$C3 = \frac{2 Iout}{\Delta VC f}$$

$$C4 = \frac{4DIout}{(1-2D)^2 \Delta VC f}$$

$$C5 = \frac{(1+D) Iout}{\Delta VC f}$$

5. RESULTS AND DISCUSSION

The analysis of these discussed converter topologies are based on the following assumptions. 1) Diode and switching devices are operating at ideal conditions, 2) The resistor, capacitor and inductor are assumed as frequency dependent, time invariant linear elements. 3) The value of the capacitor is assumed large with constant voltage in one switching time duration. 4) The converters operating in continuous conduction mode.

The chosen simulation values for all the discussed topologies are: $V_{in} = 12$ V, source side inductors L_1 and L_2 values are 330 µH and capacitors C_1 and C_2 values are 470 µF, filter values L_f and C_f values are 330 µH and 470 µF respectively, $f_s = 40$ kHz, duty cycle = 0.1 to 0.99 for switched capacitor DC-DC converter topologies and duty cycle = 0.1 to 0.6 for Z-source/quasi Z-source DC-DC converter topologies. Resistive load R_L of value 50 Ω is chosen for all these converter topologies. Simulations are carried for these topologies for the corresponding duty ratio for the selected range in steps of 0.05 and the obtained output DC voltages are noted. The maximum output DC voltage for the corresponding duty ratio is presented in the following tables and the values for these ranges are shown in respective figures.

It can be observed that switched capacitor converter topologies exhibit very higher voltage gain for the duty ratio above 0.9 and Z-source/quasi Z-source topologies does the same at a duty ratio value ranging from 0.44 to 0.48. Table 1 gives the performance of switched capacitor DC-DC converter topologies, where the maximum output DC voltage obtained is tabulated with its corresponding duty ratio and Figure 13 plots the output DC voltage of these converter topologies as a role of D.

Table 1. Performance of switched capacitor DC-DC converter topologies				
Switched capacitor DC-DC converter topologies	Maximum output DC voltage(Volts)	Corresponding duty ratio		
Third order boost DC-DC converter	135.4	0.95		
Switched capacitor DC-DC converter (topology 1)	132.1	0.92		
Switched capacitor DC-DC converter (topology 2)	213.2	0.93		

250 v 0 200 0 l u t 150 t a Third order boost DC-DC p g converter 100 u e Switched capacitor de – de v converter (Topology 1) 50 0 Switched capacitor dc-dc D 1 converter (Topology 2) С 0 0.9 0.92 0.96 0.98 0.98 0.5 0.6 0.8 0.100.3 0.0 8 Duty ratio, D



Table 2 gives the performance of Z-source DC-DC converter topologies, where the maximum output DC voltage obtained is tabulated with its corresponding duty ratio and Figure 14 plots the output DC voltage of these Z-source DC-DC converter topologies as a role of D. Table 3 gives the performance of quasi Zsource DC-DC converter topologies, where the maximum output DC voltage obtained is tabulated with its corresponding duty ratio and Figure 15 plots the output DC voltage of these quasi Z-source DC-DC converter topologies as a function of D. It is observed that output DC voltage of switched capacitor DC-DC converter topologies are high at higher duty ratio, whereas Z-source/quasi Z-source DC-DC converter topologies exhibit better DC voltage boosting at a value of 0.4 which results in minimum stress to the switch.

Table 2. Performance of Z-source DC-DC converter topologies				
Z source DC-DC converter topologies Maximum output DC voltage (Volts) Corresponding duty of				
Topology 1	87.39	0.48		
Topology 2	88.23	0.47		
Topology 3	87.56	0.47		
Topology 4	85.56	0.44		

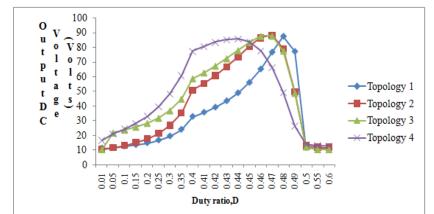
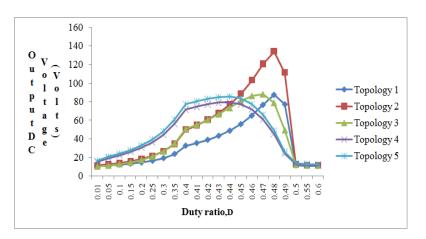
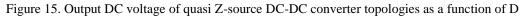


Figure 14.	Output DC volta	age of Z-source	e DC-DC converter t	topologies as a	function of D

Table 3. Performance of quasi Z-source DC-DC converter topologies				
Quasi Z source DC-DC converter topologies	Maximum output DC voltage (Volts)	Corresponding duty ratio		
Topology 1	87.39	0.48		
Topology 2	134.3	0.48		
Topology 3	88.23	0.47		
Topology 4	79.27	0.44		
Topology 5	85.56	0.44		





6. CONCLUSION

A family of switched capacitor and Z-source/quasi Z-source DC-DC converter topologies for photovoltaic power applications has been worked in this paper. Steady state analysis of these topologies has been discussed with detailed simulation results to verify its effectiveness. Output DC voltage obtained for all the converter topologies is presented in a comprehensive manner to meet the requirement of various applications. The converters discussed in this paper have the advantages such as continuous input current, reduced capacitor voltage stress, low voltage stress across the output diode and power switches. Also, these converters are suitable for photovoltaic applications where a varying low DC input voltage is converted to a high stabilized DC output voltage.

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