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Multicarrier SPWM Control Techniques for Three Phase Eleven Level Diode Clamped Multilevel Inverter and Hybrid Inverter with Reduced Number of Components

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ABSTRACT

A comparative analysis of three phase eleven level Diode Clamped Multilevel Inverter (DCMLI) and hybrid inverter is performed in this paper in which the later requires fewer carrier signals, less number of devices and gate drive circuits. The performance is evaluated using Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD) and Carrier Overlapping (CO) Sinusoidal Pulse Width Modulation (SPWM) methods. The hybrid multilevel inverter has superior features over diode clamped multilevel inverters and is more efficient since the positive levels of the inverter that are generated by high frequency switches (level generation part), are reversed by low frequency switches (polarity generation part) when the voltage polarity is required to be changed for negative polarity. Therefore, the overall cost and complexity of the hybrid inverter are greatly reduced particularly for higher inverter output voltage levels. Simulation is performed for three phase eleven level diode clamped multilevel inverter and hybrid multilevel inverter using MATLAB/Simulink for induction motor load and the total harmonic distortion is evaluated at different load torques.

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1. INTRODUCTION

The multilevel inverters have drawn tremendous interest in high power high voltage applications due to their merits such as reduced voltage stress on devices, lower switching losses, lower EMI problems and less THD. The neutral point clamped inverter was proposed by Nabae [1]. The basic concept of multilevel inverter is to synthesize a staircase voltage waveform from several lower voltage DC sources which approaches the sinusoidal wave with reduced harmonic distortion [2]. In multilevel inverters, the semiconductors are wired to form series type connection so that the operation at higher voltages is possible. The switching losses and the switching frequency can be reduced by staggering the switching because the switches are not truly series connected. Conventional multilevel inverters include diode clamped inverter, flying capacitor inverter and cascaded H-bridge inverter [3], [4]. The major drawback of multilevel inverters is the higher number of power semiconductor switches required that complicates the overall system [5-9]. A multilevel inverter implemented with hybrid topology has many advantages as the levels increase when compared to conventional multilevel inverters. The hybrid multilevel inverter eliminates the diodes and capacitors that are used in DCMLI, capacitors used in flying capacitor inverters and also reduces the semiconductor switches and carrier signals required than in cascaded inverters, diode clamped, and flying capacitors inverters. An approach of utilizing high-power devices with low-switching-frequency reduces voltage distortion of output but has got current harmonics which is a major drawback. There are

asymmetrical methods of using different values of voltage source which requires more number of power switches and diodes with different rating. Some topologies suffer from the capacitor balancing problems [10-14]. Whereas in case of hybrid multilevel inverter, the voltage sources used have equal values and has many advantages compared with conventional methods. It uses less number of switches and carrier waves and also operates the switching devices at line frequency which results in more efficiency [15-17]. In this paper PD, APOD and CO SPWM methods are utilized to drive the three phase diode clamped multilevel inverter and hybrid multilevel inverter.

2. ELEVEN LEVEL DIODE CLAMPED MULTILEVEL INVERTER

The three phase eleven level diode clamped multilevel inverter is implemented using carrier based sinusoidal pulse width modulation techniques for eleven level to verify the performance of the inverter. In an eleven level diode clamped multilevel inverter the switches are arranged into ten pairs. When one switch of the pair is turned ON, the other switch of the same pair must be OFF. Each switch pair works in complimentary mode and the diodes are used to provide access to mid-point voltage. At any point of time ten switches are triggered to achieve desired voltage level. The DC bus voltage is split into eleven voltage levels by using ten series connection of DC capacitors. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/10$ and voltage stress on each device is limited to $V_{dc}/10$ through clamping diodes. The middle point of the ten capacitors 'N' can be defined as the neutral point. Carrier waveforms for three phase eleven level diode clamped multilevel inverter are presented in Figure 1 to Figure 3 for PD, APOD and CO SPWM methods.

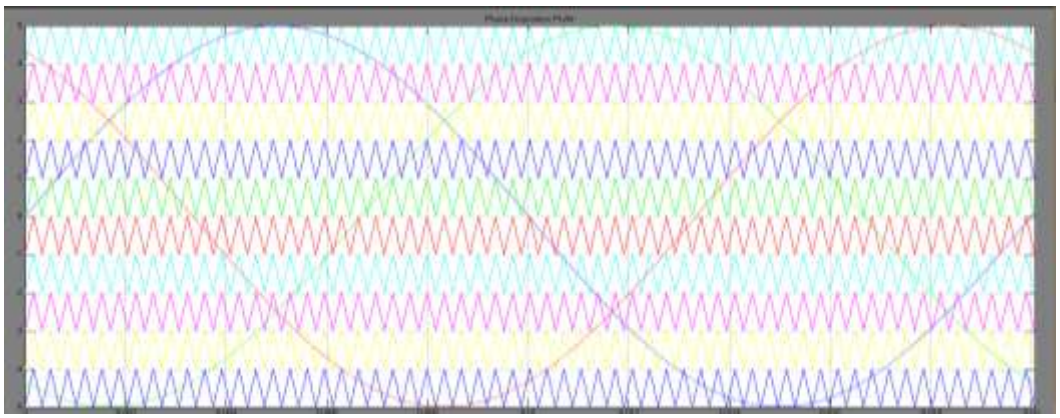

Figure 1. PD method for three phase eleven leven diode clamped multilevel inverter

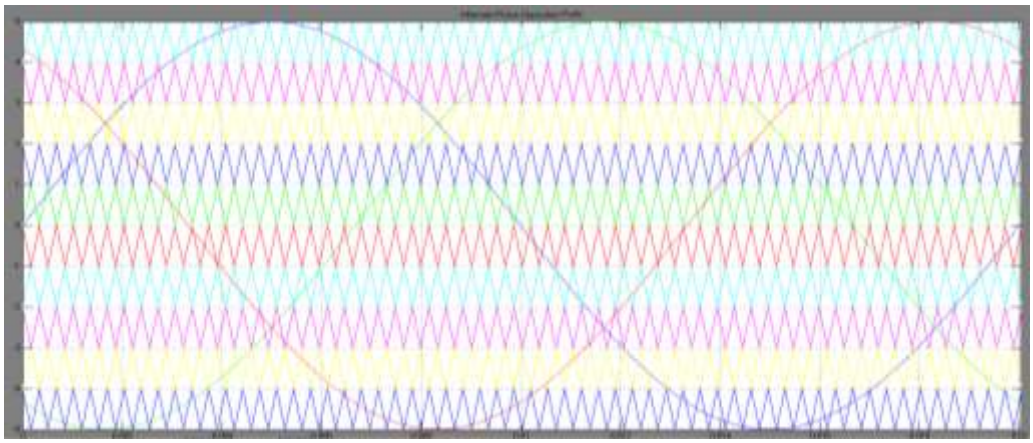

Figure 2. APOD method for three phase eleven leven diode clamped multilevel inverter

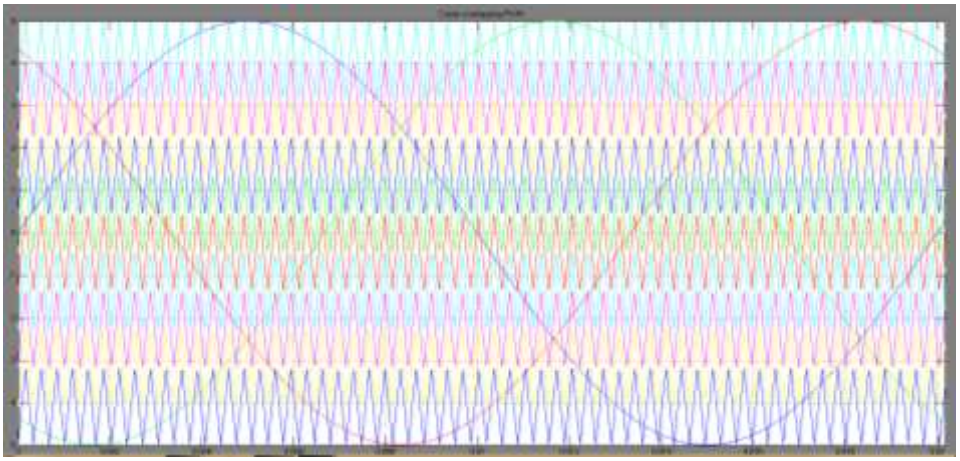

Figure 3. CO method for three phase eleven leven diode clamped multilevel inverter

Ten saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required for diode clamped multilevel inverter in order to produce eleven levels by sinusoidal pulse width modulation technique. Higher number of clamping diodes are required as the number of level increases in case of diode clamped multilevel inverters. Also, the capacitor voltage unbalance complicates the control of the system. The diode clamped multilevel inverters needs large number of power semiconductor switches and associated gate drive circuits. In order to mitigate the aforementioned drawbacks, hybrid multilevel inverter is implemented.

3. ELEVEN LEVEL HYBRID MULTILEVEL INVERTER

The output voltage of hybrid multilevel inverter is separated into level generation part that utilizes high frequency switches to produce required levels in positive polarity and polarity generation part which requires low frequency switches that are responsible to generate polarity of output voltage. The level generation part and polarity generation part together helps in producing required multilevel output voltage. Whereas, in diode clamped multilevel inverters, many of the power semiconductor switches are involved for generating the levels in the output voltage in positive and negative polarities. Compared to the diode clamped multilevel inverters where all the switches are responsible for generation of bipolar levels, hybrid multilevel inverter eliminates more number of power semiconductor switches.

The sinusoidal pulse width modulation method for eleven level diode clamped multilevel inverter requires ten carriers, but five carriers are sufficient in hybrid inverter. Figure 4 shows an eleven level hybrid multilevel inverter for one phase leg. Fourteen switches and five isolated sources which are equally rated are needed for one phase leg of an eleven level hybrid multilevel inverter. The output voltage levels are generated by level generation part without polarity and the output voltage polarity is decided by the polarity generation part. Then, the output voltage required will be transferred to the output according to output polarity required. When the voltage polarity required to be changed for negative polarity, the voltage direction is reversed. For the supply voltage Vdc, the six levels which are generated by level generation part are 0, Vdc/5, 2Vdc/5, 3Vdc/5, 4Vdc/5, Vdc. By using the polarity generation part, positive levels are converted into negative polarity (i.e., Vdc/5, 2Vdc/5, 3Vdc/5, 4Vdc/5, Vdc are converted to -Vdc/5, -2Vdc/5, -3Vdc/5, -4Vdc/5, -Vdc) as per the requirement of output polarity. Therefore, the required eleven levels are generated using the hybrid multilevel inverter.

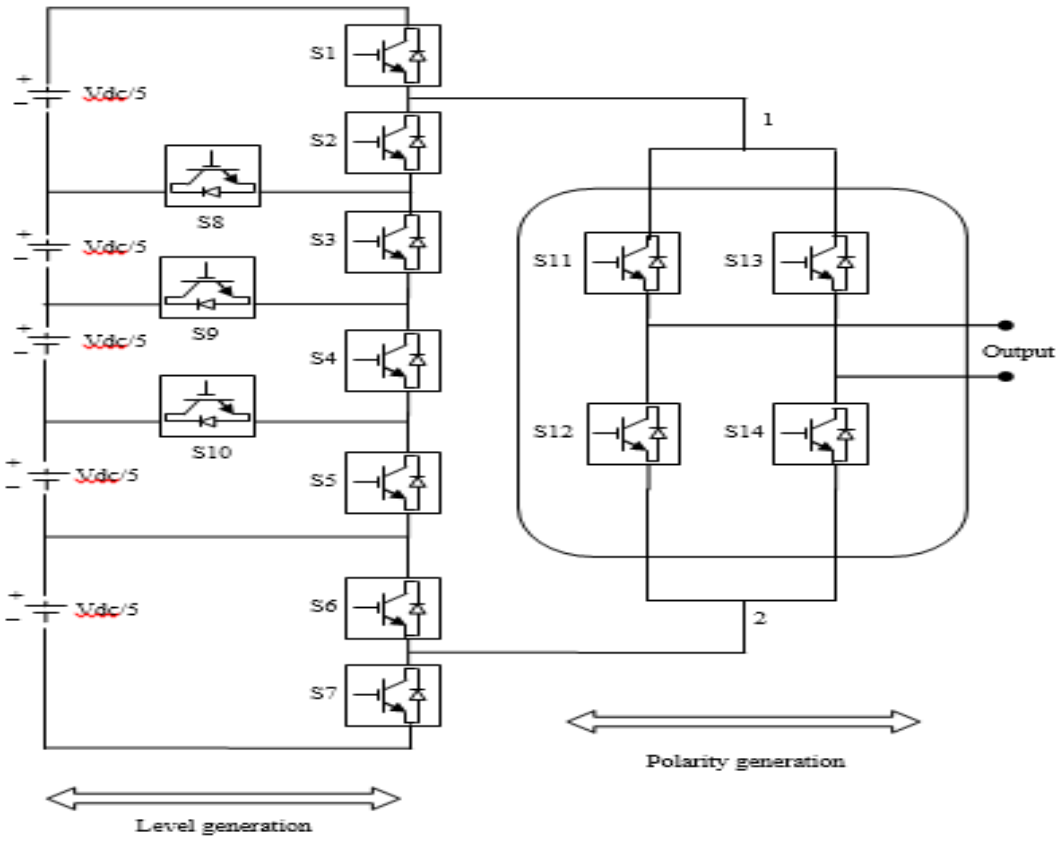

Figure 4. Structure of eleven level hybrid inverter for one phase leg

Hybrid inverter requires fewer components and half of the carriers compared to diode clamped inverter for sinusoidal pulse width modulation controller. Level generation part of hybrid inverter generates six levels and then these voltage levels will be reversed by using polarity generation part when the voltage polarity required to be changed for negative polarity. Complexities of capacitor balancing are not faced by the hybrid inverter because of fixed dc voltages. Polarity generation part works in forward and reverse modes. In Figure 4 the switches S11 and S14 will conduct in forward mode for positive output voltage polarity whereas S12 and S13 conducts in reverse mode for negative output voltage polarity. Hence, the output polarity is determined by the polarity generation part. The hybrid multilevel inverter doesn't require generation of negative pulses for negative cycle control. However, the polarity generation part performs this task while level generation part produces the number of levels required. Based on the requirement of output voltage, these levels are translated to positive or negative. In order to generate the required levels for eleven level hybrid multilevel inverter, the switching modes are shown in Table 1.

Table 1. Switching States for Eleven -Level Hybrid Inverter

Mode	0	1	2	3	4	5
1	S2, S3, S4, S5, S6	S2, S3, S4, S5, S7	S2, S3, S4, S10, S7	S2, S3, S9, S7	S2, S8, S7	S1, S7
2		S2, S3, S4, S10, S6	S2, S3, S9, S6	S2, S8, S6	S1, S6	

It describes the switch according to Figure 4 that should be turned ON to generate the required voltage level. The inverter is controlled by ten possible switching patterns. The switching mode selection should be such that during each mode transfer, less switching transients occur and also reduced switching power dissipation. By this, unwanted voltage levels during switching cycles can be avoided. The switching patterns (S2-S3-S4-S5-S6), (S2-S3-S4-S5-S7), (S2-S3-S4-S10-S7), (S2-S3-S9-S7), (S2-S8-S7) and (S1-S7) are shown in Figure 5 for producing 0 to 5 levels in the output voltage.

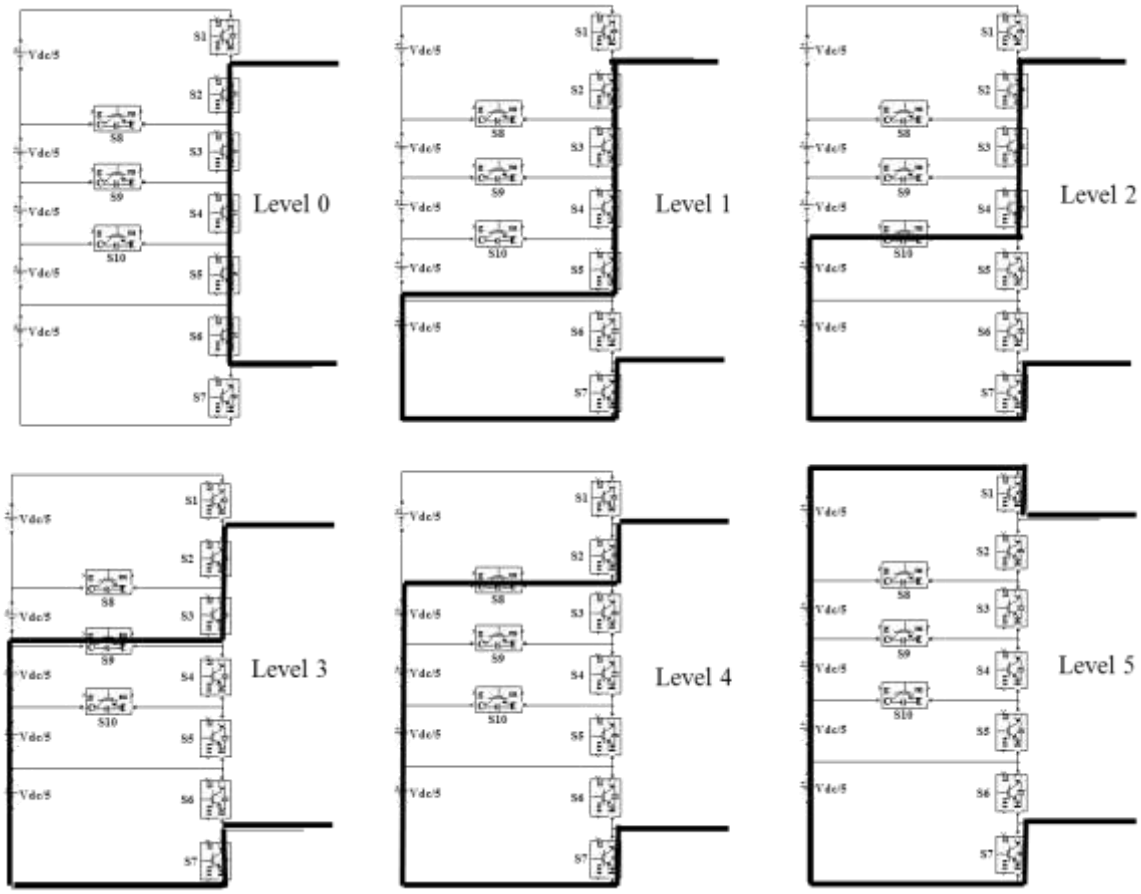

Figure 5. Switching sequence of eleven level hybrid multilevel inverter

For hybrid inverter, the modulator and five carriers for PD, APOD and CO SPWM methods are shown in Figure 6 and Figure 8. In order to meet the voltage requirements, five states are considered with certain switching patterns. To determine the overall converter efficiency, the number of switches that are required in the current path, plays an important role. Compared to conventional multilevel inverters, less number of switches are required in the hybrid multilevel inverter for conducting the circuit current which results in more efficiency. The number of power semiconductor switches required for multilevel inverters is the most important part that defines the control complexity and reliability.

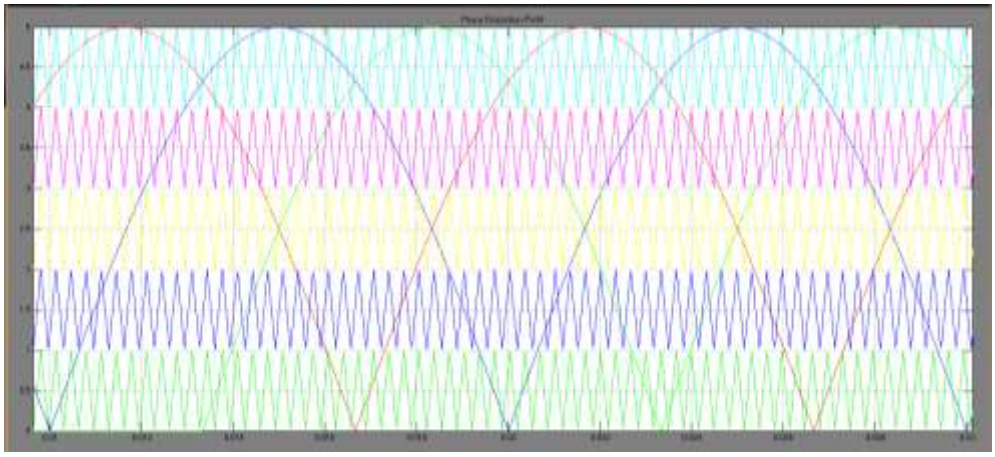

Figure 6. PD method for three phase eleven leven hybrid multilevel inverter

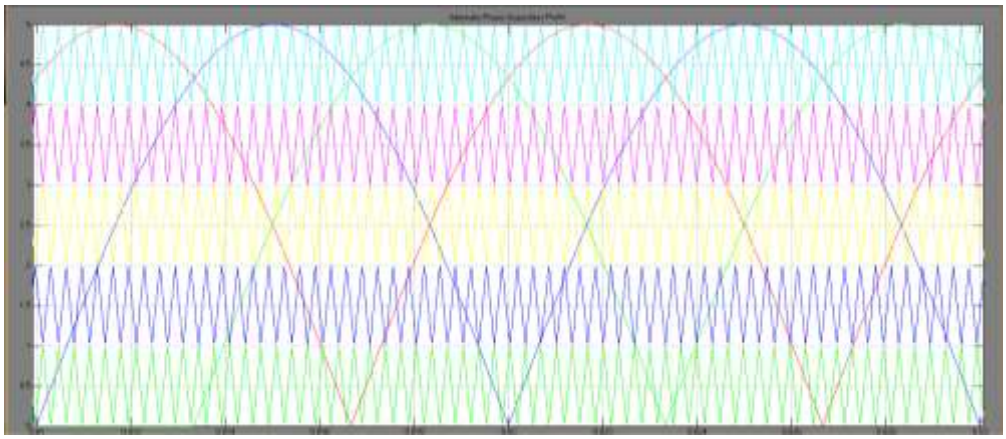

Figure 7. APOD method for three phase eleven leven hybrid multilevel inverter

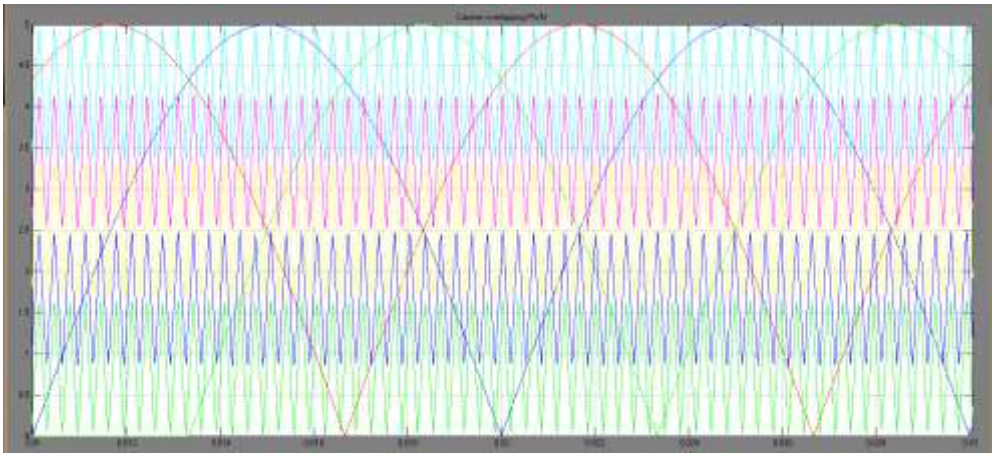

Figure 8. CO method for three phase eleven level hybrid multilevel inverter

The components required in hybrid multilevel inverter is lower than diode clamped inverter. Therefore, hybrid multilevel inverter requires reduced number of switches and less carrier signals compared to diode clamped multilevel inverter for implementation of pulse width modulation techniques

4. RESULTS AND ANALYSIS

For enhancement of output voltage and minimizing THD, phase disposition and alternate phase opposition disposition carrier based PWM methods are performed. The results of three phase eleven level diode clamped multilevel inverter and hybrid multilevel inverter are shown from Figure. 9 to Figure 21 for induction motor load. A squirrel cage induction motor used for diode clamped inverter and hybrid inverter has the following parameters: Nominal Power=10Hp, poles=4, rms voltage=400 V, frequency=50 Hz, speed=1500 rpm, stator resistance Rs=0.7384Ω, stator leakage inductance Lls=3.045mH; rotor resistance Rr′=0.7402Ω, rotor leakage inductance Llr′=3.045mH; mutual inductance Lm=0.1241H, inertia J=0.07kgm^2. The total input voltage of the three phase eleven-level hybrid multilevel inverter is 440 volts dc (5 isolated dc sources of each 88 volts). The frequency of the switches used in polarity generation part is 50 Hz and 3 KHz in level generation part.

4.1 Eleven level diode clamped multilevel inverter using PD, APOD and CO methods

The results of three phase diode clamped multilevel inverter fed induction motor for eleven level are shown in Figure 9 and Figure 10 using phase disposition method.

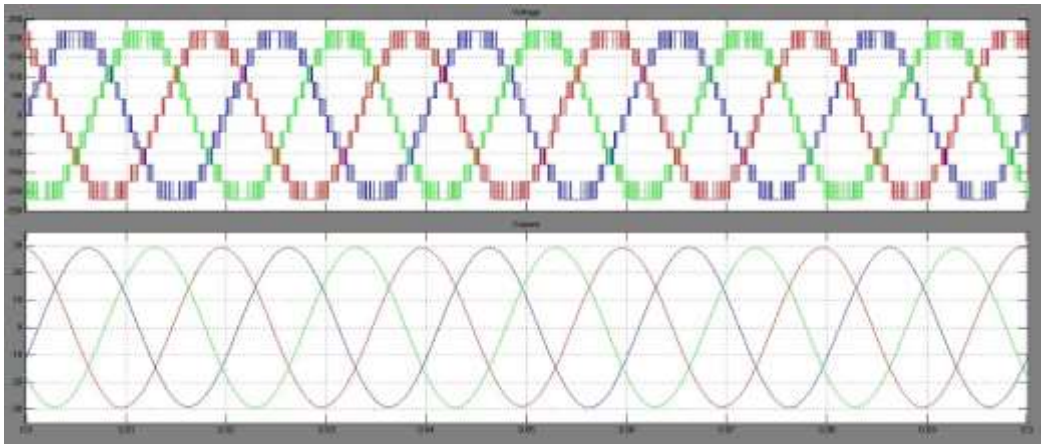

Figure 9. Waveforms of voltages and currents using PD method for DCMLI

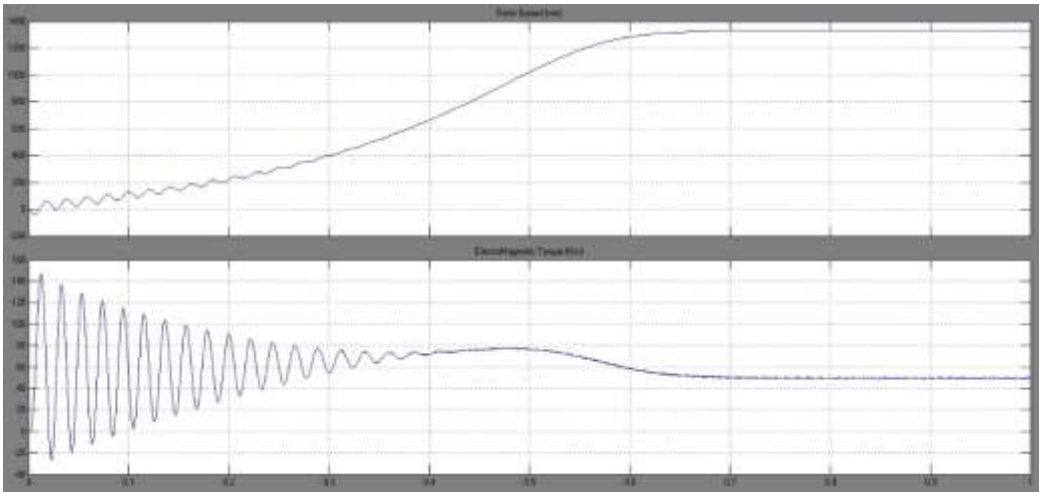

Figure 10. Speed and torque response using PD method for DCMLI

Figure 11 and Figure 12 shows the results of alternate phase opposition disposition method implemented for eleven level diode clamped multilevel inverter using induction motor load.

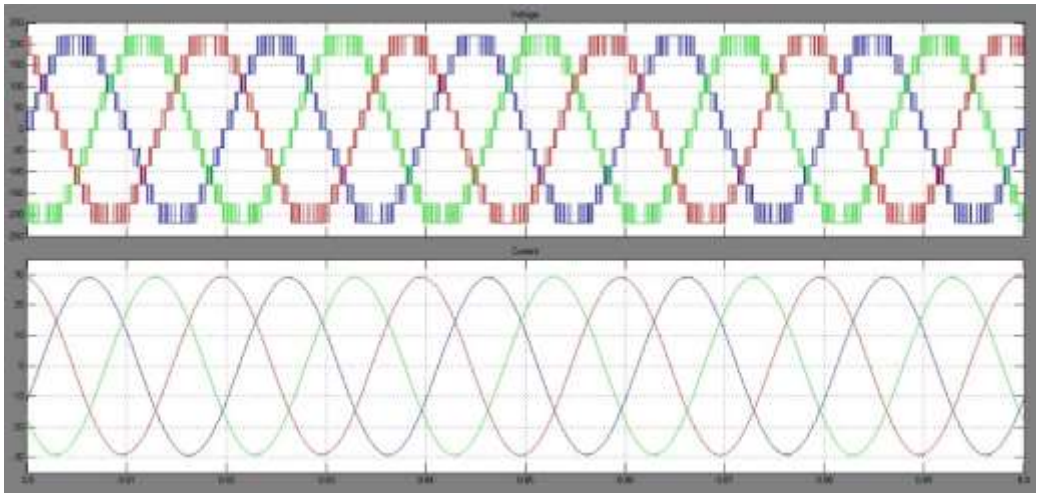

Figure 11. Waveforms of voltages and currents using APOD method for DCMLI

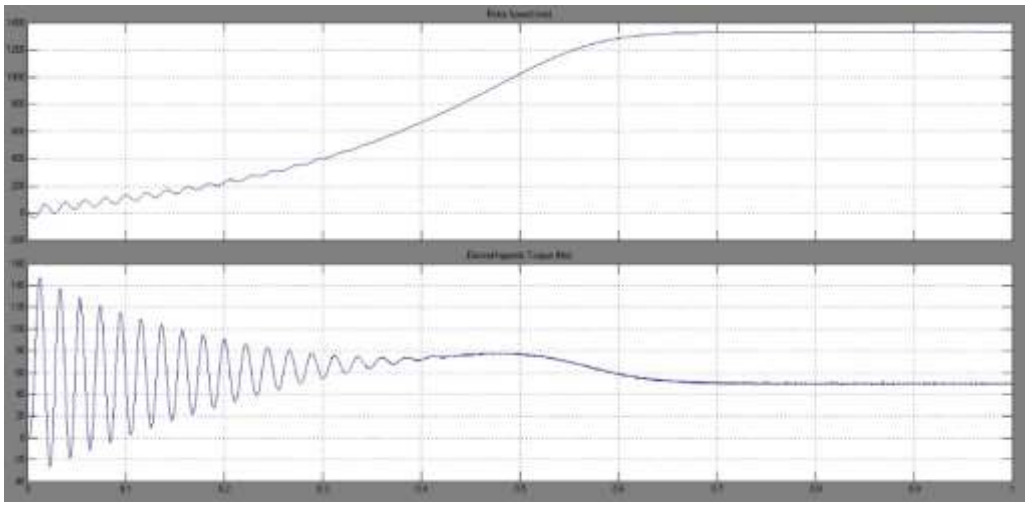

Figure 12. Speed and torque response using APOD method for DCMLI

Figure 13 and Figure 14 presents the results obtained for carrier overlapping technique for eleven level diode clamped multilevel inverter fed induction motor.

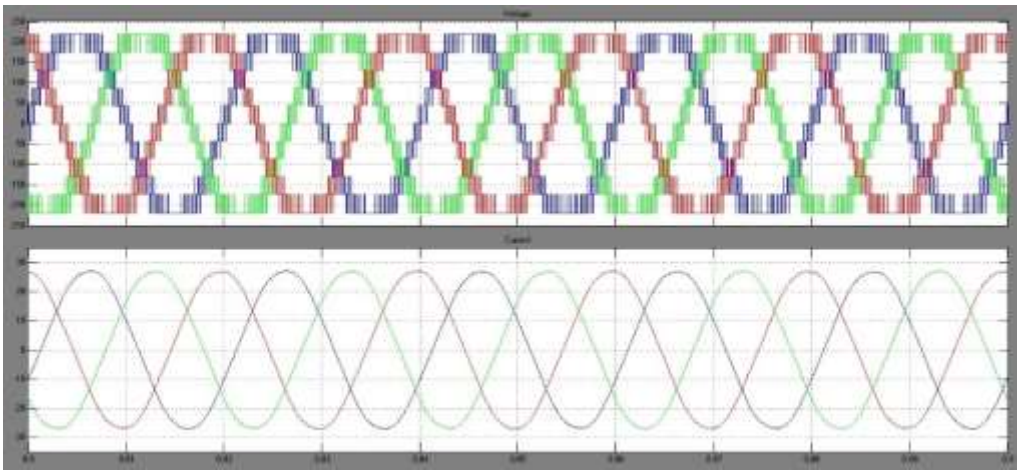

Figure 13. Waveforms of voltages and currents using CO method for DCMLI

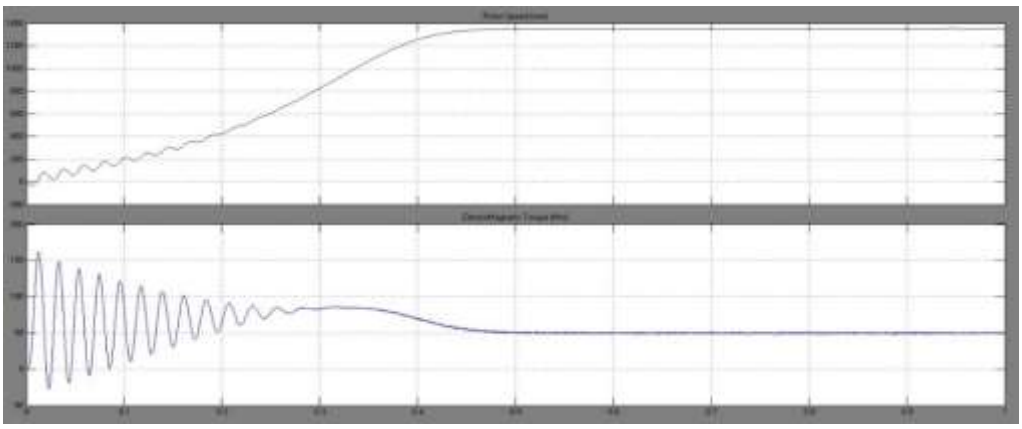

Figure 14. Speed and torque response using CO method for DCMLI

4.2. Eleven level hybrid inverter using PD, APOD and CO methods

The output voltage waveform for level generation part of eleven level hybrid multilevel inverter using phase disposition method is shown in Figure 15 that is responsible for generating required levels in positive polarity. Based on the required output polarity, the polarity generation part will transfer the required level to the output. The phase disposition method is implemented for three phase eleven level hybrid inverter fed induction motor and the results are shown in Figure 16 and Figure 17. Figure 18 and Figure 19 presents the waveforms of alternate phase opposition disposition method implemented for three phase eleven level hybrid multilevel inverter fed induction motor.

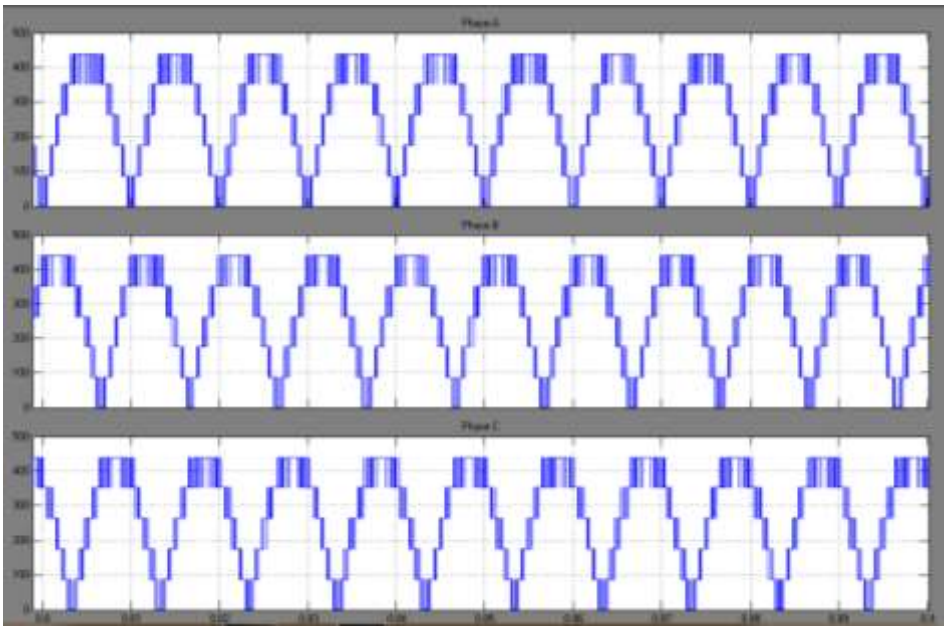

Figure 15. Output voltage waveform for level generation part of eleven level hybrid multilevel inverter

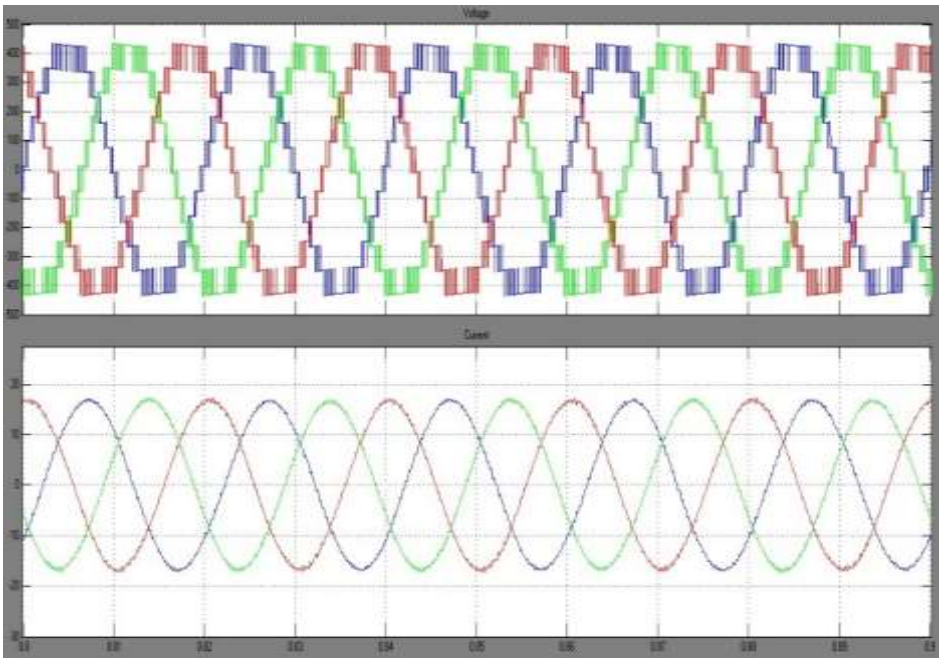

Figure 16. Waveforms of voltages and currents for hybrid inverter using PD method

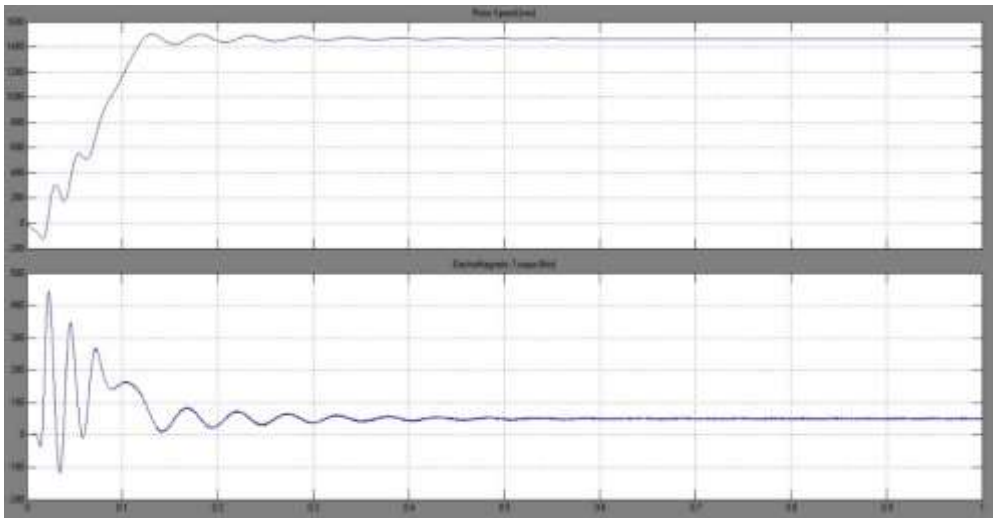

Figure 17. Speed and torque response for hybrid inverter using PD method

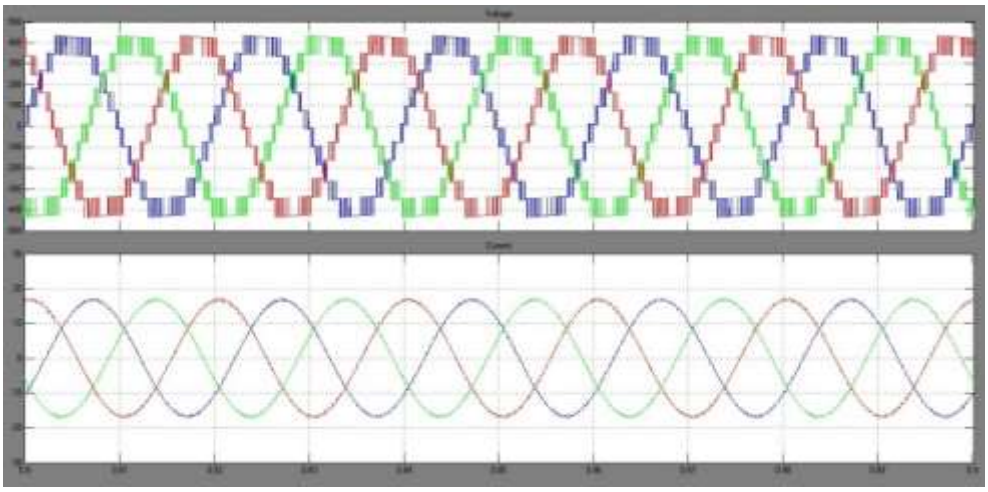

Figure 18. Waveforms of voltages and currents for hybrid inverter using APOD method

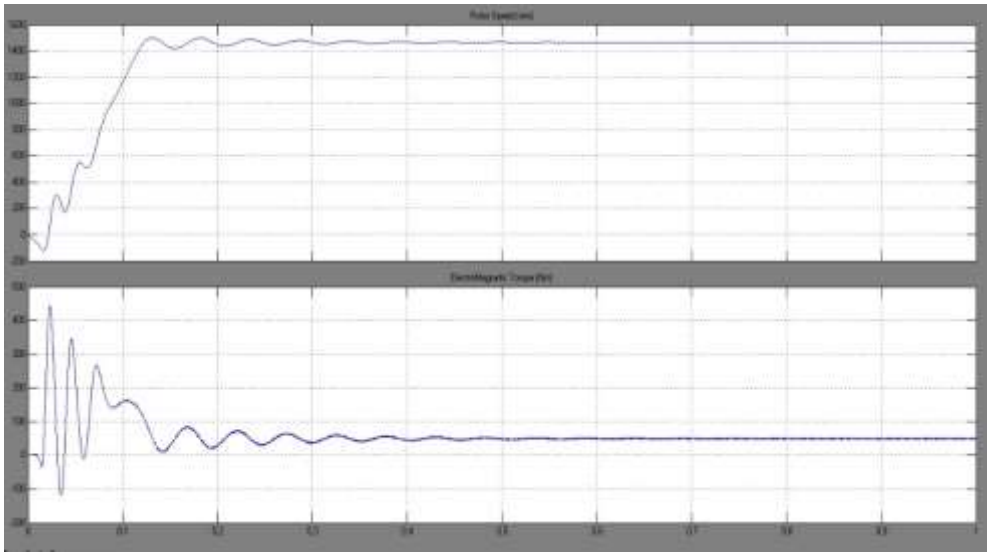

Figure 19. Speed and torque response for hybrid inverter using APOD method

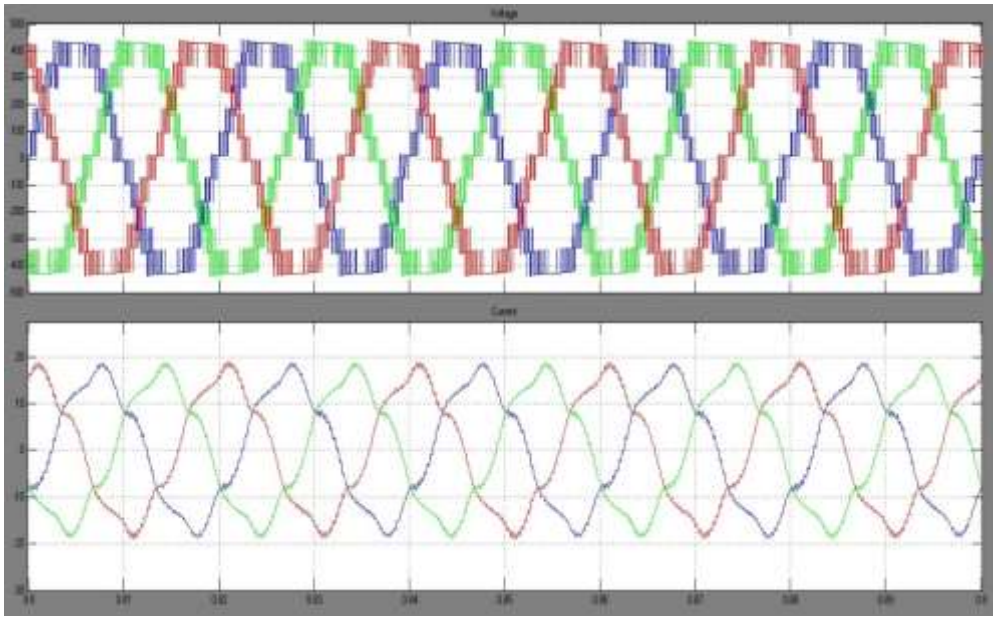

Figure 20. Waveforms of voltages and currents for hybrid inverter using CO method

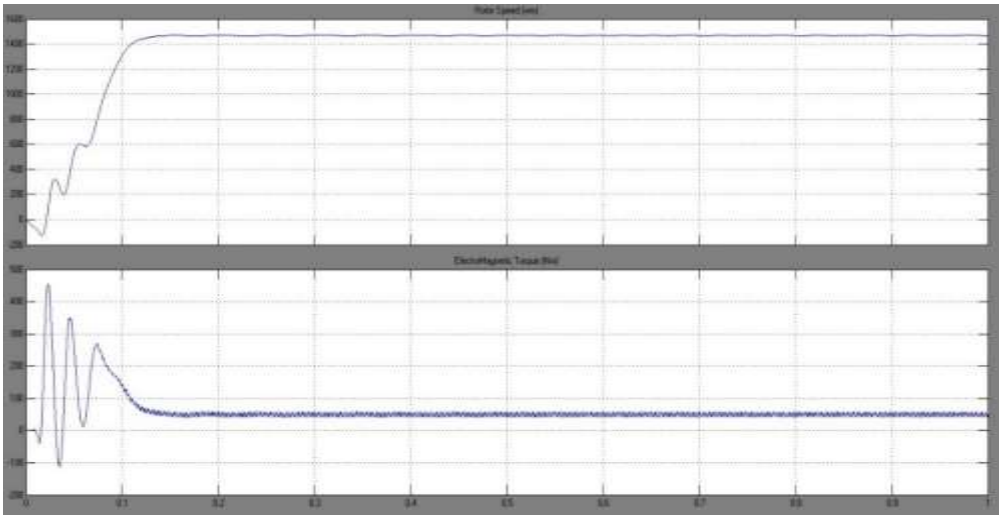

Figure 21. Speed and torque response for hybrid inverter using CO method

4.3. Comparative Analysis

The FFT analysis is carried out for output voltages of three phase eleven level diode clamped multilevel inverter fed induction motor and also for hybrid multilevel inverter using phase disposition, alternate phase opposition disposition and carrier overlapping modulation strategies. Comparison of performance in terms of THD is tabulated in Table 2.

Table 2. Comparison Table of Voltage THD (%)

Load Torque	PD method		APOD method		CO method	
	Diode clamped inverter	Hybrid Inverter	Diode clamped inverter	Hybrid Inverter	Diode clamped inverter	Hybrid Inverter
No-load	8.2	5.86	8.29	5.9	12.34	7.8
Half-load	8.33	5.92	8.36	6.02	12.28	8.02
Full-load	8.37	6	8.43	6.04	12.32	8.07

Table 3. Comparison Table of Current THD (%)

Load Torque	PD method		APOD method		CO method	
	Diode clamped inverter	Hybrid Inverter	Diode clamped inverter	Hybrid Inverter	Diode clamped inverter	Hybrid Inverter
No-load	1.96	1.19	2.13	1.08	6.66	16.85
Half-load	0.7	1.05	0.86	0.96	2.72	14.86
Full-load	0.35	0.79	0.41	0.69	1.38	11.34

5. CONCLUSION

The phase disposition, alternate phase opposition disposition and carrier overlapping sinusoidal pulse width modulation strategies have been implemented in this paper to drive the diode clamped multilevel inverter and hybrid inverter fed induction motor for eleven level output. The transition between modes in each state of hybrid inverter needs minimum commutation of switches that improves the efficiency of the inverter during switching states. The number of switches in hybrid inverter that conduct the circuit current is lower than conventional multilevel inverters i.e., diode-clamped, flying capacitor and cascaded H-bridge inverters. From the results of multicarrier based schemes, it is observed that the hybrid inverter has better performance compared to diode clamped multilevel inverter in terms of power switches that are required, control requirements and voltage THD that leads to higher reliability, reduction of converter size and cost.

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