International Journal of Applied Power Engineering (IJAPE)
Vol.8, No.3, December 2019, pp. 277~286
ISSN: 2252-8792 DOI: 10.11591/ijape.v8.i3.pp277-286

Neutral point clamped quasi Z source inverter for photovoltaic systems

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Article Info

Article history:

Received Jan 17, 2019
Revised Mar 6, 2019
Accepted Apr 20, 2019

Keywords:

Photovoltaic systems
Reduced component stress
Three level neutral point quasi Z source inverter
Voltage boosting ability

ABSTRACT

Multilevel inverters are becoming popular for power conversion in renewable energy systems, AC-DC hybrid micro grids etc. The voltage stress and inrush current through these inverter leg switches are quite higher as compared to the load ratings which increase the chances of inverter leg switch failure. A three level neutral point clamped quasi Z source inverter topology is discussed in this paper which has the features of lower component count, reduced capacitor voltage stress, and it can be operated at different control strategies to achieve wide range of voltage boosting ability, suited for photovoltaic (PV) systems. It also ensures continuous input current irrespective of the DC supply voltage variations and injects stable and smooth power to the load/grid. The effectiveness of the proposed inverter is verified by simulation results in MATLAB Simulink model as well as performing experiment with the help of a laboratory prototype.

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1. INTRODUCTION

Latest advances in solar technology and developments in power electronics offers a cost effective photovoltaic (PV) power generation for meeting electric requirement of the country. Also, strategic and supportive government incentives and tariff schemes are contributing to the wide spread usage and promotion of PV power systems. Multilevel inverter produce an output voltage that is always lower than the total dc source voltage, which is not desired for interfacing renewable sources like PV systems. The harmonic losses produced by these inverters are low, and the waveform quality will be better at higher modulation ratio. Neutral point clamped (NPC) topology is one of the most well known type of multilevel inverters and is widely spread in the market for various industrial applications. NPC inverter has a common DC bus for three phases that makes it suitable for stand alone and grid connected applications where a renewable energy resource should be used and there are limits on the number of isolated DC supplies [1-3].

Multilevel voltage source inverter (MVSI) have advantages like improvement in waveform quality, lower generated common mode voltage, lower voltage stress across semiconductors, reduced switching losses, better harmonic performance, reduced electromagnetic interference suited for high power applications [4-5]. However, MVSI may produce increased output voltage with the aid of expensive and bulky transformers (which increases the system size and weight) or by the use of dc-dc boost converters (number of power converter stages increases system control complexity and decreases the system efficiency). In MVSI, shoot through (i.e. switching all the switches in the inverter leg) results dead short circuit of the source. Shoot

through is avoided by providing dead band between switching control signal fed to the complementary switches of inverter leg, which introduces distortion in the output AC voltage. This situation can be overcome by the use of Z source inverter (ZSI) which has the features of both buck and boost abilities, to achieve the required AC voltage in a single stage, suited for various applications like renewable energy systems and electric vehicles etc.

ZSI is constructed by simply inserting a X shaped LC impedance network between the input dc source (from PV system) and inverter bridge. The impedance network, comprising symmetrically placed passive components viz inductors and capacitors, serves mainly to accumulate inductive energy during unique shoot through interval before releasing that energy for boosting the inverter output voltage in the remaining duration of a switching period. Variants in ZSI are developed by various researchers over the years [6-8]. Quasi ZSI is an improved derivative of ZSI which maintains continuous input current, less voltage stress across the switching component, and have reduced passive component ratings. Z source energy conversion technique to various inverters has been worked out with different modulation schemes with LCL filter are reported in [9, 10]. Selection of power semiconductor devices influence the efficiency of the designed inverter system with conduction losses, low switching and self discharge losses at optimal switching speed, effectiveness in terms of device failure as reported in [11-13].

Combining the features and properties discussed above, a three level single phase neutral point clamped (NPC) quasi Z Source inverter which utilises two basic quasi Z source impedance networks in a symmetrical fashion has been worked out in [14]. This NPC quasi ZSI utilizes four inductors, four capacitors and two diodes in the intermediate network for single stage boost mode of operation as well as to give a three level AC output.The overall efficiency of the photovoltaic system depends on selected inverter topology and employed modulation scheme together with loss mechanisms and grid codes as defined by IEEE/IEC standards.

In this paper, a three phase three level neutral point clamped quasi Z source inverter (3P/3L NPC qZSI) is proposed. It is a combination of quasi Z source network and three level neutral point clamped inverter. It can evenly distribute losses among switching devices by selecting the upper or lower NPC paths, leading to a substantial increase in the inverter output power. It can buck and boost the input dc voltage with short circuit immunity and possess high energy density.3P/3L NPC qZSI consists of two quasi Z (qZS) network which contains 4 inductors (L_1-L_4), 4 capacitors (C_1-C_4) to boost the input dc voltage to a higher dc voltage with reduced Z source network capacitor voltage stress and also inhibit the starting inrush current. The power circuit of 3P/3L NPC qZSI consists of 12 switches, 6 clamping diodes and 2 balancing capacitors (C_{b1} and C_{b2}) are connected with single DC source energised preferably photovoltaic system. Rest of the paper is organized as follows. Operational analysis of the proposed inverter topology with mathematical validation is presented in section 2, Simulation and experimental results are discussed in section 3 and 4 respectively and paper is ended with a conclusion in section 5.

2. OPERATIONAL ANALYSIS OF THE PROPOSED TOPOLOGY

The general circuit of 3P/3L NPC qZSI is shown in Figure 1. The input DC source realized from PV system can be splitted into two dc sources by connecting two series connected capacitors. By employing qZS network, combined dc voltage is boosted up and fed into the NPC circuitry which allows the inverter to produce three distinct voltage levels corresponding to each phase leg. It has advantages such as continuous input current, lower voltage stress across semiconductors, lower voltage blocking capability, decreased d*v*/dt, operates at higher switching frequency due to lower switching losses, possibility to use shoot through, balanced neutral point voltage, reduced capacitor voltage stress, inherent inrush current limitation and better harmonic performance. It has better elimination capability of common mode leakage current, so no additional common mode filters are required. Due to the above features, this inverter is especially suitable for PV systems, where superior harmonic performance and ability to support independent maximum power point tracking is required.

The schematic of three phase three level neutral point clamped inverter (3P/3L NPC inverter) is shown in Figure 2. It contains four switches (S_{X1}, S_{X2}, S_{X3}, S_{X4},) in each leg (X=A, B and C) and two diodes (D_{X1}, D_{X2}) clamped to the midpoint of capacitors (X=A, B and C). For phase A, gating signals of switches S_{A3} and S_{A4} are in complementary to S_{A1} and $S_{A2,}$ which is the same in other remaining legs. Hence, there are just two separate pulses to command those four switches for each phase leg. Each branch of the inverter has three output voltage levels: $0 \pm V_{dc}/2$, where V_{dc} is peak of the dc link voltage. The clamped diodes are used to produce zero voltage. The operating period of 3P/3L NPC qZSI is divided into several time intervals. Due to quasi Z source (qZS) network, another shoot through state is added when all the switches are conducting. During this state, energy is accumulated in inductors and is transferred to capacitors and output load within other states. As a result, V_{dc} is regulated only by adjusting the shoot through duty cycle.

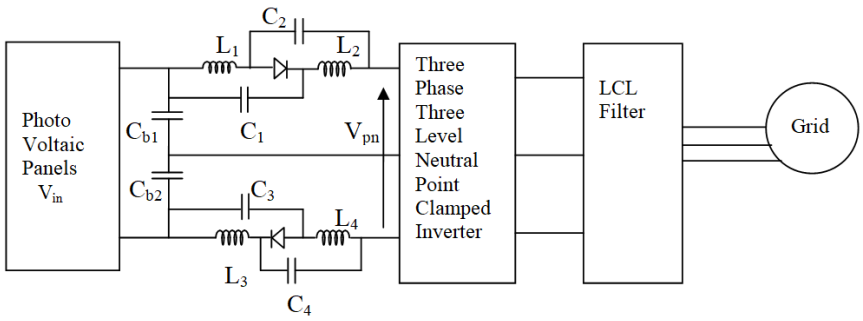


Figure 1. Three phase three level neutral point clamped quasi Z source inverter

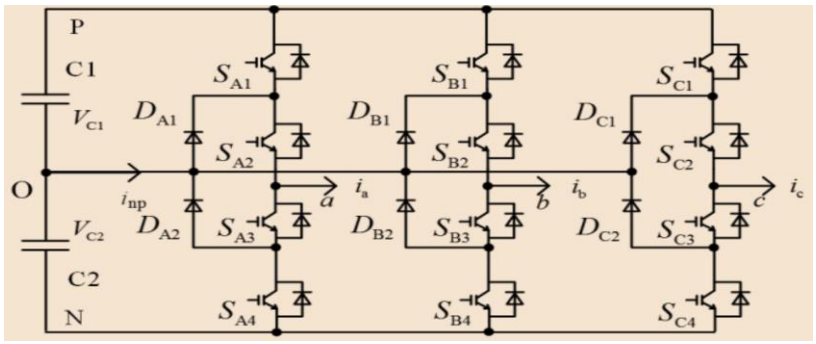


Figure 2. Circuit schematic of three phase three level neutral point clamped inverter

The behavior of qZS network can be represented by means of three equivalent circuits shown in Figure 3. Accordingly, all the switching states can be separated into three main modes: zero state as shown in Figure 3(a), active states as shown in Figure 3(b) and shoot-through state as shown in Figure 3(c) that can be applied within the zero state.

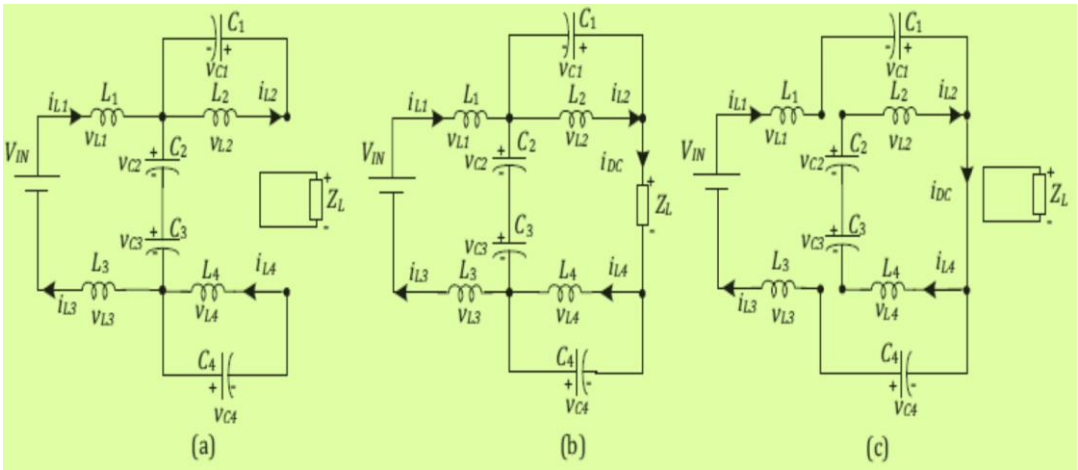


Figure 3. Equivalent circuits of 3P 3L-NPC qZSI: (a) zero state, (b) active state, (c) shoot-through state

Assuming that $L_1=L_2=L_3=L_4=L$, $C_1=C_2=C_3=C_4=C$, and the topology is symmetrical, following equations are realized [15, 16].

$$V_{L1}=V_{L2}=V_{L3}=V_{L4}=V_L \quad (1)$$

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_C \quad (2)$$

$$V_C = \frac{D_o \, V_{dc}}{2(1-2D_o)} \quad (3)$$

Where D_o is the shoot-through duty ratio,

$$D_o = T_o / T_s \quad (4)$$

The peak output phase voltage can be expressed as:

$$V_{out} = \frac{M \, V_{dc}}{2(1-2D_o)} = M \, B \frac{V_{dc}}{2} \quad (5)$$

where M is the modulation index, B is the boost factor

$$B = \frac{V_{dc}}{V_{in}} = \frac{V_{c1} + V_{c2} + V_{c3} + V_{c4}}{V_{in}} = \frac{1}{(1-2D_o)} \quad (6)$$

The output AC voltage in the three phases is given by:

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} S_{a2} & S_{a1} \\ S_{b2} & S_{b1} \\ S_{c2} & S_{c1} \end{bmatrix} \begin{bmatrix} V_{c1} + V_{c2} \\ V_{c2} \\ \end{bmatrix} \quad (7)$$

where V_{ao}, V_{bo} and V_{co} are inverter output voltages referenced to the point o (as depicted on the negative side of DC link). V_{C1} and V_{C2} are DC capacitor's voltages, respectively. T_{i0-2} denotes the triggering functions associated to each inverter leg (i=a, b, c) and it can be defined as:

$$\begin{aligned} T_{0i} &= \begin{Bmatrix} 1, & \text{if switching case 0 } (S_{i3} \text{ and } S_{i4} \text{ are ON}) \\ 0, & \text{other switching cases} \end{Bmatrix} \\ T_{i1} &= \begin{Bmatrix} 1, & \text{if switching case 1 } (S_{i2} \text{ and } S_{i3} \text{ are ON}) \\ 0, & \text{other switching cases} \end{Bmatrix} \\ T_{i2} &= \begin{Bmatrix} 1, & \text{if switching case 2 } (S_{i1} \text{ and } S_{i2} \text{ are ON}) \\ 0, & \text{other switching cases} \end{Bmatrix} \end{aligned} \quad (8)$$

Using these switching functions, the currents relations can be derived:

$$\begin{bmatrix} i_o \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} S_{a0} & S_{bo} & S_{co} \\ S_{a1} & S_{b1} & S_{c1} \\ S_{a2} & S_{b2} & S_{c2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (9)$$

Exhaustive research work have been done in developing various modulation techniques like carrier based pulse width modulation (CB PWM), space vector pulse width modulation (SVPWM), phase shift PWM, selective harmonic elimination PWM, nearest level modulation for NPC inverter with the feature of neutral point potential balancing at low switching frequencies are discussed [17-36]. These PWM techniques have different characteristics in terms of voltage utilization, harmonic suppression and switching frequency, suitable for different applications. Among these options, CB PWM is the simplest one to implement, which directly generates duty cycles for the switches from reference voltage vector, instead of sector identification and extensive numeric calculations of the switching period. Moreover, this method reduces total computation time of the controller, which in turn allows the system switching frequency to increase.

3. SIMULATION RESULTS

To verify the merits of proposed 3P/3L NPC qZSI topology, a comprehensive simulation study is performed in MATLAB Simulink environment. The simulation and experimental parameters are shown in Table 1.

Table 1. Parameters Used in Simulation and Experiment

Parameter		Value
Input Voltage, V_{in}		12 V
Quasi Z-source inductors (L_1=L_2=L_3=L_4)		2mH
Quasi Z-source capacitors (C_1=C_2=C_3=C_4)		2200 µF
LCL Filter	Inverter side inductor, L_{inv}	2 mH
	Load side inductor, L_{grid}	2 mH
	Load side capacitor, C_f	0.22 µF
Three-phase resistance load, R		10 kΩ, 10 W
Carrier frequency (fs)		2.5 kHz
Modulating signal frequency (fm).		50 Hz

LCL filter is employed to reduce the ripple which appears across the load terminals. The powered inverter is then terminated using a simple three phase resistance load for testing. Carrier frequency of 2.5 kHz has been used to generate PWM gate signals fed to the switches. Modulating signal frequency has been taken same as the frequency of required output AC voltage. The shoot through duty ratio 'D_o' and modulation index 'M' has been chosen as 0.1 and 0.9 respectively to realize the boost factor B of value 2, where the output phase voltage, V_{out} reaches a value of 24 V (AC) from the input DC supply of 12 V. Figure 4 shows the input DC voltage of value 12 V and boosted DC voltage having a peak value of 28 V which appear across the dc link. Figure 5 depicts boosted DC voltage of equal values in the range of 14 V obtained in the upper and lower legs due to quasi Z network. It is observed that the neutral point voltage is balanced in both the legs.

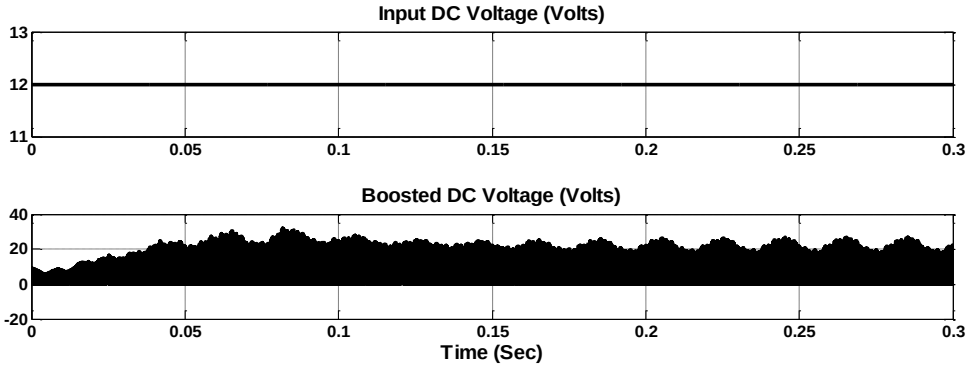


Figure 4. Input DC Voltage and boosted DC voltages

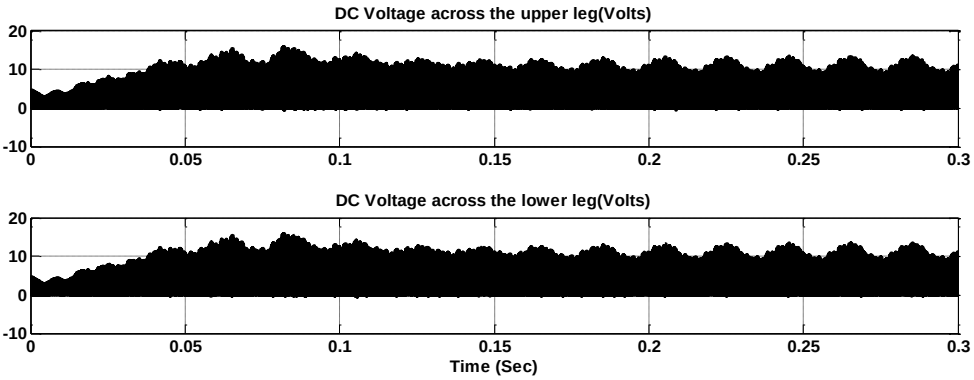


Figure 5. Boosted DC voltages of the quasi Z network obtained in the upper and lower legs

Performing simulation, voltage developed across the capacitors has been found to be same i.e. (V_{c1}=V_{c2}=V_{c3}=V_{c4}=1.77 V) with negligible ripple and input current is continuous with the value of (I_{L1}=I_{L2}=I_{L3}=I_{L4}=7.99 A). The proposed 3P/3L NPC qZSI topology can greatly reduce the Z source network capacitor voltage stress and inductor start current as mentioned above. To further inhibit the start inrush current, a soft start strategy can be applied which increases D_0 from 0 gradually at startup. Figure 6 and 7 shows current through the inductors (L_1 & L_2) and voltage across the capacitors (C_1 & C_2) of the upper quasi Z network and current through the inductors (L_3 & L_4) and voltage across the capacitors (C_3 & C_4) of the lower quasi Z network respectively.

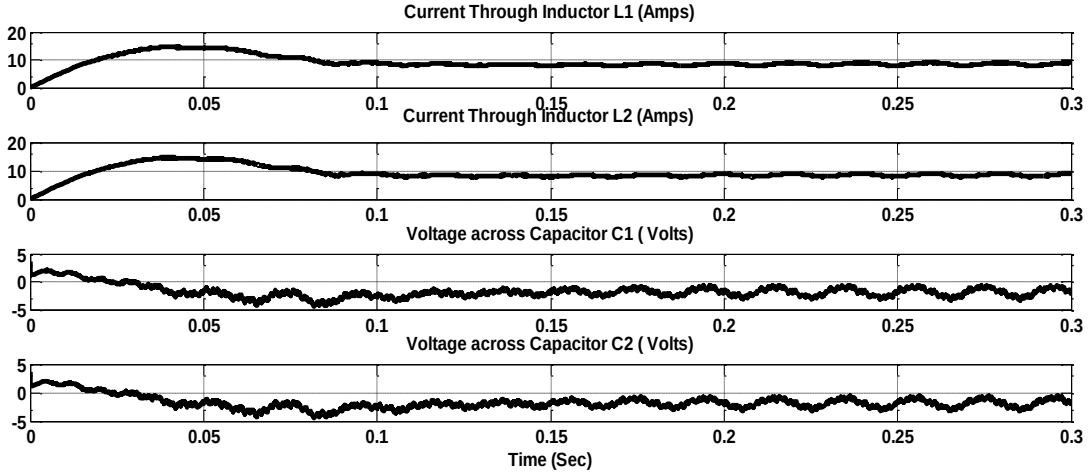


Figure 6. Current through the inductors (L_1 & L_2) and voltage across the capacitors (C_1 & C_2) of the upper quasi Z network

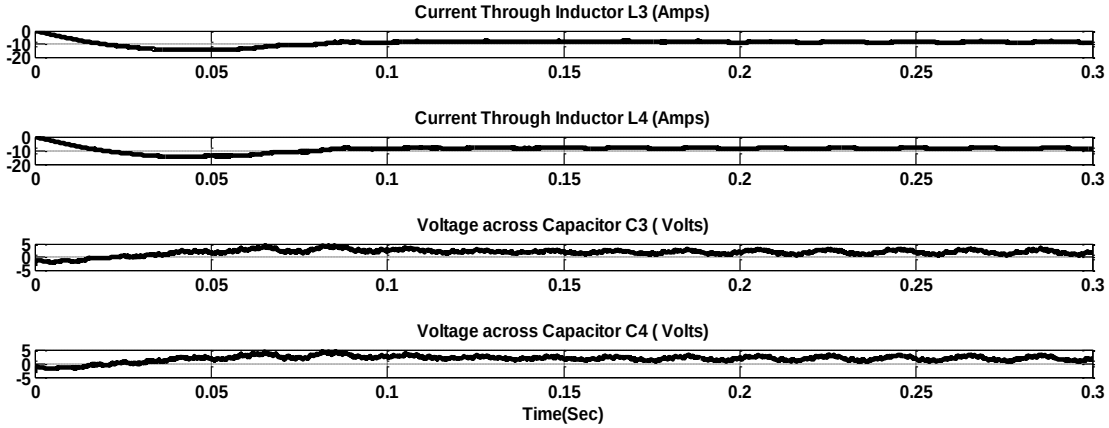


Figure 7. Current through the inductors (L_3 & L_4) and voltage across the capacitors (C_3 & C_4) of the lower quasi Z network

The simulation results of phase voltage (V_{xn}) (i.e. voltage between point 'X=R, Y, B' and 'n' shown in Figure 8). It is observed that a balanced boost three level phase voltage (V_{xn}) of value nearly 24 V has been achieved across the resistive load. The phase voltage and phase current waveform has been shown, where it has been observed that load is drawing a balanced three phase current. The input current is continuous and voltage across the DC link is uniform, and load voltage is purely sinusoidal which makes the proposed inverter suitable for photovoltaic system. The phase voltages and its corresponding total harmonics distortion (THD) of the load are observed from start time 0 sec to complete 15 cycles of the simulation FFT window. The corresponding values are given to exhibit the performance of the inverter.(for phase A, V_{out}=24.26 V, V_{THD}=2.20%, phase B, V_{out}=24.68 V, V_{THD}=2.64% and phase C, V_{out}=25.12 V, V_{THD}=3.20%).

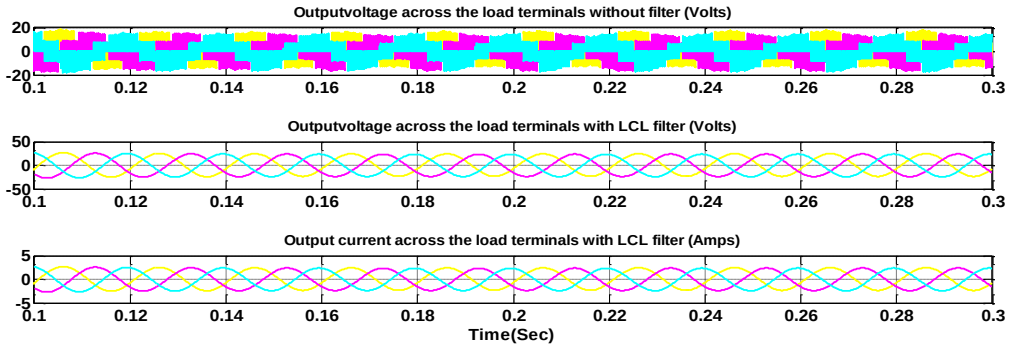


Figure 8. Simulated output AC voltage and AC current obtained across the load terminals with and without LCL filter

4. EXPERIMENTAL RESULTS

The proposed inverter is validated experimentally by developing a laboratory prototype, as shown in Figure 9. A three phase three level neutral point clamped quasi Z source inverter has been built and tested to validate its performance. The circuit parameters are given in Table 1. Twelve no.s of 8A, 500V, 0.850 Ω, N channel power MOSFET of type IRF 840 (TO-220AB package) and 6 No.s of clamping diodes of type IN4007 (DO-204AL) are employed. The controller is implemented using Arduino Uno, ATmega328 real-time controller board, which has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, SRAM 2 KB, EEPROM 1 KB, flash memory 32 KB, a USB connection, a power jack, an ICSP header, and a reset button. The sampling time of the controller has been set to 20 μs.

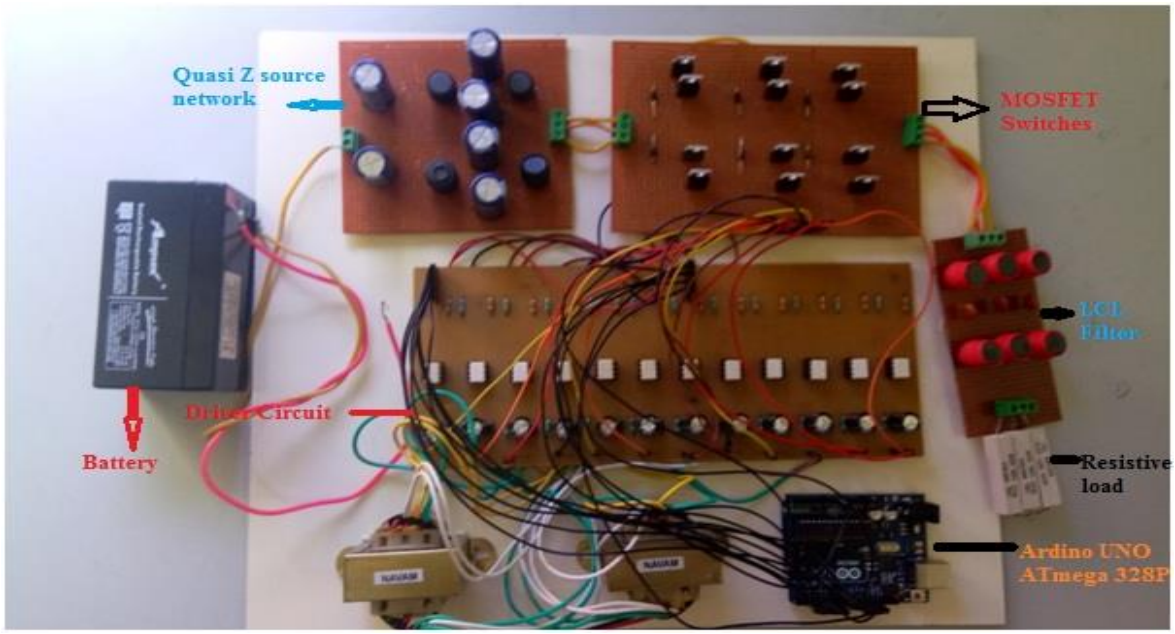
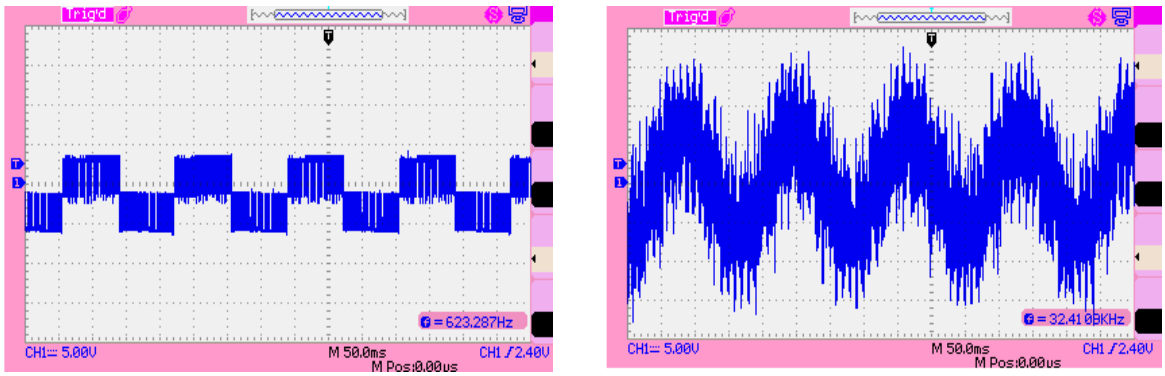


Figure 9. Experimental prototype of the proposed three phase three level neutral point clamped quasi Z source inverter

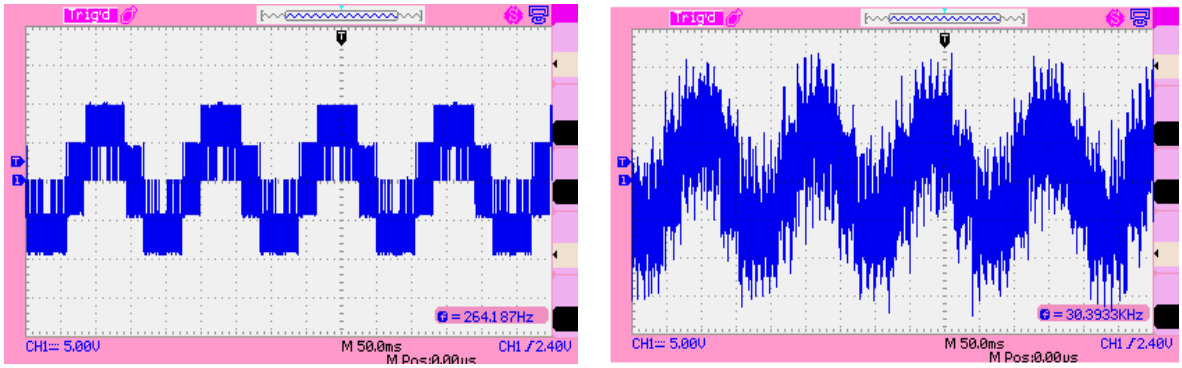
For experimental validation, a laboratory prototype has been developed for 12 volts DC input and 24 volts (r.m.s) output phase voltage (Vph) are obtained during normal operation of the inverter in carrier based switching algorithm, where its performance can be viewed in terms of voltage waveforms, shown in Figure 10 and Figure 11. 50 Watts resistive load has been connected to the inverter. Inductors and capacitors have been chosen same as taken in simulation. PWM signals have been generated using Arduino Uno, ATmega328. TLP250 and SN5401 ICs have been used as gate driver circuit and buffer circuit respectively. It should be mentioned that the inverter operates at low switching frequency of 2.5 kHz which reduces the

system switching losses, ensures high power factor, low THD grid currents, robustness and operation at constant switching frequency which makes it to be a good candidate in interfacing renewable energy sources like photovoltaic systems. The balancing of the DC capacitors voltages is also accomplished. Due to the associated non idealities, it can be realized that the voltage amplitudes of experimental results are less than the theoretical values. Performance of this proposed inverter can be made better by taking lower inductor current ripple into consideration, relaxing on capacitor voltage ripple based on the allowable ripple content. The efficiency of the proposed inverter is little low because of additional switches and diodes which introduces switching losses. But, use of less number of passive elements in the inverter reduces system volume and weight.



(a) (b)

Figure 10 Phase voltage waveforms observed at the load: (a) before filter, (b) after LCL filter



(a) (b)

Figure 11. Line voltage waveforms observed at the load: (a) before filter, (b) after LCL filter

5. CONCLUSION

A new 3P/3L NPC qZSI topology is proposed in this paper. The proposed inverter is able to boost the input DC voltage and give required three level AC output in a single stage unlike conventional NPC VSI, by utilizing shoot through state. The steady state operation of the inverter is discussed and voltage gain function is derived. Both simulation and experimented results are presented to validate its effectiveness and practicality which shows that this topology can produce continuous current, voltage with better harmonic performance, significant reduction in total harmonic distortion, Z source network capacitor voltage stress and also inhibit the start inrush current and better neutral point potential balancing with enhanced system reliability. This proposed inverter is well suited for photovoltaic systems.

ACKNOWLEDGEMENTS

This work is part of the Central Power Research Institute Project, A Government of India Society, Ministry of Power, Bangalore (Project Code: RSOP/2015/DG/6/15122015). The support of this organization is gratefully acknowledged.

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