

## ANFIS based AZSPWM methods for reduction common mode voltage in asynchronous motor drive

R. Lingangouda<sup>1</sup>, Pradeep B. Jyoti<sup>2</sup>

<sup>1</sup>Department of Electrical and Electronics Engineering, Rao Bahadur Y Mahabaleswarappa (RYM) Engineering College, Ballari, India

<sup>2</sup>Department of Electrical and Electronics Engineering, Proudhadaveraya Institute of Technology (PDIT), Hospet, India

### Article Info

#### Article history:

Received Aug 16, 2021

Revised Aug 14, 2022

Accepted Aug 20, 2022

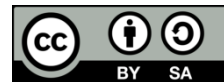
#### Keywords:

ANFIS  
AZSPWM  
CMV  
SPWM  
SVPWM

### ABSTRACT

Space vector pulse width modulation (SVPWM) is a popular technique in the field of variable frequency induction motor drives. It gives better working and good direct current bus utilization in comparison to the sinusoidal PWM (SPWM) method. However, it decreases harmonic fluctuations and generates high common mode voltage (CMV) fluctuations, which results in common mode currents inside the motor. Hence, the performance of the motor may be deteriorated. To reduce the CMV, this paper presents a family of active zero state PWM (AZSPWM) methods using an adaptive neuro-fuzzy interference system (ANFIS). The proposed approach uses a five-layer hybrid learning algorithm for training the network. The training data is obtained from the classical SVPWM method. To analyze the proposed PWM methods, simulation is carried out using MATLAB and evaluated.

*This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.*



### Corresponding Author:

R. Lingangouda  
Department of Electrical and Electronics Engineering  
Rao Bahadur Y Mahabaleswarappa (RYM) Engineering College  
Cantonment, Ballari-583104, Karanataka, India  
Email: gouda402@rymec.in

## 1. INTRODUCTION

The variable frequency induction motor drive (IMD) has become well known in various speed control applications with the help of pulse width modulation (PWM) methods. A detailed survey on the performance of various PWM methods was conducted in [1] and concluded that space vector pulse width modulation (SVPWM) gives good performance at all modulation indices over the SPWM method. The implementation of SVPWM was discussed in detail in [2] for the generation of pulses for the inverter. However, the SVPWM generates high common mode voltage (CMV) fluctuations because of the null voltage vectors. The CMV results in circulating the common mode currents (CMC), which results in leakage or bearing currents in the motor. The modelling of this current and CMV is addressed in [3]–[5], and the effects of CMV and CMC are described. The CMV can be reduced by using active and passive filters, which raise the cost and weight of the structure [6].

To mitigate CMV without using the passive and active filters, various PWM methods were developed in [7]–[13]. These PWM methods use only active vectors for the generation of pulses. These PWM methods use different combinations to maintain the volt-time balance. Among various combinations, one popular approach is to use two opposite active states to create an effective zero voltage. This approach is known as the active zero state approach. By using the different combinations, three PWM methods can be derived as explained in [13]. In all active zero state PWM (AZSPWM) methods, the modulating signals are

the same as in the SVPWM method. But, the selection of the carrier signal will be different from sector to sector.

In recent years, the usage of fuzzy and neural networks has been increasing in various applications, as explained in [14]. In this, the modulating signals of SVPWM are derived by using the neural network approach. The combination of fuzzy and neural networks, which is known as adaptive neuro-fuzzy interference system (ANFIS) applications, has also increased in recent years. The implementation of SVPWM using the ANFIS was described in [15]. In this paper, the signal variations for SVPWM and AZSPWM methods are obtained by using the concept of ANFIS, and then the pulses are derived for SVPWM and AZSPWM methods.

**2. AZSPWM METHODS**

For a 3-phase, 2-level inverter, eight voltage vectors are possible among which, two are zero states ( $V_0$  and  $V_7$ ) and remaining are active states ( $V_1$  to  $V_6$ ) as shown in Figure 1. The allusion voltage vector ( $V_{ref}$ ) in Figure 1 equivalent to the required value of the fundamental components for the output voltages, which is sampled in each slice time period ( $T_s$ ). In each sector with the help of corresponding active and zero states, average voltage vector is produced for each and every sampling time period. This can be represented as given in (1) for first sector.

$$V_{ref}T_s = V_1T_1 + V_2T_2 + V_0T_0 + V_7T_7 \tag{1}$$

Then, the active and zero state times can be derived as given in (2), (3) and (4).

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \left( \sin\left(\frac{\pi}{3} - \alpha\right) \right) T_s \tag{2}$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i (\sin \alpha) T_s \tag{3}$$

$$T_z = T_s - T_1 - T_2 \tag{4}$$

Where  $M_i$  is known as modulation index and defined as  $M_i = \pi V_{ref}/2V_{dc}$ . The CMV is defined as the potential difference between neutral point to middle point of dc supply of the inverter as shown in Figure 2 and given by as in (5).

$$V_{com} = \frac{V_{ao}+V_{bo}+V_{co}}{3} \tag{5}$$

As the VSI generates pulsed voltages, the instantaneous CMV will not be zero. The CMV magnitudes will be  $\pm V_{dc}/6$  and  $\pm V_{dc}/2$  for active and zero states respectively. As the SVPWM technique uses two zero states in each  $T_s$ , it generates high CMV variations. Hence, to mitigate the CMV, the proposed AZSPWM methods will not use zero states and in order to create effective zero state, two converse active vectors will be used. The application of voltage vectors in each sector is given in Table 1 for SVPWM and AZSPWM methods.

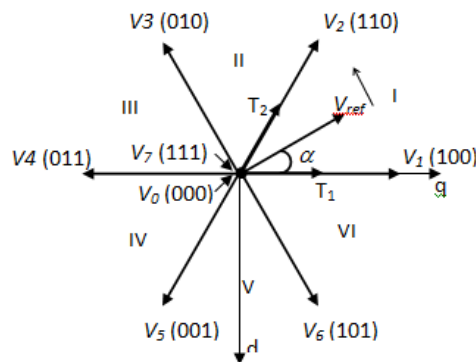


Figure 1. Voltage space vectors of a 3-phase, 2-level inverter

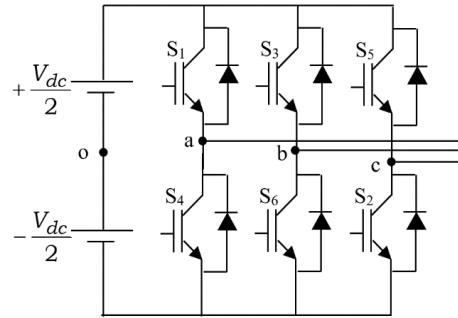


Figure 2. 3-phase, 2-level inverter

Table 1. Volt-time balance sequence of SVPWM and AZSPWM methods

Sector	SVPWM	AZSPWM1	AZSPWM2	AZSPWM3
1	0127-7210	3216-6123	5122-2215	4211-1124
2	0327-7230	4321-1234	6233-3326	5322-2235
3	0347-7430	5432-2345	1344-4431	6433-3346
4	0547-7450	6543-3456	2455-5542	1544-4451
5	0567-7650	1654-4561	3566-6653	2655-5562
6	0167-7610	2165-5612	4611-1164	3166-6613

**3. ANFIS APPROACH FOR PROPOSED AZSPWM METHODS**

The schematic diagram of 2-level inverter fed induction motor with the proposed ANFIS approach is shown in Figure 3. The d, q-axes sampled voltages are the inputs for ANFIS block to generate the modulating signals of SVPWM method as explained in [15]. The rule procedure and structure of the ANFIS is explained in detailed in [15]. After obtaining the modulating signals of SVPWM algorithm, these will be collating with a common triangular signal to obtain the sampling pattern of SVPWM algorithm. Whereas, for the generation of pulse pattern of AZSPWM methods both positive and negative carrier signals will be used as given in Table 2 in each sector [13].

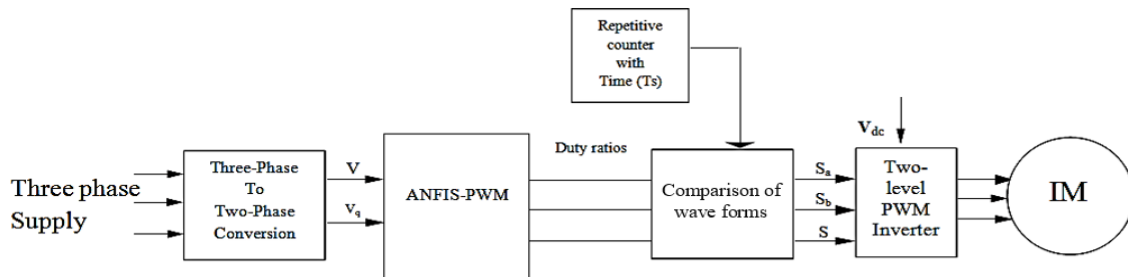


Figure 3. Proposed ANFIS based PWM methods

Table 2. Generation of pulse pattern of AZSPWM methods

Methods	Phase	A1	A2	A3	A4	A5	A6
ASPWM1	A	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$
	B	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$
	C	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$
ASPWM2	A	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$
	B	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$
	C	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$
ASPWM3	A	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$
	B	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$	$-V_{tri}$	$-V_{tri}$
	C	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	$+V_{tri}$	$+V_{tri}$	$+V_{tri}$

**4. SIMULATION RESULTS AND DISCUSSION**

To validate the SVPWM and AZSPWM algorithms, simulation is performed with the help of MATLAB platform. The study is done with switching frequency of 5 kHz. The IM rating referred for case study is of 4- KW, 400-V, 1470- rpm, 4-pole, 50 -Hz, 3-phase IM having the following variables:  $R_s=1.57-\Omega$ ,

$R_r = 1.21-\Omega$ ,  $L_s=0.17\text{-H}$ ,  $L_r=0.17\text{-H}$ ,  $L_m = 0.165 \text{-H}$  and  $J=0.089\text{-Kg.m}^2$ . The outcomes are presented in Figures 4 to Figure 7 with the harmonic distortion of  $I_L$  (Line current). From the results, it is concluded that the AZSPWM methods will mitigate the CMV with slightly high harmonic fluctuations.

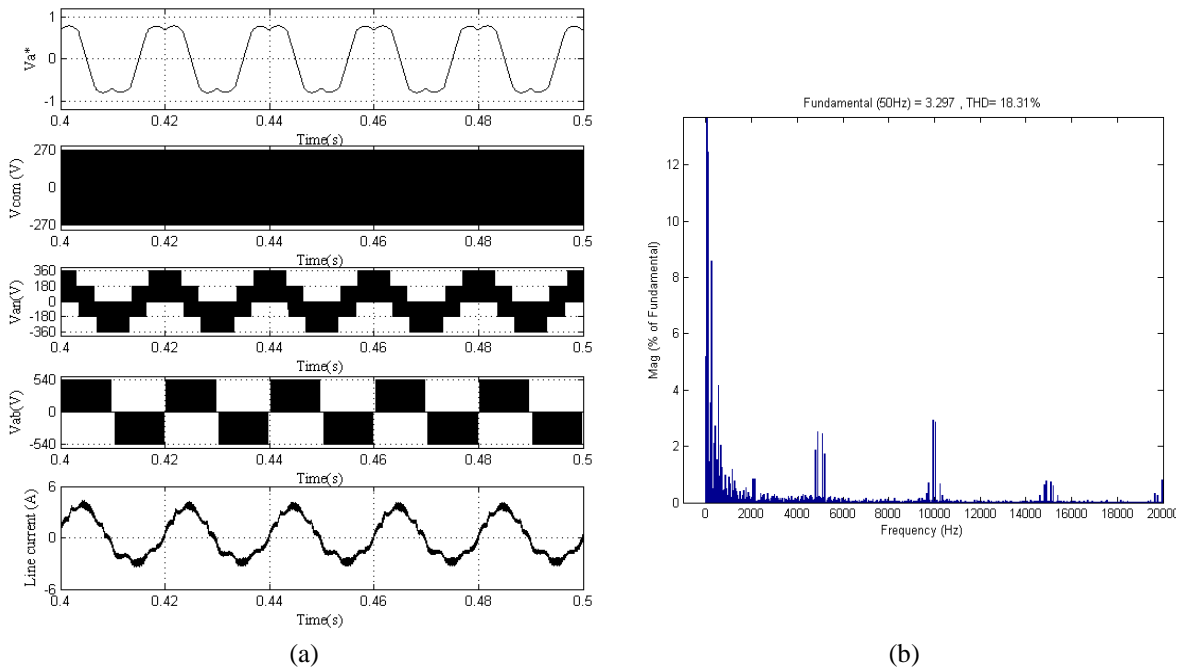


Figure 4. Steady state graphs and CMV for SVPWM data stand on (a) v/f control IM drive and (b) spectrum of  $I_L$  distortion

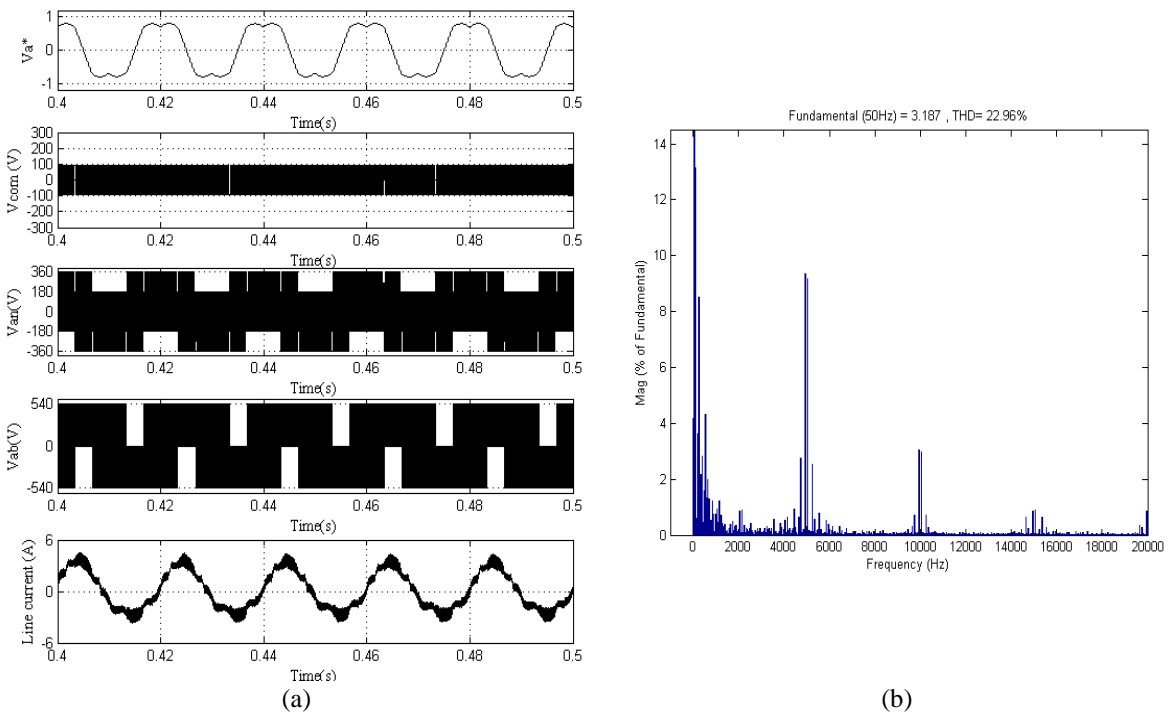


Figure 5. Steady state graphs and CMV for AZSPWM1 data stand on (a) v/f control IM drive and (b) spectrum of  $I_L$

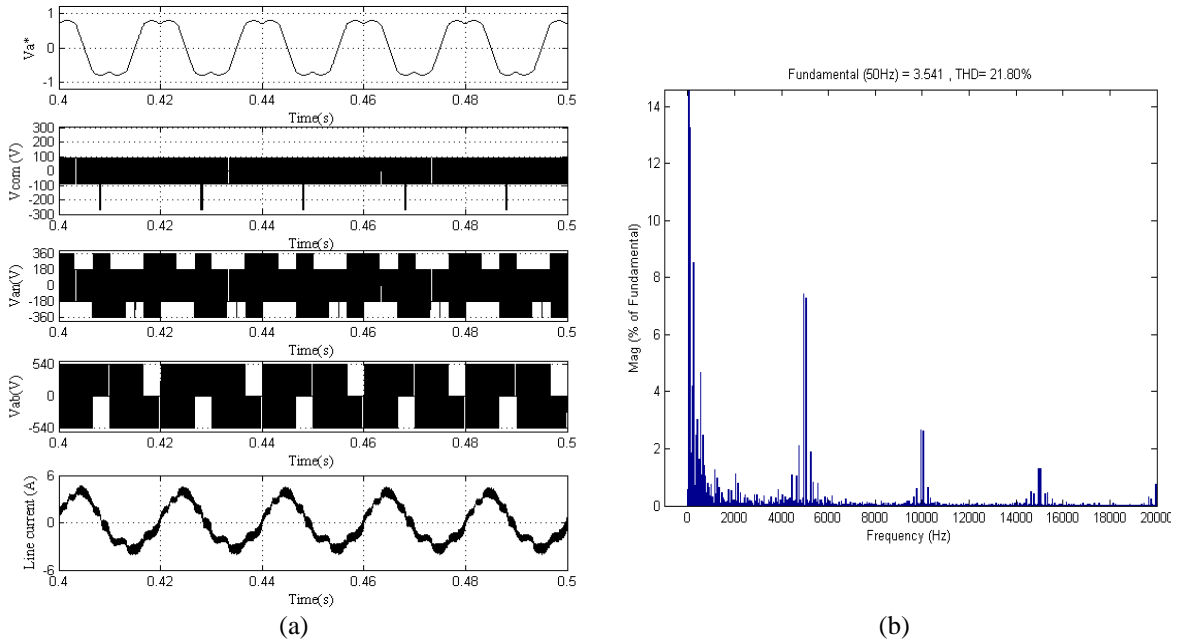


Figure 6. Steady state graphs and CMV for AZSPWM2 data stand on (a) v/f control IM drive and (b) spectrum of  $I_L$  distortion

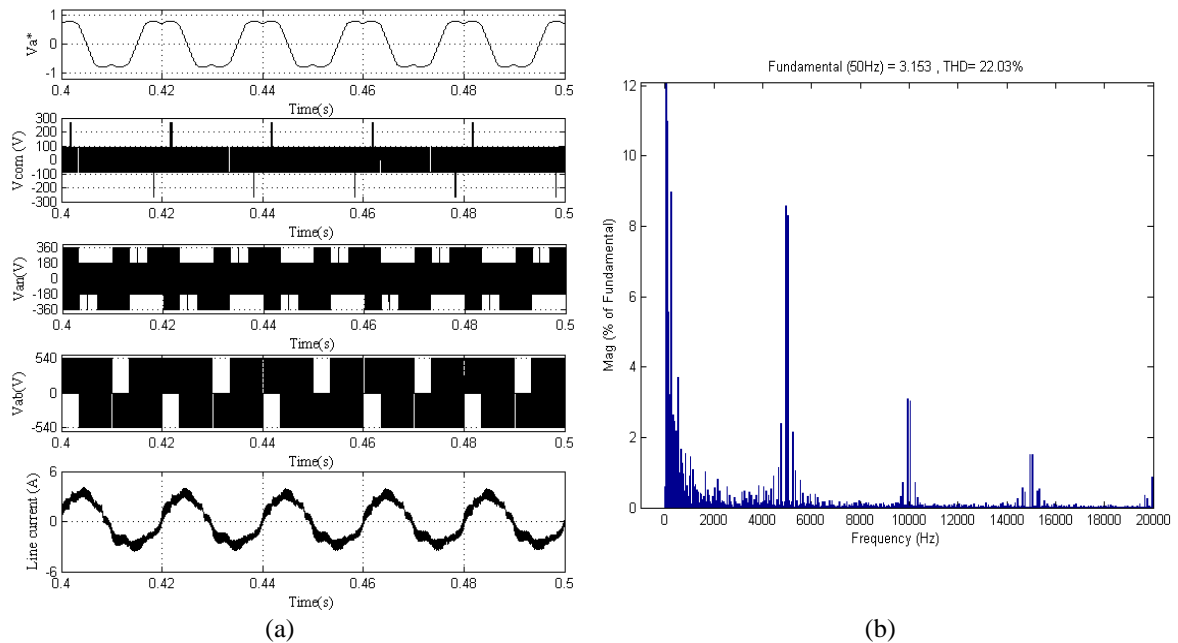


Figure 7. Steady state graphs and CMV for AZSPWM3 data stand on (a) v/f control IM drive and (b) spectrum of  $I_L$  distortion

5. CONCLUSION




The SVPWM gives good steady state performance and popular in various applications. But it exhibits more CMV fluctuations due to the usage of zero state. Hence, to reduce the CMV, in this paper ANFIS based AZSPWM methods are presented avoiding Zero State. To prove the effectiveness, simulation Analysis has been done and output are tabulated. From the output results, it is finalized that the AZSPWM methods give high harmonic fluctuations due to the opposing signals in the  $V_L$ . But, the AZSPWM methods give reduced CMV variations compared to SVPWM method.

## REFERENCES




- [1] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Transactions on Industrial Electronics*, vol. 39, no. 5, pp. 410–420, 1992, doi: 10.1109/41.161472.
- [2] H. W. van der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988, doi: 10.1109/28.87265.
- [3] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1105–1114, 1996, doi: 10.1109/28.536872.
- [4] S. Ogasawara, H. Ayano, and H. Akagi, "Measurement and reduction of EMI radiated by a PWM inverter-fed AC motor drive system," *IEEE Transactions on Industry Applications*, vol. 33, no. 4, pp. 1019–1026, 1997, doi: 10.1109/28.605744.
- [5] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, 1996, doi: 10.1109/28.491472.
- [6] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a PWM inverter," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 835–841, Sep. 1998, doi: 10.1109/63.712285.
- [7] Y.-S. Lai and F.-S. Shyu, "Optimal Common-Mode Voltage Reduction PWM Technique for Inverter Control With Consideration of the Dead-Time Effects—Part I: Basic Development," *IEEE Transactions on Industry Applications*, vol. 40, no. 6, pp. 1605–1612, Nov. 2004, doi: 10.1109/TIA.2004.836149.
- [8] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou, "Optimal Common-Mode Voltage Reduction PWM Technique for Inverter Control With Consideration of the Dead-Time Effects—Part II: Applications to IM Drives With Diode Front End," *IEEE Transactions on Industry Applications*, vol. 40, no. 6, pp. 1613–1620, Nov. 2004, doi: 10.1109/TIA.2004.836151.
- [9] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization - a survey," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.*, 2006, pp. 1162–1167. doi: 10.1109/SPEEDAM.2006.1649943.
- [10] L. H. Kim, N. K. Hahm, C. Y. Won, K. H. Han, and Y. R. Kim, "A new PWM method for conducted EMI reduction in inverter fed motor drive," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, 2005, vol. 3, pp. 1871–1876. doi: 10.1109/APEC.2005.1453306.
- [11] R. M. Tallam, R. J. Kerkman, D. Leggate, and R. A. Lukaszewski, "Common-Mode Voltage Reduction PWM Algorithm for AC Drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1959–1969, Sep. 2010, doi: 10.1109/TIA.2010.2057396.
- [12] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 2, pp. 469–476, 1999, doi: 10.1109/28.753643.
- [13] A. M. Hava and E. Un, "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 241–252, Jan. 2009, doi: 10.1109/TPEL.2008.2005719.
- [14] M. P. Kazmierkowski, L. E. B. Da Silva, B. K. Bose, and J. O. P. Pinto, "A neural-network-based space-vector PWM controller for voltage-fed inverter induction motor drive," *IEEE Transactions on Industry Applications*, vol. 36, no. 6, pp. 1628–1636, 2000, doi: 10.1109/28.887215.
- [15] G. Durgasukumar and M. K. Pathak, "Comparison of adaptive Neuro-Fuzzy-based space-vector modulation for two-level inverter," *International Journal of Electrical Power & Energy Systems*, vol. 38, no. 1, pp. 9–19, Jun. 2012, doi: 10.1016/j.ijepes.2011.10.017.

## BIOGRAPHIES OF AUTHORS



**R. Linganagouda**    Graduated in the year 2009 from VTU Belagavi, Karnataka & M. Tech from VTU Belagavi, and Karnataka in the year 2012. He is currently pursuing Ph. D at VTU Belagavi, Karnataka. He is presently working as Assistant Professor in the Department of Electrical and Electronics Engineering at RYM Engineering college Ballari, Karnataka, India. His research areas include PWM techniques, and Analysis of common mode voltage of Induction motor drives. He can be contacted at email: gouda402@rymec.in.



**Pradeep B. Jyoti**    Graduated from Karnataka University Dharwad, Karnataka in the year 1986, M.E from Gulbarga University, Gulbarga in the year 1989 and Ph.D at Jawaharlal Nehru Technological University, Hyderabad, India in the year 2014. He is presently working as Professor in the Department of Electrical and Electronics Engineering, at PDIT, Hosapete, India. His research areas include SVPWM techniques, and Vector control of electrical drives. He can be contacted at email: pradeepbjyoti@gmail.com.