

# Analysis of switched impedance source/quasi-impedance source DC-DC converters for photovoltaic system

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## ABSTRACT

This paper proposes the switched impedance source converter (SZSC) or switched quasi impedance source DC-DC converter (S-qZSC) based photovoltaic (PV) grid-connected systems. To increase the voltage from low level to high level, all PV grid-connected systems need step-up DC-DC converters. This step-up factor can be increased by connecting the terminals of a traditional quasi impedance source DC-DC converter with an additional diode and a switch. In this proposed converter, the capacitor not only serves as a filter. It is, however, bound in series to the charging loops of the inductors. On the one hand, saturated inductors can trigger instability, which can be avoided. When used for dc-ac conversion, however, the modulation index of the backend H-bridge can be set to a wider range. As compared to existing Z-source-based systems, a shorter duty period results in a higher boost factor.

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## 1. INTRODUCTION

The increased use of renewable energy has been fueled by the global energy crisis [1]. One of the most important players in the battle against the energy crisis is solar energy. As shown in Figure 1, photovoltaic (PV) arrays are a low dc source voltage that requires a high step-up DC-DC converter to transform to a higher voltage level before connecting to a grid-connected inverter [2], [3]. However, a higher switching duty cycles is needed to achieve the high voltage gain, which decreases efficiency and causes inductor saturation. Traditional impedance source inverter (ZSI) has many flaws, including a high inrush current, discontinuous input current, and higher voltage stress on condensers [4]–[11] suggests quasi impedance source inverters to overcome limitations. The boost factor of the ZSI can be increased using a variety of methods. When diodes, inductors and capacitors are connected to the Z-source network, for example, a higher dc-link voltage is generated [12], [13]. A cascaded quasi-Z-source network [14] is used in the topology to achieve higher voltage gain.

Currently, research on the Z-source network focuses primarily on the conversion of DC-AC power, despite the fact that the Z-source network, with its unique advantages, can also be used in the conversion of DC-DC [15], [16]. Figure 2 depicts the initial impedance source DC-DC converter with a  $1/(1-2D)$  boost factor (switch S duty cycle is D). Yu *et al.* [17] defined a hybrid three Z-topology boost converter that unite traditional Z-source topology in a number of different ways. The boost factor, which is best suited to PV applications, can be greater than  $1/(1-4D)$ . The main disadvantage is that it necessitates a large number of passive materials, making it more expensive and larger in volume.

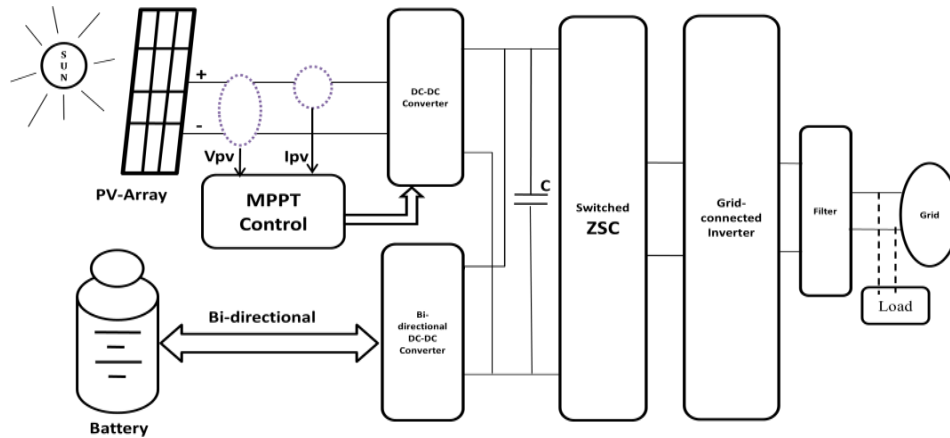


Figure 1. The grid-connected photovoltaic system

This work introduces a novel class of DC-DC converter designed for PV systems with low passive components. By connecting the standard output ports of the impedance source/quasi-impedance source topology with one more switch and diode as shown in Figure 1. When the switches are switched on, the output capacitor not only acts as the DC connection. However, it is bound in cascaded to the charging loops of the inductors. The proposed boost converter, Will achieve the identical voltage gain of  $1/(1-4D)$  with fewer modules than the hybrid three Z-topology boost converters in lesser unit cost and high power density [17]. In another way, for the same boosting voltage, the latest topologies need a low duty ratio, resulting in smaller inductors and a lower risk of inductive saturation [18]. Figure 2(a) depicts the standard impedance source converter circuit, which includes the two inductors ( $L1$  and  $L2$ ) and two capacitors ( $C1$  and  $C2$ ) in an X-shape. Figure 2(b) indicates one switching cycle. The quasi-Z-source inverters (qZSIs) continuous current mode state consists of two states: shoot-through and non-shoot-through. Figure 2(c) represents changeable input current that can arise when the circuit starts to increase the current by turning a portion of the short zero states into open zero states depending on the load condition and capacitance value.

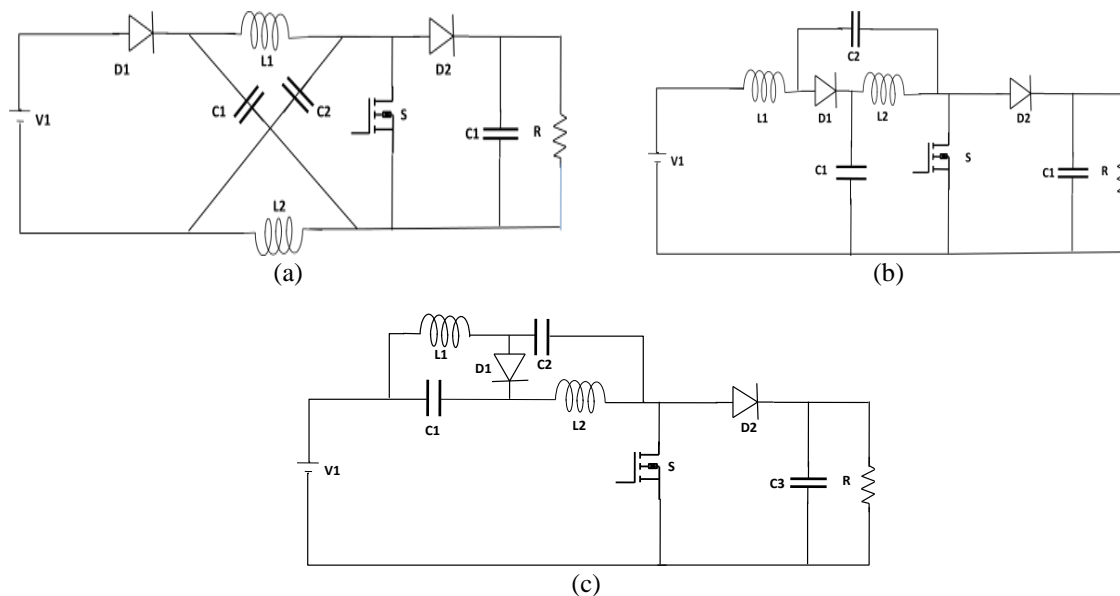


Figure 2. The original Z-source converter of (a) the standard Z-source DC-DC converter, (b) a DC-DC converter with a constant input current that uses a quasi-impedance source, and (c) A DC-DC converter with a changeable input current that uses a standard quasi-impedance source

Figure 3 shows the proposed switched-Z-source dc-ac inverter as an example. The boost factor of the frontend switched-Z-source network is  $1/(1-4D)$ , which allows for a substantial voltage gain with a low

duty cycle. As a result, the backend H-modulation Bridge's index can be tuned to a wider range. As indicated in Figure 3, there are several different types of functioning as:

- Mode 1: during the Shoot-through situation, the output side of the impedance network, i.e. the inverter bridge terminals, is short-circuited by a combination of semiconductor switches ( $S_{21}$ ,  $S_{22}$ ,  $S_{23}$  and  $S_{24}$ ). The input diode  $D_1$  turns off during this time interval, and energy is transmitted from capacitors to inductors [19]–[22]. The stored energy is sent to the load in the inverter's next active switching states, and the input diode conducts.
- Mode 2: the primary circuit alternates between two active and two zero states during the non-shoot-through condition. During this mode the diodes  $D_1$ ,  $D_2$ , and  $D_3$  are reverse biased and switches  $S_{21}$  and  $S_{24}$  can be turned on at same time. The inductors  $L_1$  and  $L_2$  store energy while the capacitors  $C_1$ ,  $C_2$ , and  $C_3$  are discharged, and the energy stored in capacitor  $C_3$  is supplied to the load.

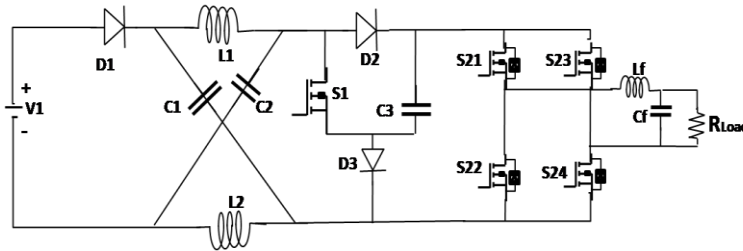


Figure 3. The proposed dc/ac inverter switched impedance source circuit topology

## 2. MODELING THE PV CELL

A photovoltaic (PV) material is one that can convert photon into electrical energy. Electrons can be released from an atom by photons with short wavelengths. On a conductor, electrons can flow and form an electric current. The sun provides the energy required to break the bonds. This is a significant opportunity because the earth's surface receives 6000 times the total daily energy consumption. A PV module can be described using an equivalent circuit that includes a current source, a diode, and a resistor to represent internal resistance. When the sun's rays strike the solar cell, current is generated as:

$$I_{ph} = \left( \frac{I_{sc} + K_i(T - 298) \cdot I_r}{100} \right) \quad (1)$$

Where  $I_{sc}$  = short circuit current,  $K_i$  = temperature constant,  $I_r$  = irradiance, and  $T$  = temperature in Kelvin.

Current flowing through the diode  $I_D$  determines the output current from the solar cell, and current flows to the internal resistance  $I_{sh}$  [2]. The equation then becomes:

$$I = I_{ph} - I_D - I_{sh} \quad (2)$$

In (3), must be used to compute current flows in a diode.

$$I_D = I_s \left[ e^{\frac{q(V + I \cdot R_s)}{NKT}} - 1 \right] \quad (3)$$

Where  $I_0(I_{sat})$  = saturation current,  $V$  = voltage across solar cell,  $R_s$  = series branch resistance,  $K$  = Boltzmann constant,  $q$  = charge of an electron ( $1.602 \times 10^{-19}$  C), and  $N$  = ideality factor (Ideally 1).

From Figure 4, PV module output current and voltage relationship is given by (4).

$$I = I_{ph} - I_s \left[ e^{\frac{q(V + I \cdot R_s)}{NKT}} - 1 \right] - \left( \frac{V + I \cdot R_{se}}{R_{sh}} \right) \quad (4)$$

From (4), the I-V characteristic curve can be obtained which gives operation of the solar panel. At fixed temperature and irradiance, the meeting of the I-V characteristic curve and the load characteristics is the solar panel's operational point. The operative position of the panel goes from zero resistance to infinite resistance, resulting in the appearance of open circuit voltage ( $V_{oc}$ ) [23]–[30].

The multiplication of highest value of the voltage and current gives maximum power. As shown in Figure 5, when the panel voltage reaches voltage at maximum power ( $V_{mpp}$ ), a PV module operates at its maximum power. By modifying the load, the maximum power can be obtained, which will cause the current flowing in the circuit is limited and in addition to the panel voltage.

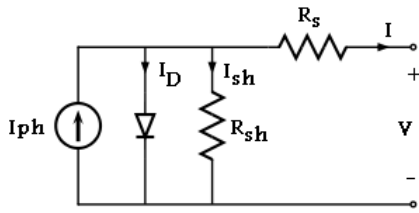


Figure 4. PV cell equivalent circuit

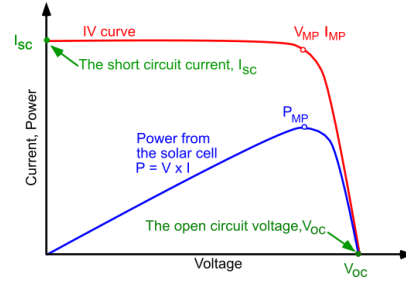


Figure 5. PV module characteristic curve

### 3. WORKING PRINCIPLE AND CIRCUIT TOPOLOGIES OF THE PROPOSED CONVERTERS

The following simulation is mainly focused on first network i.e., switched-ZSC, since the circuit configurations of the proposed three circuits are identical. The following other two SQZSCs can also be analyzed with similar technique. The critical current mode (CRM) is a subset of either the continuous conduction mode (CCM) or the discontinuous conduction mode (DCM). Two cases (Cases 1 and 2) may appear in CCM under differing combinations of inductance, duty cycle, and load resistance, but only in case 3 may appear in Discontinuous Conduction Mode. Throughout a loop, each and every circuit has different state [20], [21]. All of the circuit states are found in the two modes which are depicted in Figures 6(a)-(e) (see Appendix). In Figure 6(a) the reference directions for each variable are shown i) Case 1 - State1  $\rightarrow$  State2, ii) Case 2 - State1  $\rightarrow$  State2  $\rightarrow$  State3, and iii) Case 3 - State1  $\rightarrow$  State2  $\rightarrow$  State3. In this state, the voltages across the three capacitors can be calculated using KVL. State1  $\rightarrow$  State2  $\rightarrow$  State3  $\rightarrow$  State4. For the sake of simplicity, assuming: i) all ideal power components; ii)  $L_1=L_2$  and  $C_1=C_2$  are ignored; and iii)  $L_1=L_2$  and  $C_1=C_2$ . Figure 6(b) represents the current loop corresponding to state1, which indicates current through  $L_1$  &  $C_1$  are equal. Figure 6(c) indicates path of the currents for State2. Figure 6(d) indicates the currents path in state3, further Figure 6(e) represents path of currents corresponding to State4.

### 4. IMPEDANCE NETWORK MATHEMATICAL ANALYSIS

Let us assuming that the capacitors ( $C_1$  &  $C_2$ ) and inductors ( $L_1$  &  $L_2$ ) have identical values. the input voltage is  $V_d$ ; the output voltage  $V_i$ ; series arm inductors  $L_1$  and  $L_2$ ; parallel arm capacitors  $C_1$  and  $C_2$ .

An impedance source inverter equivalent circuit model is derived from Figure 7 in (5)-(15);

$$V_{cap1} = V_{cap2} = V_{cap} \quad (5)$$

$$V_{ind1} = V_{ind2} = V_{ind} \quad (6)$$

$$V_{ind} = V_{cap}, V_D = 2V_{cap} \text{ and } V_I = 0$$

At switching cycle  $T$

$$V_{ind} = V_0 - V_{cap} \quad (7)$$

$$V_D = V_0$$

$$V_I = V_{cap} - V_{ind} = 2V_{cap} - V_0 \quad (8)$$

Where  $T = T_0 + T_1$  and the dc source voltage is  $V$ . The average voltage of the inductors should be zero in steady state after one switching cycle ( $T$ ).

$$V_{ind} = (T_0 \cdot V_{cap} + T_1(V_0 - V_{cap}))/T = 0$$

$$V_{cap}/V_0 = T_1/(T_1 - T_0) \quad (9)$$

Similarly, the Avg DC voltage across the inverter bridge can be determined using (8).

$$\begin{aligned} V_I &= (T_0 \cdot 0 + T_1) \cdot (2V_{cap} - V_0)/T \\ V_I &= (2V_{cap} \cdot T_1/T) - (T_1 V_0/T) \end{aligned} \quad (10)$$

$$2V_{cap} = V_0$$

From (10)  $T_1 * V_0 / (T_1 - T_0) = 2V_{cap} * T_1 / (T_1 - T_0)$

$$V_{cap} = V_0 * T_1 / (T_1 - T_0)$$

The maximum dc-link voltage of the inverter bridge is,

$$V_I = V_{cap} - V_{Ind} = 2V_{cap} - V_0 = T / (T_1 - T_0) * V_0 = B * V_0 \text{ here } B = T / (T_1 - T_0) \text{ i.e.} \quad (11)$$

Boost factor is B, Output peak phase voltage of the inverter is,

$$V_{ac} = M * V_i / 2 \quad (12)$$

Here modulation index is M and source voltage

$$V_{ac} = M * B * V_0 / 2 \quad (13)$$

Before selecting an acceptable buck-Boost factor, the  $V_0$  can be stepped down and up (BB)

$$B.B = B * M \text{ (range from 0 to 1)} \quad (14)$$

The capacitor voltage is

$$V_{cap1} = V_{cap2} = V_{cap} = (1 - T_0/T) * V_0 / (1 - 2T_0/T) \quad (15)$$

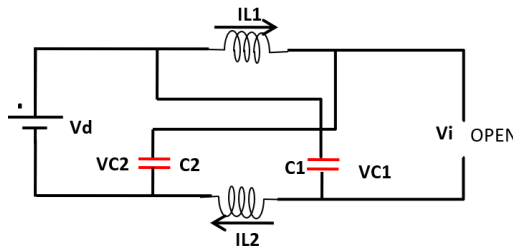


Figure 7. Impedance source inverter equivalent circuit

## 5. EFFECT OF THE PARASITIC PARAMETERS OF THE EFFICIENCY

### 5.1. Power switching loss

Conduction loss and switching loss are two types of losses in power switches. The conducting loss can be measured using Figure 7.

$$P = 8I_L^2 r_s D \quad (16)$$

The power switch loss can be determined by linearizing the voltages and currents of the commutating switches [20], [21] as change their states,

$$P_S = \frac{2 f_s V_0 I_L (t_{on} + t_{off})}{3} \quad (17)$$

The input power can be calculated using (11) as where the switching frequency is  $f_s$  and  $t_{off}$  and  $t_{on}$  are the switch turn-off and turn-on delays.

### 5.2. Diode power loss

Reverse recovery loss and conduction loss are the two forms of diode power losses. Conduction loss is denoted by

$$P_{cond\_D} = 3I_L V_D (1 - D) \quad (18)$$

Diodes reverse recovery loss is given by,

$$P_{RRD} = Q_{RR1}V_{C1}f_s + Q_{RR2}V_{C2}f_s + Q_{RR3}V_{C3}f_s \quad (19)$$

Where  $D_1$ ,  $D_2$  and  $D_3$  diodes and  $Q_{RR1}$ ,  $Q_{RR2}$  and  $Q_{RR3}$  reverse recovery charge of diodes respectively.

### 5.3. Inductor loss

An ideal inductor has zero power loss because it has no resistance and just inductance,  $R = 0$ , and no power is dissipated within the coil. A device that stores energy as an electromagnetic field and measures in henrys is known as an inductor (H). Conduction losses will occur in a practical inductor with internal resistance. So, the conduction loss can be measured, decides the key power loss.

$$P_{Cond L} = 2I_L^2 r_L \quad (20)$$

### 5.4. Capacitor loss

The capacitors total power losses are calculated as,

$$P_{cond C} = I_L^2 r_C (1 - 5D) \quad (21)$$

Then, the derived total conduction losses are

$$P_{cond} = P_{cond S} + P_{cond D} + P_{cond L} + P_{cond C} \quad (22)$$

The input power calculated as,

$$P_i = V_i I_i = V_i I_L \quad (23)$$

Following that, the proposed SZSC efficiency can be determined by using

$$\eta = P_o / P_i = \frac{P_i - P_{cond} - (P_s + P_{RRD})}{P_i} \quad (24)$$

## 6. CONTRASTS WITH PREVIOUS Z-SOURCE TOPOLOGIES

Furthermore, as shown in Table 1, the proposed topology output is differentiated to that of the converters in [17], [22]–[30]. The capacity to boost is a critical metric for assessing the efficiency of a dc-dc converter. When the voltage gain  $G$  is greater than 5, with the same duty ratio the proposed work produces a higher boost factor than the other converters. Although the boost factor is the same as in [17], which is a complicated hybrid three cascade Z-network boost converter. To put it another way, the proposed topology dramatically decreases the no. of passive elements needed to achieve the identical boosting capability. There are two advantages, the first one to decrease the probability of inductive saturation, and the second one to increase the modulation index (MI). As a consequence, when using the two-stage dc-ac conversion, a wider range can be reserved for the MI of the posterior H-bridge. Component numbers are also compared in Table 1 between topologies and the proposed one. The posterior H-bridge is replaced with a diode, output capacitor and switch in each structure to convert it to a dc-dc converter. In comparison to proposed hybrid three-Z-network boost converter, The new one has the identical  $1/(1-4D)$  voltage gain but uses 2 fewer inductors, 4 fewer capacitors, and 1 fewer diode and adding another switch feature increases power density while lowering cost.

When the voltage gain  $G > 5$ , as illustrated in Figure 8, the suggested topology produces a greater boost factor than other converters at the same duty ratio, while the boost factor is the same as in [18], which is a complex hybrid 3-Z-network boost converter. The matlab-simulink detailed specifications are given in Table 2.

Table 1. Current and voltage parameters in Switched-ZSC/SQZSCs

Voltage components				Current components			
Modes	SZSC	CSQZSC	DSQZSC	Modes	SZSC	CSQZSC	DSQZSC
Output voltage ( $V_o$ )	$\frac{1}{1-4D} V_i$	$\frac{1}{1-4D} V_i$	$\frac{1}{1-4D} V_i$	Input current ( $I_i$ )	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$
Voltage on the capacitor C1 ( $V_{C1}$ )	$\frac{1-2D}{1-4D} V_i$	$\frac{1-2D}{1-4D} V_i$	$\frac{2D}{1-4D} V_i$	Current stress of the inductor L1 ( $I_{L1}$ )	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$
Voltage on the capacitor C2 ( $V_{C2}$ )	$\frac{1-2D}{1-4D} V_i$	$\frac{2D}{1-4D} V_i$	$\frac{2D}{1-4D} V_i$	Current stress of the inductor L2 ( $I_{L2}$ )	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$	$\frac{1}{1-4D} I_o$
S1 and S2 switches are under voltage stress ( $V_{s1}$ and $V_{s2}$ )	$\frac{1}{1-4D} V_i$	$\frac{1}{1-4D} V_i$	$\frac{1}{1-4D} V_i$	S1 and S2 switches are under voltage stress ( $V_{s1}$ and $V_{s2}$ )	$\frac{2D}{1-4D} I_o$	$\frac{2D}{1-4D} I_o$	$\frac{2D}{1-4D} I_o$

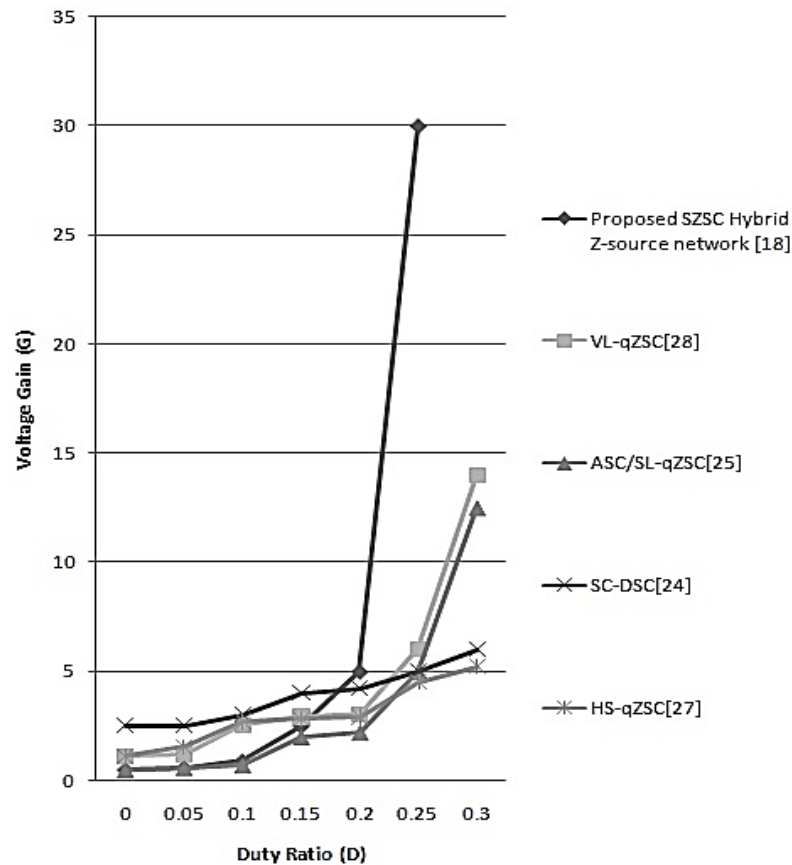


Figure 8. The relationship between variations of voltage gain with respect to variation of duty ratio

Table 2. Simulink specifications

S.NO	Parameters	Value
1	Reference irradiance ( $\text{W/m}^2$ )	1000
2	Reference Temperature( $25+273$ )(K)	298K
3	No. of parallel strings of an array	2
4	No. of series connected module for string	4
5	O.C voltage ( $V_{oc}$ )	68V
6	S.C current ( $I_{sc}$ )	7.5A
7	Switching Frequency( $f_{sw}$ )	25KHZ
8	Inductors ( $L_1=L_2$ )	320 $\mu$ H
9	Capacitors ( $C_1=C_2$ )	340 $\mu$ F
10	Load resistor	100 $\Omega$
11	Output power ( $P_{out}$ )	440.7w

## 7. SIMULATION RESULTS

For 100V dc/ac conversion, a 215 V dc voltage output is used, and voltage input is set by connecting four PV panels in series sequence. The simulation parameters are as follows, based on the previous analyses; i)  $V_i$  is 68 volts; ii)  $f_s$  is 25 kHz; and the service period is 0.2; iii) the evaluate output power is 185 was expected; iv)  $L_1=L_2=320\mu\text{H}$ , with a parasitic resistance of 28-m $\Omega$ ; v)  $C_1=C_2=C_3=330\mu\text{F}$ , with a 10-m $\Omega$  equivalent sequence resistance; vi) Switches  $S_1$  and  $S_2$  have an on-state resistance of 14.5m $\Omega$ ; vii) The diodes  $D_1$ ,  $D_2$ , and  $D_3$  have a forward voltage drop of 1V. Figure 9 show input inductor currents, for one, are simulated waveforms in switched ZSC/switched QZSCs as well as voltage across capacitors 215[V/div] ( $V_{c2}=V_{c4}=215\text{V}$ ).

Figure 10 shows the proposed converter with PV-array is operated at its MPPT under radiation level of 1000  $\text{W/m}^2$ , the voltage at PV-array is 68.4V with respect to time in seconds, Current at PV-array is 7A with respect to time in seconds and the power at PV-array is 478.8W ( $P_{pv}=V_{pv} \cdot I_{pv}$ ) with respect to time. The load draws 440.7W of power with respect to time in seconds, as shown in Figure 11.

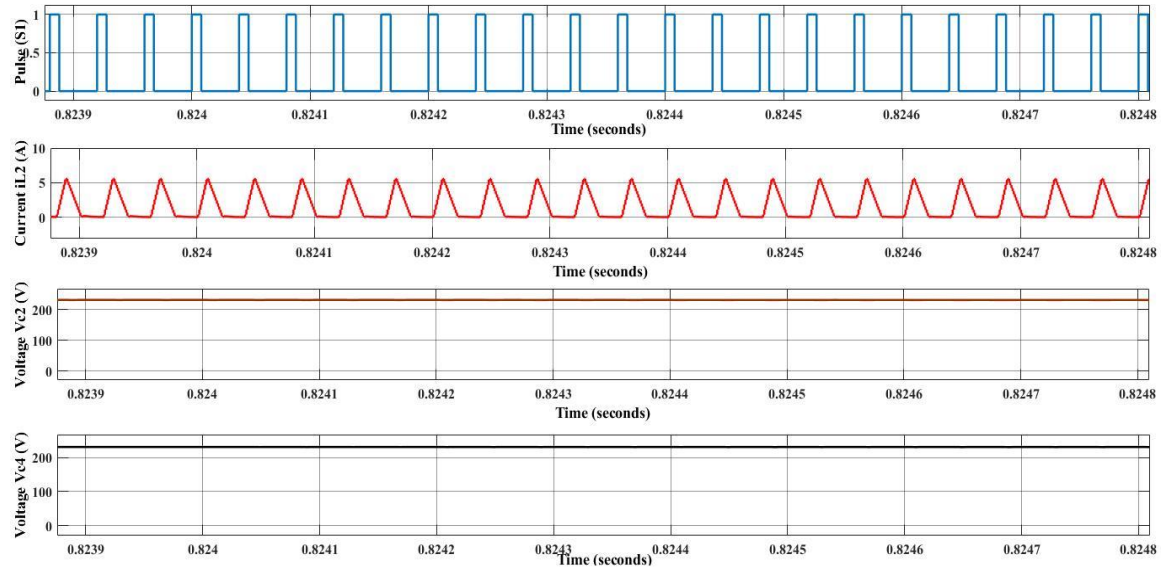


Figure 9. Steady state performance of the proposed SZSC's simulation waveforms at 0.2 duty cycle, gate signal S1,  $i_{L1}$ ,  $v_{C2}$  and  $v_{C4}$  ( $v_{C2}=v_{C4}=215V$ )

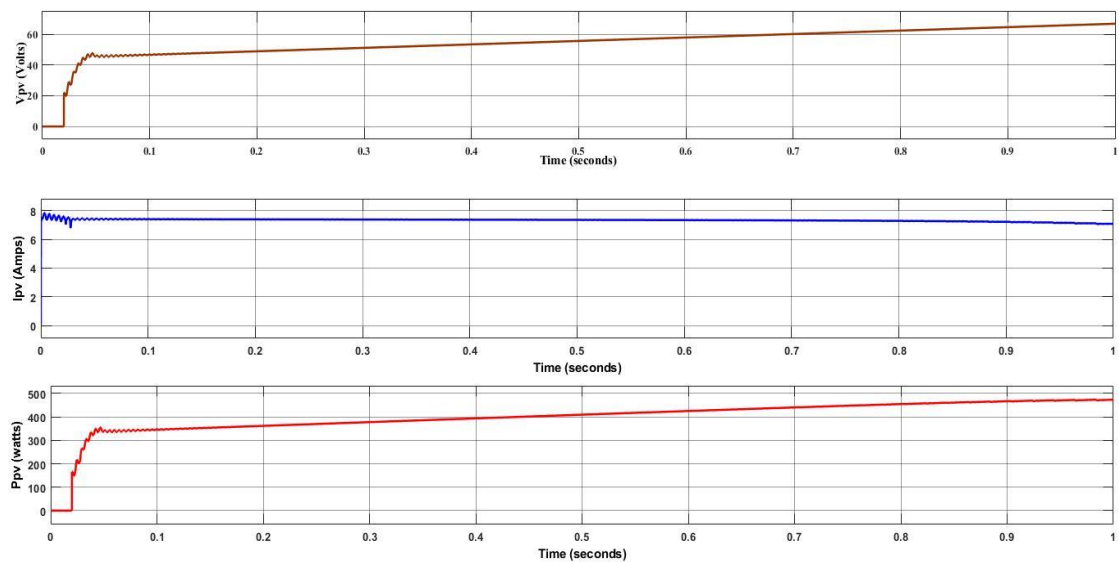


Figure 10. Steady state and starting performance of MPPT-based P&O behavior voltage, current and power

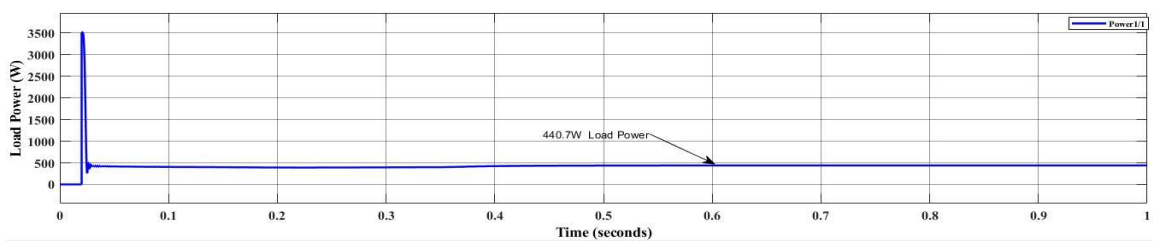


Figure 11. Steady state performance waveforms of load power

Shown in Figure 12(a) shows percentage of battery SOC (%) is 79.99 with respect time in seconds; Figure 12(b) shows the operation of inductor current discharged from 250A to -0.5A flow through it. Figure 12(c) shows voltage across inductor 52V with respect to time in seconds.



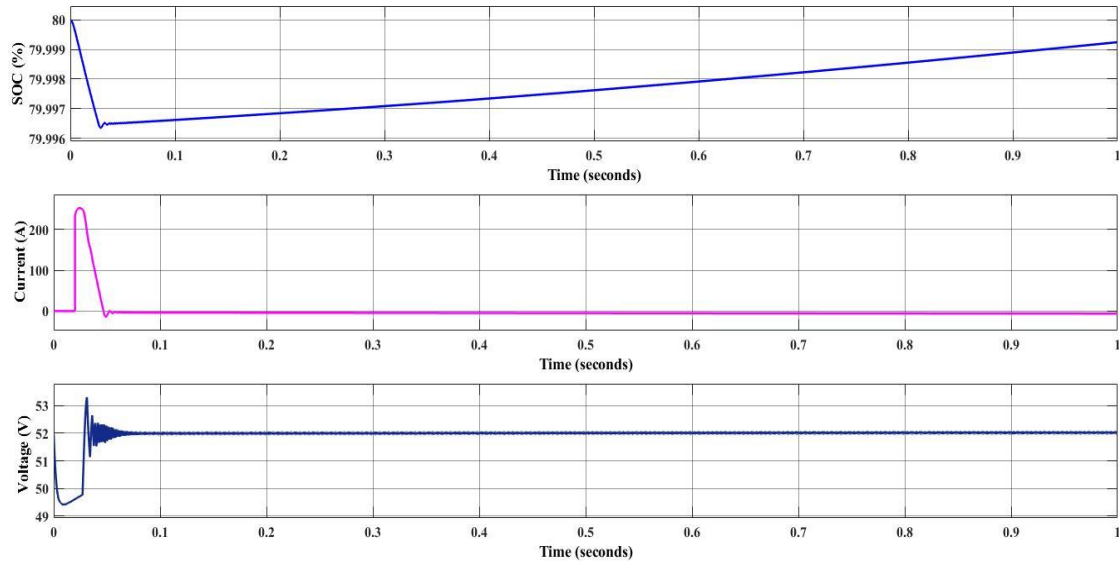


Figure 12. Steady state waveforms of (a) battery SOC (%), (b) battery current, and (c) battery voltage

## 8. CONCLUSION

It is suggested that a series of switched impedance source/switched quasi-ZSCs with modified topology be developed for Photovoltaic systems. By putting an extra switch and diode to ordinary ZS/qZS DC-DC converter s, the increased boost factor up to  $1/(1-4D)$ . To achieve higher voltage gain while avoiding the instability induced by inductor saturation, a short duty cycle is used. The boost ratio of the proposed converters is the same as the hybrid three Z-network boost converters. That were recently proposed, but with fewer passive components, allowing for higher power density and lower unit costs. The operating principles of these devices are detailed in this paper, as are the parameters of current and voltage, as well as conversion efficiency of the parasitic parameters the effects. Eventually, results of the simulation provided to support the properties and theoretical analysis previously mentioned.

## APPENDIX

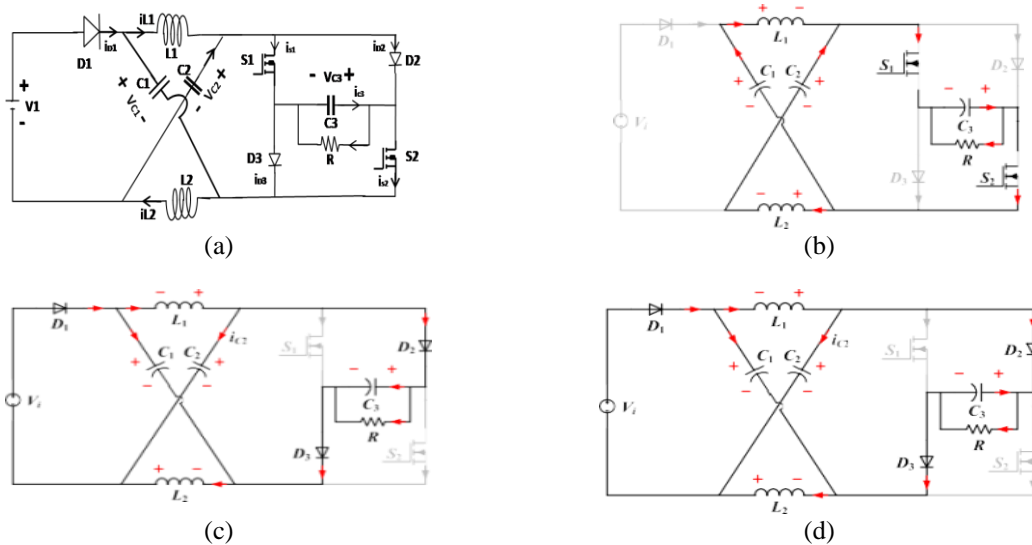


Figure 6. Operating states of SZSC; (a) specifications of reference directions, (b) current loop of the proposed SZSC in State1:  $S_1$  and  $S_2$  on;  $D_1$ ,  $D_2$  and  $D_3$  off, (c) current loop of the proposed SZSC in State2:  $D_1$ ,  $D_2$  and  $D_3$  on;  $S_1$  and  $S_2$  off, and (d) current loop of the proposed SZSC in State3:  $D_1$ ,  $D_2$  and  $D_3$  on;  $S_1$  and  $S_2$  off

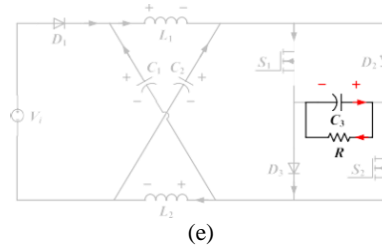


Figure 6. Operating states of SZSC; (e) the proposed SZSC's current loop in State 4 is as:  $S_1$ ,  $S_2$ ,  $D_1$ ,  $D_2$ , and  $D_3$  are all turned off (continue)





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