Analysis of single switch step up DC-DC converter with switched inductor-switched capacitor cells for PV system

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ABSTRACT

The presented work exhibits high gain and increased efficiency for DC-DC converter. Additionally, this topology significantly improves the voltage conversion ratio when compared with other DC-DC converters reported recently. The non-existence of high frequency transformer ensures compactness and low cost and henceforth, it is apt for clean energy applications. The analysis of the high gain converter in steady state is carried out in continuous conduction mode (CCM). Initially, the proposed converter performance is analyzed using MATLAB/Simulink platform and prototype of the same with a power rating of 200 V, 100 W is built and tested. The reliability and robustness of the converter is perceived from the experimental results and peak efficiency achieved is around 93%.

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1. INTRODUCTION

The importance of renewable resources in distribution system increases rapidly due to the diminution of conventional energy resources. Renewable sources such as photo voltaic (PV) cells, fuel cells and provide low DC voltage. DC microgrid applications require a DC-DC converter with high gain to transform this low DC voltage into high value. There are a number of literature references that describe high gain DC-DC converters, both isolated and non-isolated. A converter with voltage lift technique is presented in [1]. It is suggested to attain high voltage gain by a hybrid approach where both switches are switched on simultaneously. Though this topology offers more benefits its application restricted only for low voltage. A novel high gain converter that involves switched inductor (SL) for boosting applications is proposed in [2]. By utilizing fewer components and the two switches in the circuit topology renders high voltage gain with small value of duty cycle but imparts high voltage stress.

The concept of the switched capacitor (SC) is introduced in [3]. The primary merits of the SC converter are the continuous input current, high voltage gain with minimal voltage and current stress and, absence of high frequency-transformer. More number of boosting cells is needed to get high gain thereby, circuit becomes bulkier. A converter with switched capacitance technique is presented in [4]. It is possible for the converter to achieve a high gain in voltage with less duty ratio. Though one switch is adopted, the voltage gain is comparatively low. A switched inductor-capacitor divided network converter attains high gain with a single switch [5]. There is a low voltage across the switches compared to output voltage but more number of diodes contributes more conduction losses.

DC-DC switch-mode boost converters operate with switched capacitor voltage multipliers [6], achieving four times higher voltage gains, with only half the voltage stress on the transistor and diodes. A review on certain topological evolution in boost converters using switching capacitors is described in [7]. The common ground feature with topological evolution on a SC with a double-switch configuration is also highlighted. Additionally, four enhanced voltage gain boost topologies are described along with its downsides. A new technique using two DC-DC converter with different connection, where the output voltages are either positive or negative is proposed in [8]. However, voltage lifting strategies are based totally on boosting gain cells to improve the gain further. It instigates more control complexities. Based on traditional CUK and SEPIC converters, a new dual-output converter is introduced in [9]. Due to the fact that transformers increase output, the volume and price will increase as well as losses. It uses low value of inductor and capacitor.

To enhance static gain with lower switch stress, voltage multiplier technique is employed for typical non-isolated DC-DC converters. A unique step-up DC-DC converter that has combined SL, SC and voltage multiplier cell is introduced in [10]. Numerous high gain DC-DC converters that employ SL and SC structure are available in literature [11]–[16]. However, proposed converter has more gain compared to these converters. A switched inductor coupled with voltage multiplier based high gain topology for renewable applications is addressed in [17]. Also, SEPIC topology based on Quazi-Z source structure with SC cell operated in boost mode for electric vehicle application is reported in [18]. A DC-DC converter with active switched LC network that extracts maximum power from solar by utilizing fuzzy controller type MPPT is described in [19]. A high step up converter with SC structure suitable for solar PV applications is presented in [20]. Unlike fossil fuels, renewable energy sources produce intermittent power. Using step-up DC-DC power converters, energy flow can be controlled efficiently with single stage power conversion [21]. A high gain non isolated bidirectional DC-DC converter suitable for PV systems is presented in [22] and it provides improved dynamic response. PV systems are particularly sensitive to power consumption and require significant boost in performance to achieve higher power and efficiency. A SEPIC converter with PV as input source is presented in [23]. This converter exhibits high gain with minimal duty cycle. A DC-DC converter with SL, SC, and voltage multiplier structure is analyzed and outcomes are presented in [24]. A high conversion ratio DC-DC converter which incorporates a SEPIC converter and voltage multiplier cell is presented in [25].

In the presented converter, the gain is 27 for a duty ratio of 0.8. The paper organization is as below. In section 2, we examine the operational modes of the converter, and in section 3, we discuss its design procedure. Section 4 presents simulation results, followed by section 5 with experimental results. In section 6, we conclude our discussion.

2. DESCRIPTION AND OPERATION PRINCIPLE OF THE CIRCUIT

The suggested SL-SC DC-DC converter is portrayed in Figure 1(a). As shown, the converter circuit contains an input DC supply and includes a SL-SC structure.

– Mode 1

Figure 1(b) shows the mode 1 operation. Upon turning on the MOSFETs, the diode D1 and D3 begin to conduct due to the forward bias of the diode. Thus, current I_{L1} and I_{L2} flow linearly through the inductors L_1 and L_2, thus storing energy. Diodes D2 and D3 are off in this mode. The capacitors C_1, C_2, and C_3 are discharged.

$$V_{in} = V_{L1} = V_{L2} \tag{1}$$

$$V_{C1} + V_{C2} = V_{C5} \tag{2}$$

$$V_{C4} + V_{C5} = V_0 \tag{3}$$

$$V_{C1} + V_{C2} + V_{C3} = V_{C4} + V_{C5} \tag{4}$$

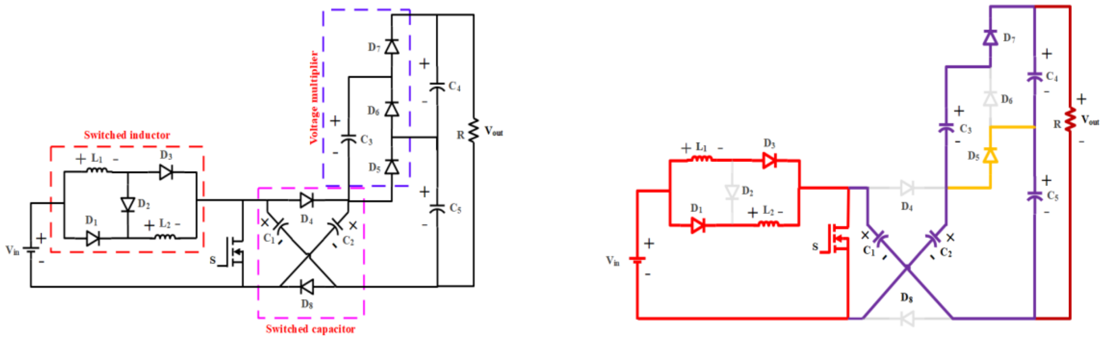
– Mode 2

Figure 2(a) exhibits the mode 2 operation. The MOSFET S is turned OFF, and diode D2 conducts. Through the inductors L_1 and L_2, current flows linearly. Diodes D_1 and D_3 do not conduct in this duration. Figure 2(b) depicts the working of each and every device in the presented circuit.

$$V_{in} - V_{L1} - V_{L2} - V_{C1} = 0 \tag{5}$$

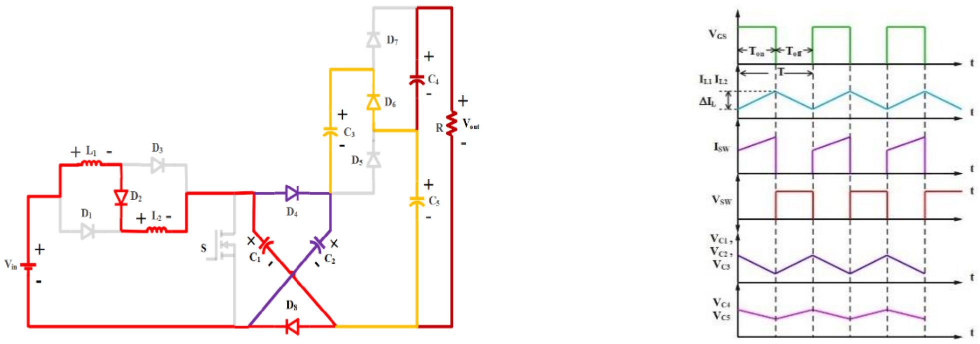
$$V_{in} - V_{L1} - V_{L2} - V_{C2} = 0 \tag{6}$$

$$V_{in} - V_{L1} - V_{L2} - V_{C2} + V_{C5} - V_{C3} - V_{C1} = 0 \quad (7)$$



(a) (b)

Figure 1. Circuit diagram (a) proposed SL-SC converter and (b) S on



(a) (b)

Figure 2. The operating mode of suggested converter: (a) S off and (b) switching waveforms

3. DESIGN PROCEDURE

From in (5) and $V_{L1} = V_{L2}$, $V_{C5} = V_{C1}$

$$V_{L1} = V_{in} - V_{L1} - V_{C1}$$

$$V_{C1} = \left(\frac{1+D}{1-D}\right) \cdot V_{in} \quad (8)$$

From in (7), we have:

$$V_{in} - V_{L1} - V_{L1} - V_{C2} + V_{C5} - V_{C3} - V_{C1} = 0$$

$$V_{C1} + V_{C5} - V_{C4} = 0 \quad (9)$$

$$V_0 = V_{C1} + 2V_{C5} \quad (10)$$

$$V_{C1} = \frac{V_0}{3} \quad (11)$$

From in (8) and (11), we have:

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{3(1+D)}{1-D} \quad (12)$$

– Inductor selection

The current ripple through an inductor determines the choice of an inductor:

$$V_L = L\frac{di}{dt} = V_{in} \quad (13)$$

The (13) can be rewritten as (14).

$$V_L = L\frac{\Delta i}{\Delta t} = V_{in} \quad (14)$$

The inductor ripple is calculated as (15).

$$L = \frac{DV_{in}}{\Delta I_L f_s} \quad (15)$$

– Capacitor selection

In mode 2, capacitor current calculated as (16):

$$I_{C3} = C_3 \cdot \frac{dv}{dt} = I_0 \quad (16)$$

Where the variation of the capacitor voltage, the (16) is can be rewritten as (17).

$$I_{C3} = C_3\frac{\Delta V_C}{\Delta t} = I_0 \quad (17)$$

From (17), we obtain:

$$C = \frac{3(1+D)}{\Delta V_C R f_s} \quad (18)$$

where ΔV_C is the capacitor voltage ripple. The capacitance is selected as (19).

$$C = C_1 = C_2 = C_3 = C_4 = 0.5C_5 \quad (19)$$

The converter component ratings are mentioned is enlisted in Table 1. An experimental prototype was built to verify the theoretical analysis and the boosting capability of the proposed converter. The parameter for experiment is shown in Table 2.

Table 1. Design specification of the proposed converter

Parameter		Value	Parameter		Value
Supply voltage	V_{in}	25 V	Load resistance	R_L	400 Ω
Inductor	L_1, L_2	0.4 mH	Switching frequency	f_s	20 kHz
Capacitor	C_1, C_2, C_3, C_4	50 μF	Load current	I_0	0.5 A
Output capacitor	C_5	100 μF	Output power	P_0	200 W
Output voltage	V_0	200 V			

Table 2. Component specification for the proposed hardware setup

Components		Specification
Inductor	L_1, L_2	0.4 mH, 20 A
Capacitor	C_1, C_2, C_3, C_4	47 μF, 100 V
Output capacitor	C_5	100 μF, 120 V
Load resistance	R_L	400 Ω
Power MOSFET	S	IRFP150N
Power diode	$D_1 - D_8$	MUR3020PT

4. SIMULATION RESULT

Below is a description of the simulation results, which verifies the performance of this DC-DC converter model. Figure 3 shows the input DC supply of 25 V and Figure 4 shows input current. The DC output voltage rise from 0 V and attains constant value 185 V and is shown in Figure 5. Figure 6 depicts output current. Figure 7 depicts the different waveform of gate pulse, inductor current, capacitor voltage and diode voltage. Figures 8 and 9 show load versus efficiency and source voltage versus efficiency curve of proposed converter. The output voltage is maintained at 200 V and the efficiency is also above 90%. Figure 10 shows the sudden load changes of output voltage waveform. The output voltage of 200 V is regulated when the load is changed during the time period of 0.6 s and 1.2 s. Figure 11 shows the output current waveform of sudden load changes. The output current of 0.5 A is regulated even when the load is changed during the time period of 0.6 s and 1.2 s.

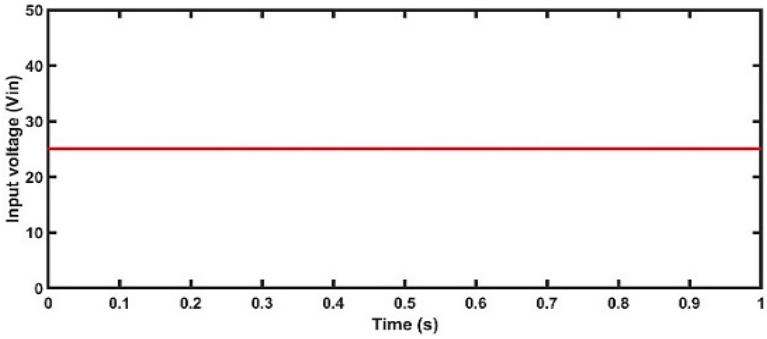


Figure 3. Converter Input DC voltage

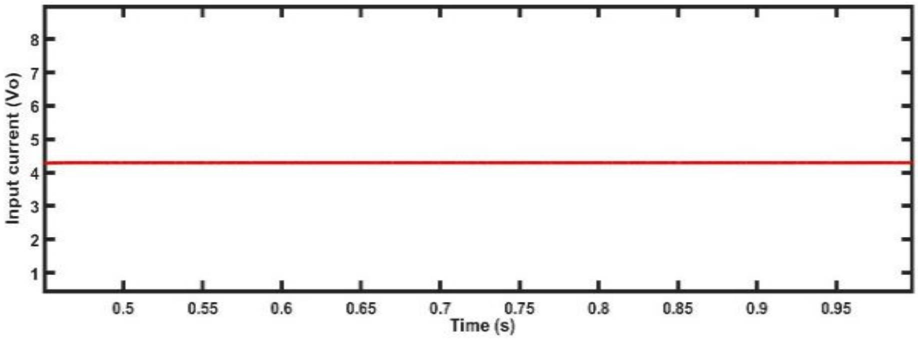


Figure 4. Converter Input DC current

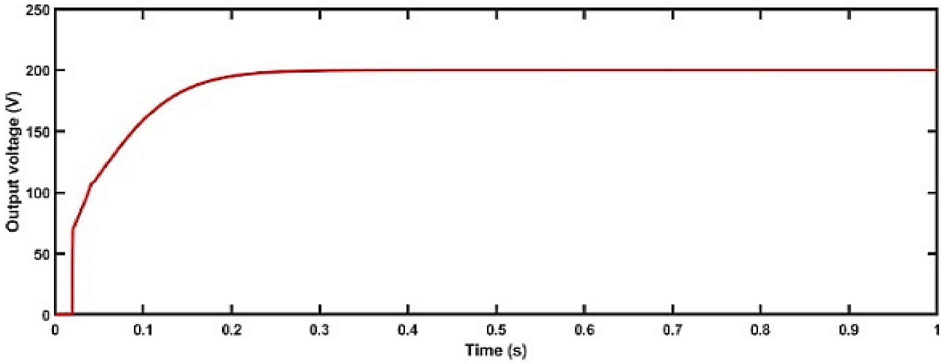


Figure 5. Converter DC output voltage

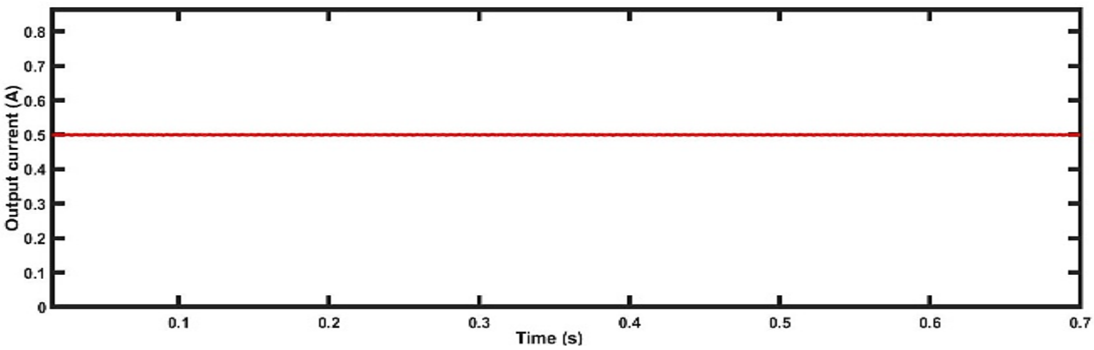


Figure 6. Converter DC output current

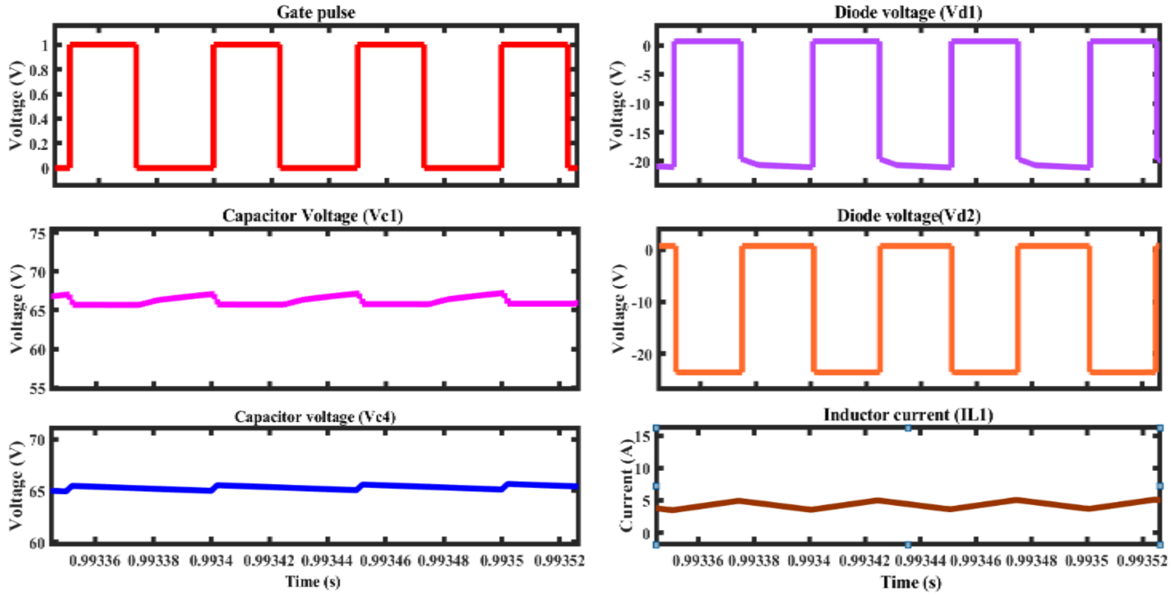


Figure 7. Gate pulse, capacitor voltage, inductor current, and diode voltage waveform

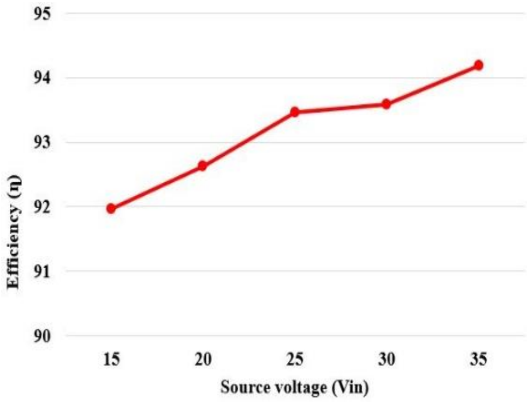


Figure 8. Load (%) (vs) efficiency curve

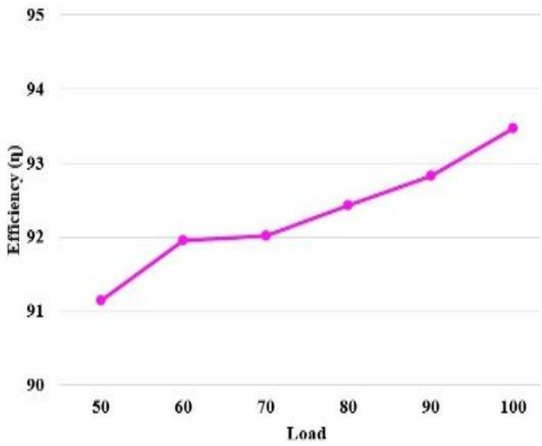


Figure 9. Comparative analysis of source variation (vs) efficiency

A switch voltage stress chart is shown in Figure 12 for the proposed converter and other related converters. From figure it can be inferred that the suggested topology has lower switch voltage stress than all other topologies for duty cycle 0<d<0.8. A duty cycle chart for the suggested converter and other relevant converters is illustrated in Figure 13. As can be seen, suggested topology has higher gain in voltage than other topologies for 0<d<0.8.

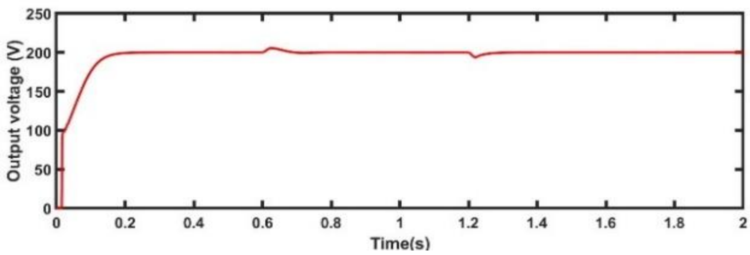


Figure 10. Output voltage waveform of sudden load change

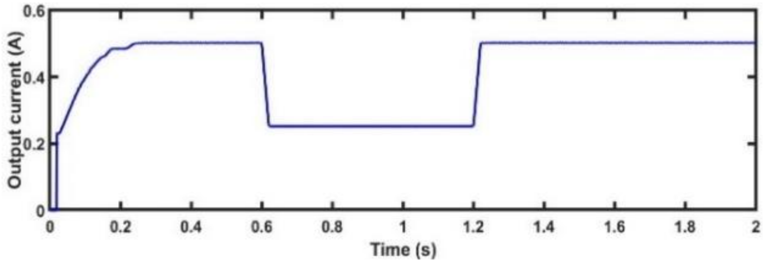


Figure 11. Output current waveform of sudden load change

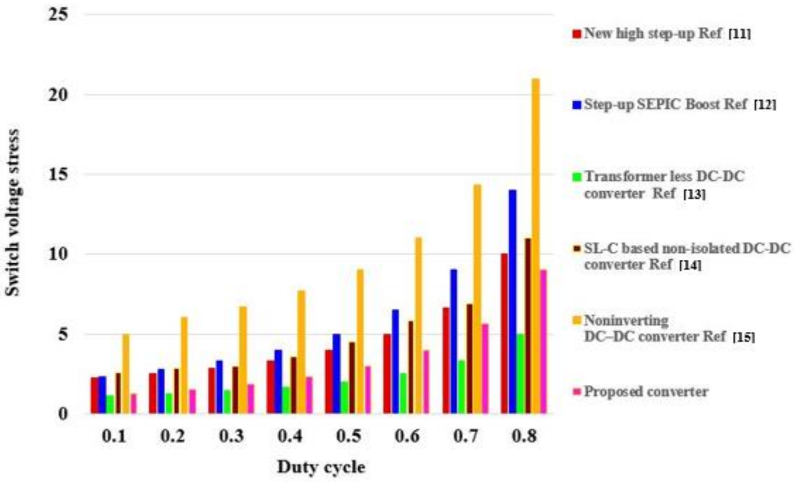


Figure 12. Comparative analysis of switch voltage stress (vs) duty cycle

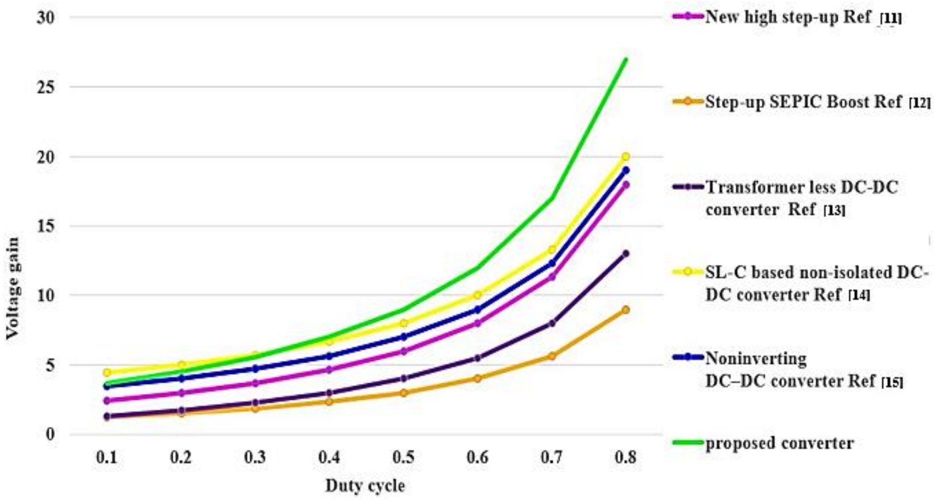


Figure 13. Comparative analysis of voltage gain (vs) duty cycle

5. EXPERIMENTAL RESULT OF THE PROPOSED CONVERTER

Through such a number of stages, the general description of the suggested converter's hardware design is established. The converter prototype was designed using a variety of parameters. Some parameters are involved in achieving the optimal result. The value of elements that were used to make the converter has been shown in Table 2. Figure 14 shows experimental setup that includes RPS, rheostat, converter, and gate driver circuit. Figures 15 portray the gate pulse obtained.

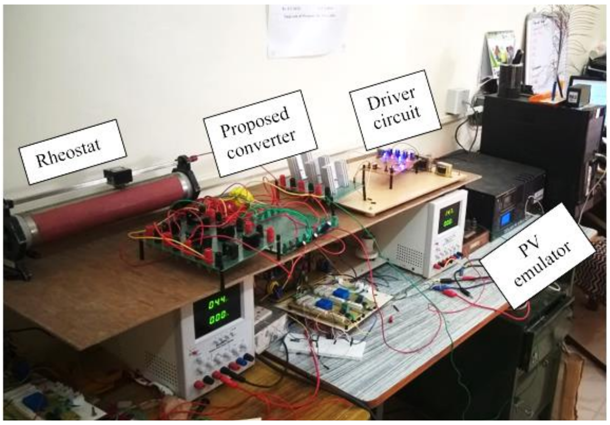


Figure 14. Photograph of the proposed topology using PV emulator

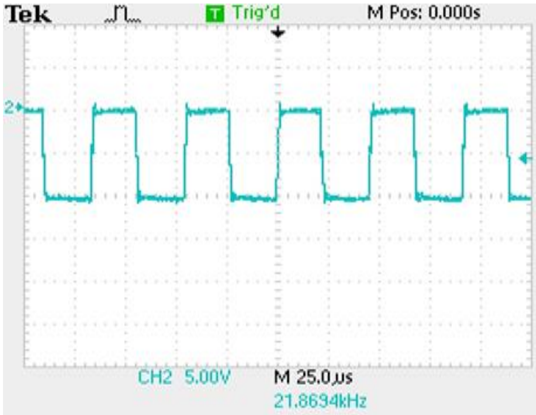


Figure 15. Gating pulse for the switch

Table 3 compares the suggested converter with other comparable converters presented in topologies [11]–[16] with reference to the components count, power switch voltage stress, and the voltage gain. When compared with topologies [11], [6], this converter attain s a higher voltage gain. There is only one power switch in each of the converters presented in [11] and [14]. Nevertheless, the voltage gain is lower and switch voltage stress is more compared to proposed converter. As compared with the proposed converter, there are more inductors used in the converters [15] and [16]. Furthermore, they have less voltage gain and a higher switch voltage stress compared to the converter that has been proposed.

Table 3. Comparative analysis of the proposed converter with competitive topologies

Converters		New high step-up [11]	Step-up SEPIC boost [12]	Transformer less DC-DC converter [13]	SL-C based non-isolated DC-DC converter [14]	DC-DC non isolated converter [15]	Noninverting DC-DC converter [16]	Proposed converter
Number of components	C	4	4	5	4	5	3	5
	D_i	4	5	3	6	5	5	8
	S	1	2	1	1	3	2	1
	L	3	2	3	2	4	4	2
Total no. of components		12	13	12	13	18	14	16
Voltage gain (G)		$\frac{2(1+D)}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+2D}{1-D}$	$\frac{4}{1-D}$	$\frac{5-D}{1-D}$	$\frac{3+D}{1-D}$	$\frac{3(1+D)}{1-D}$
Switch voltage stress (S1)		$\frac{2V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{2V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{2V_{in}}{1-D}$	$\frac{(1+D)V_{in}}{1-D}$
Switch voltage stress (S2)		--	$\frac{(1+D)V_{in}}{1-D}$	--	--	$\frac{V_{in}}{1-D}$	$\frac{2V_{in}}{1-D}$	
Switch voltage stress (S3)		--	--	--	--	$\frac{V_{in}}{1-D}$	--	--
Switch voltage stress (S4)		--	--	--	--	$\frac{V_{in}}{1-D}$	--	--
L.I.C.R		Yes	No	Yes	Yes	No	Yes	Yes
Switching frequency		33 kHz	100 kHz	100 kHz	40 kHz	40 kHz	33 kHz	22 kHz
Common ground		Yes	Yes	Yes	Yes	No	No	yes

Notes: C: capacitor, Di: diode, S: switch, L: inductor, L.I.C.R: low input current ripple

Figure 16 exhibits the experimental results of the SL-SC converter in CCM when V_{in}= 24 V. The gate pulse and output voltage are displayed in Figure 16(a), Figure 16(b) portrays the current waveform of the $L_1$and L_2. The experimental waveform of each inductor closely matches with the analytical waveform, which is illustrated in Figure 8. Figure 16(c) and Figure 16(d) indicate the voltage waveform capture from the diodes D_1-D_8. There is a comparison between the proposed structure and other structures and is based on their switch voltage stress, boosting capacity and the number of components and is shown in Table 3.

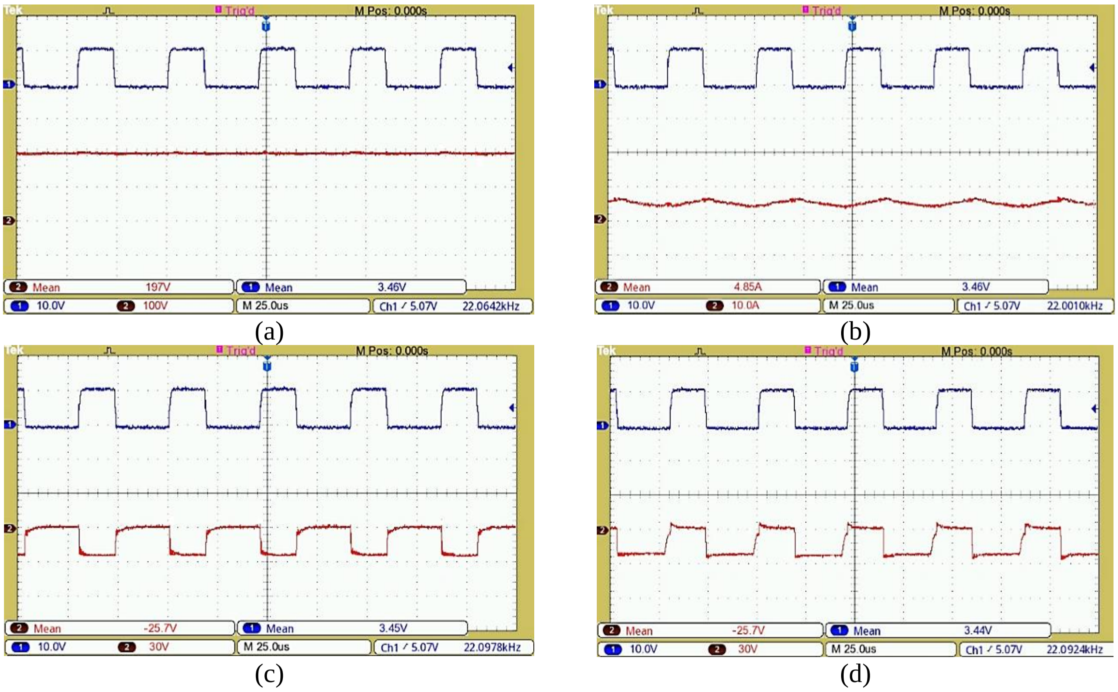


Figure 16. Hardware waveform of proposed converter (a) output voltage, (b) inductor current (I_{L1}, I_{L2}), (c) diode voltage (D_2, D_4, D_6, D_8), and (d) diode voltage (D_1, D_3, D_5, D_7)

6. CONCLUSION

The paper presents a non-isolated DC-DC converter. With the proposed structure, high voltage gain can be achieved, and voltage stress can be maintained at minimal value. The voltage conversion ratio is further improved by adding a voltage multiplier circuit. The detailed operating mode for CCM are studied with the help of practical design. Based on the experimental results, the presented converter has a 93% efficiency and well-regulated output voltage. From the comparison results it can be seen that the converter exhibits low voltage stress across the components. The integration and implementation of the closed loop control of the proposed converter with the renewable energy system is the future task.

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