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Bidirectional controller supported inductively coupled dual buck converter based DSTATCOM with passive filter for PQ improvement

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ABSTRACT

This research paper explains about the bidirectional controller (BC) supported inductively coupled dual buck converter (IC-DBC) based distributed static compensator (DSTATCOM) with passive filter (PF) for 3-ϕ 3-wire (3P3W) power distribution system (PDS). The most significant concern in the PDS is power quality (PQ) control. Hence, innovative approach is proposed by considering concept and benefits of BC, inductive coupled filtering transformer (IFCT), passive filter and dual buck converter. Equivalent circuit for IC-DBC based DSTATCOM is realized in view of impedance of transformer and direct coupled dual buck converter (DC-DBC) based DSTATCOM to disclose the filtering mechanism. The supremacy of the proposed DSTATCOM is introduced by comparing its simulation outcomes with DC-DBC based DSTATCOM and IC-DBC based DSTATCOM in terms of better harmonics curtailment, power factor advancement, load balancing & reduced DC link voltage compared to other approaches as per IEEE standard.

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1. INTRODUCTION

In today's age, shunt compensation is gratifying the power quality (PQ) shrinkage issue in power distribution system (PDS). Due to the propagation of electronic equipment, there will be deterioration of the PQ in the PDS. Several problems such as short circuit current flow, currents distortion, poor protection, thermal losses, over current losses, voltage collapse, inefficient filtering are occurred because of harmonic current flow in a circuit which resuits in the malfuncting at user end [1], [2]. Root source of these malfunctions are unceasingly accumulative use of several kinds of loads which are non-linear in nature like adaptable speed drives, rectifiers, switch mode power supplies, solid state voltage controllers and electronics equipment such as mobile phones, lap-tops, desktop computers, servers, and battery chargers. Complications initiated by PQ issues have severe financial impact on PDS as well as consumers. To overcome such technical hitches due to unexpected load variant, the use of directly coupled (DC), inductively coupled (IC), bidirectional controlled (BC) supported directly coupled-distributed static compensator (DC-DSTATCOM) with passive filter (PF) are superior [3], [4]. In the recent development, the planned fusion structure like BC supported IC-DSTATCOM with PF plays an vital role in industrial solicitations. The design features and its novelty centred significance are aimed to appeal the scholars, inventers and designers for the forthcoming devices due to the benefit of better shunt compensation in addition with flexible protection against harmonics over current with comparable minimal expenses.

Numerous researchers across the globe are building an effort to invent the various control techniques and optimization methods for enhancing the PQ. Usually, for mitigation of PQ related issues, DSTATCOM is favored as current allied trustworthy d-FACTS device [5], [6]. An effective harmonics curtailment enables DSTATCOM to emerge as one of the superior custom power devices in power distribution system (PDS) [7]. So, keeping design consideration for different power levels, numerous topologies such as 3-leg parallel, 3-leg modular and 2-leg modular [8] and 3 leg and 4 leg voltage source converter (VSC)-based [9] DSTATCOM was adopted. Literature review depicts that working of DSTATCOM not only depends on topology but also on the control algorithm. Thus, algorithms for instance synchronous reference frame (SRF) theory [10], [11]. Adaptive least-mean-square (ALMS) control algorithm [12], instantaneous reactive power (IRP) theory [13], *icosϕ* control technique [14]–[16], Kernel Hebbian least mean square [17], adaptive neuro-fuzzy inference system LMS algorithm [18] are considered.

In this proposed work, *icosϕ* control algorithm, is chosen because it can control real and reactive power. The planned system is implemented for harmonic curtailment in balanced condition. The prime benefits of DC-DSTATCOM: i) It can curtail harmonics and enhance PQ; ii) Non-usage of expensive coupling equipments results in less economics; iii) DC-DSTATCOM performs low frequency operation; iv) The direct coupled element provide excellent frequency response; and v) The circuit is very simple due to absence of additional component. But in DC-DSTATCOM, because of the direct contact between source, DSTATCOM and load, numerous difficulties have been retain which results in short circuit current flow, reduced protection, certain thermal losses, over current, inefficient filtering.

Owing to such type of shortcomings of DC-DSTATCOM, at present time the advancement was initiated in IC-DSATCOM which is achived by involving a coupling transformer between the source and non-linear loads. It results in numerous advantages such as increase in the compensation capability, a reduced amount of switching stress, controllability, flexibility, and upgraded voltage balancing at point of common coupling (PCC). Generally, 3 leg voltage source converter (VSC) topology is adopted in designing DSTATCOM [19], [20]. In such circumstance, star/delta transformer having rating of kilovolt ampere (KVA) with required injection of reactive power is essential. On the other hand, inductive transformer isolates device as well as system besides the desired application. However, with a use of various transformers, this sort of DSTATCOM can be designed in a numerous ways.

Suggested system offers flexibility for auxiliary enhancement by associating further converters and loads. In order to improve compensation and stability of inductively filtering converter transformer (IFCT), design scheme for impedance-match between DSTATCOM and converting transformer is briefly potryed [21], [22]. Power systems designers are under persistent burden to advance PQ, reliability and operating efficiency with an economical constraints [23], [24]. As, AC power can't be stored, only DC power can be stored. Hence, AC power needs to convert it into D.C. power so as to store electrical energy. Basically, in bidirectional controller, flow of power is not only from source to load but it also allows flow of power from load to source if required. Bidirectional controller can work in both modes, i.e. manage the flow of power in both the direction between source and load. Hence, generated excess reactive energy can be stored in DC capacitors [25]. So, in this way reactive power compensation can be easily obtained. Though inclusion of buck converter results in advancement of cost content, increased number of switches reduces the overvoltage stress on it which results in realibility improvement, over voltage protection, reduced heating losses. Ultimately, security and stability consideration dominates cost content. But, with the reference of active tuning control, BC topology is included with DSTATCOM for the purpose of flexible protection for harmonics over current. Including these, PF is served for specific reactive power compensation.

The analysis results prove that the higher order harmonics current flowing from the compensator is reduced due to the BC and PF. Thus, protecting the compensator against harmonic over current can be achieved. Some of the applications of the proposed DSTATCOM include ship power system, smart grid, AC-DC grid integration, micro grid, renewable energy grid, and electric vehicle.

The technique for filtering is designed using the comprehensive mathematical method with the help of *icosØ* algorithm in MATLAB. The following observations are inferenced from proposed BC supported inductively coupled dual buck converter (IC-DBC) based DSTATCOM with PF scheme in accordance with the standard value of IEEE-2030-7-2017 and IEC-61000-1 grid code.

- Capable of providing flexible protection against over current harmonics.
- Foremost aspects of the presented algorithm are enhanced tracking, adaptive and compensation capabilities.
- Better convergence performance is achieved.
- Numerous PQ solutions for instance curtailment in harmonics, power factor modification, superior voltage regulation, balancing of load and reduced DC-link voltage of IC-DSTATCOM will be achieved with the proposed scheme.
- The present algorithm can be reframed in future by restructuring the pamameters.

The structure of present paper is a transitory indication of research history and inspiration is presented in section 1. A brief review related with circuit configuration as well as modelling of the DC-DBC based DSTATCOM, IC-DBC based DSTATCOM and BC supported IC-DBC based DSTATCOM with PF is dipected in section 2. In a section 3, the modelling as well as design of inductive transformer, PF and BC are investigated. In a section 4, thorough implementation of *icosϕ* control algorithm under various situations is potrayed. For verifying the effectiveness of proposed topology, simulation outcomes are offered in section 5. At last in section 6, our research efforts are concluded.

2. MODELLING OF PROPOSED DUAL VOLTAGE SOURCE INVERTER (DVSI) AND CONVENTIONAL VSI

Circuit for 3P3W PDS with DC-DBC based DSTATCOM and IC-DBC based DSTATCOM are presented in Figures 1 and 2 individually. Balanced sinusoidal 3-ϕ power supply, DSTATCOM, 3-ϕ load non-linear in nature (resistive and inductive loading with uncontrolled rectifier) constitutes the DC-DBC based DSTATCOM. The IC-DBC based DSTATCOM comprises of balanced sinusoidal 3-ϕ power supply, DSTATCOM, converter transformer, non-linear natured 3-ϕ load. The BC supported IC-DBC based DSTATCOM with PF joined at PCC of PDS for shrinking of the PQ issues and harmonics over current is presented in Figure 3. Insulated gate bipolar transistors (IGBTs) switching pulses of all 3 compensators are produced by utilising the *icosϕ* control technique. The purpose of the present research work is to obtain the unswerving structure by means of *icosϕ* control algorithm.

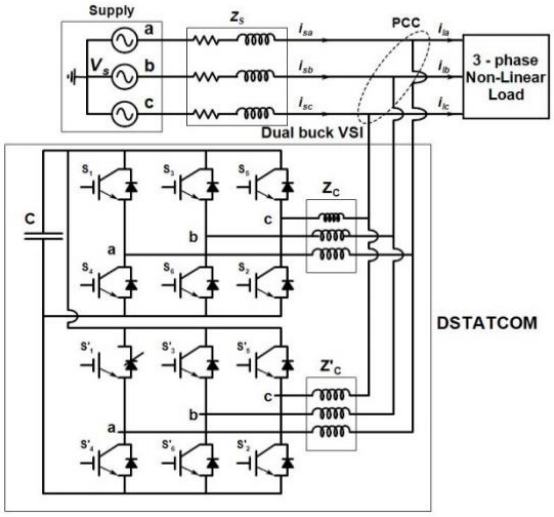


Figure 1. PDS with DC-DBC based DSTATCOM

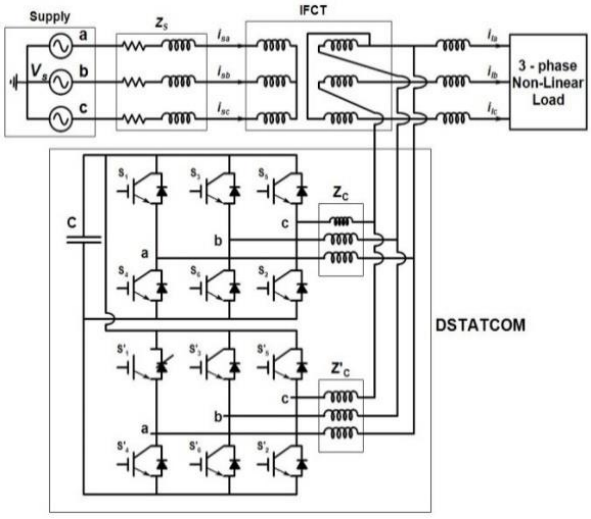


Figure 2. PDS with IC-DBC based DSTATOM

2.1. Freshness of planned topology

Numerous freshness of presented topology over DC-DBC based DSTATCOM are lightened as follows:

- Reduced supply side current THD: the % THD for source side as well as load side current are obtained as 4.51% and 27.9% correspondingly for single VSI based DSTATCOM. However, % THD for source side as well as load side current are gained as 4.14% and 27.90% correspondingly for DVSI based DSTATCOM.
- Reduced system down time cost: total load current is reliant on converter transformer plus VSC interfacing impedance, which declines the failure rate of IGBT. So, plummeting in system down time-cost results in raise of PDS reliability.
- Reduced DC-link voltage: in DVSI, rating of DC-link voltage for each VSI is diminished by around 10.29% from 750 V to 680 V, as compared to classic VSI.
- Reduction in rating of VSC: as a result of decrement in current supplied by VSC because of converter transformer plus VSC interfacing impedance, VSC rating is reduced.
- Flexibility in inverter operation: coupling of VSC via converter transformer results in ease in maintenance which increases system flexibility.
- Increment in the efficiency of system: matching impedance in between interfacing impedance of VSC and converter transformer results in increment in efficiency of system.
- Protection against in source over current harmonics: the flexible protection against harmonics over current is performed without losing shunt compensation due to involvement of both the BC and PF.

3. COMPREHENSION OF IFCT, BC AND PF

The systematic structure of the proposed BC supported IC-DBC based DSTATCOM along with PF is revealed in Figure 3. The mathematical model for IFCT is given in the sub-section 3.1. Also, BC and PF topologies are explained in the successive sub-sections.

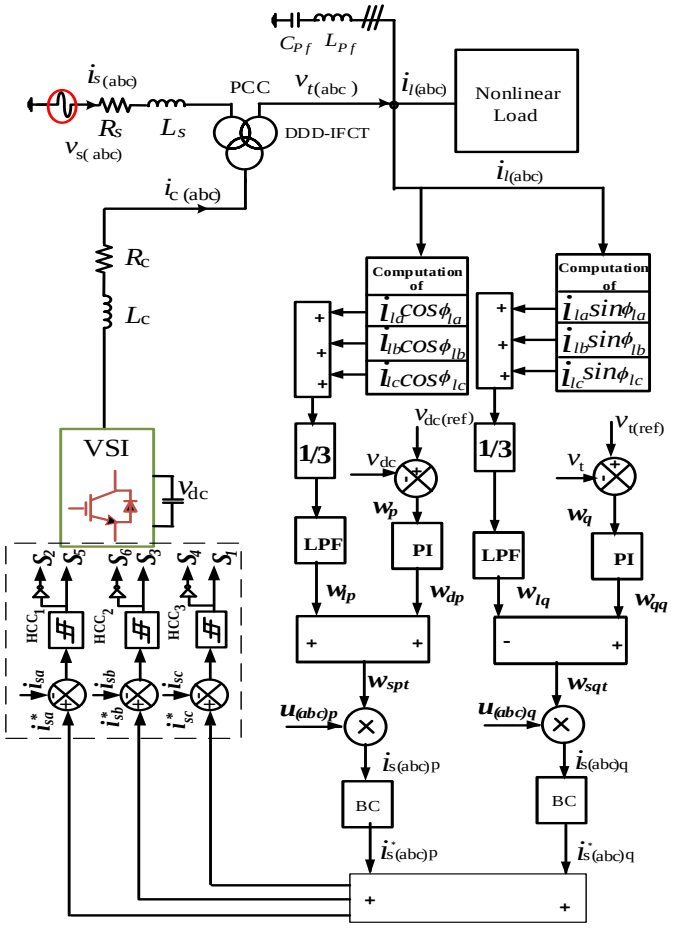


Figure 3. Switching signals generation using icosϕ control algorithm for the proposed system

3.1. Comprehension of IFCT

The IC-DSTATCOM configures inductively filter converting transformer (IFCT) with DSTATCOM consisting voltage source inverter (VSI). The IFCT structure has 3 winding which is used for connecting DSTATCOM, source and non-linear load. Among 3 windings, the primary winding (PW) with delta connection with grid, secondary side winding (SW) with delta wiring connection with non-linear load and the filtering winding (FW) with delta connection is used for connecting DSTATCOM. The purpose of special winding of IFCT is to achieve the potential balanced in between grid, load and DSTATCOM. So, we can say that harmonics are inaccessible from PW. The in-depth mathematical model for IFCT and filtering mechanism are described in the successive section.

The balance equation for voltage can be expressed as:

$$\begin{cases} N_1 i_{ap} + N_2 i_{as} + N_3 i_{af} = 0 \\ N_1 i_{bp} + N_2 i_{bs} + N_3 i_{bf} = 0 \\ N_1 i_{cp} + N_2 i_{cs} + N_3 i_{cf} = 0 \end{cases} \quad (1)$$

in relation to Kirchhoff's current law, for current the equations are given below:

$$\begin{cases} u_{abf} = (i_{zb} - i_{za})/Z_o \\ u_{bcf} = (i_{zc} - i_{zb})/Z_o \\ u_{caf} = (i_{za} - i_{zc})/Z_o \end{cases} \quad (2)$$

$$\begin{cases} i_{ap} = (u_{sa} - u_{apo})/Z_{line} \\ i_{bp} = (u_{sb} - u_{bpo})/Z_{line} \\ i_{cp} = (u_{sc} - u_{cpo})/Z_{line} \\ i_{as} = i_{al} + i_{zal} \\ i_{bs} = i_{bl} + i_{zbl} \\ i_{cs} = i_{cl} + i_{zcl} \\ i_{ap} + i_{bp} + i_{cp} = 0 \\ i_{as} + i_{bs} + i_{cs} = 0 \\ i_{af} + i_{bf} + i_{cf} = 0 \\ i_{af} = i_{cf} + i_{cat} = i_{cf} + i_{ra} + i_{za} \\ i_{bf} = i_{af} + i_{cbt} = i_{af} + i_{rb} + i_{zb} \\ i_{cf} = i_{bf} + i_{cct} = i_{bf} + i_{rc} + i_{zc} \end{cases} \quad (3)$$

moreover, as per the multi-winding transformer theory, transfer equations for voltage are given as (4).

$$\begin{cases} u_{apo} - \frac{N_1}{N_3} u_{abf} = i_{ap} z_p - \frac{N_1}{N_3} i_{af} z_f \\ u_{bpo} - \frac{N_1}{N_3} u_{bcf} = i_{bp} z_p - \frac{N_1}{N_3} i_{bf} z_f \\ u_{cpo} - \frac{N_1}{N_3} u_{caf} = i_{cp} z_p - \frac{N_1}{N_3} i_{cf} z_f \end{cases} \quad (4)$$

3.2. Comprehension of BC

The BC principle is utilized to normalize the active tuning function by adjusting the control gain. The control gain is achieved by regulating the filter weight obtained from both active and reactive side. Finally reference current is sent to hysteresis current controller (HCC) and drivers in order to produce the switching devices driving signals.

In fact, the following equation is stablished considering the filter detuning interval δ and δ_0 in the range of -0.2≤0.2.

$$\delta = \frac{1-(1-\delta_0)^2}{1-(1-\delta_0)^2} = \frac{2\delta_0 - {\delta_0}^2}{2+{\delta_0}^2-2\delta_0} = \frac{2\delta_0}{2-2\delta_0} \approx \delta_0 \quad (5)$$

Where, δ measured detuning factor and δ_0 theoritical detuning factor.

3.3. Realization of PF

The PF consist of two inductor-capacitor (LC) to tune fifth and seventh harmonics. For fifth order harmonic, its values will be $L_{PF5} = 13.5\,mH$, $C_{PF5} = 30\,\mu F$. Also, for seventh order harmonic, it will be $L_{PF5} = 6.75\,mH$, $C_{PF7} = 30\,\mu F$.

4. icosϕ CONTROL ALGORITHM

Control structure design for proposed system's is potrayed in Figure 3. In order to improve power factor and mitigation of current harmonics, reference source current is generated from 3-ϕ load current (non-linear in nature). Due to fast and robust dynamic response in steady-state as well as transient condition, *icosϕ* controller is selected in order to generate gate signals for inverter switches. Figure 3 shows the gereration of switching signal using *icosϕ* control algorithm. Following four steps describe the generation of the gate signals for DSTATCOM controlling:

- Fourier block is utilized for computing the fundamental quantity of 3-ϕ load current (i_L).
- Both active as well as reactive load current is produced by implementating the prposed control technique.
- According to algorithm, ref. source currents can be generated by utilizing active as well as reactive load currents.
- The switching signals can be generated by fedding sum of active and reactive load current to HCC.

The active power component of fundamental load current can be specified as (6).

$$\begin{bmatrix} i_{lap} \\ i_{lbp} \\ i_{lcp} \end{bmatrix} = \begin{bmatrix} Re(i_{la}) \\ Re(i_{lb}) \\ Re(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}cos\phi_{la} \\ i_{lb}cos\phi_{lb} \\ i_{lc}cos\phi_{lc} \end{bmatrix} \tag{6}$$

The weighted average value of the active power component (w_p):

$$w_p = \left(\frac{i_{la}cos\phi_{la}+i_{lb}cos\phi_{lb}+i_{lc}cos\phi_{lc}}{3}\right) \tag{7}$$

by using similar processes component of reactive power can be obtained as:

$$\begin{bmatrix} i_{laq} \\ i_{lbq} \\ i_{lcq} \end{bmatrix} = \begin{bmatrix} Im(i_{la}) \\ Im(i_{lb}) \\ Im(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}sin\phi_{la} \\ i_{lb}sin\phi_{lb} \\ i_{lc}sin\phi_{lc} \end{bmatrix} \tag{8}$$

for reactive power component, weighted average value (w_q) is:

$$w_q = \left(\frac{i_{la}sin\phi_{la}+i_{lb}sin\phi_{lb}+i_{lc}sin\phi_{lc}}{3}\right) \tag{9}$$

with the error of v_{de} in DC supply, output for proportional integral (PI) controller can be given by (10).

$$w_{dp} = k_{pdp}v_{de} + k_{idp}\int v_{de}dt \tag{10}$$

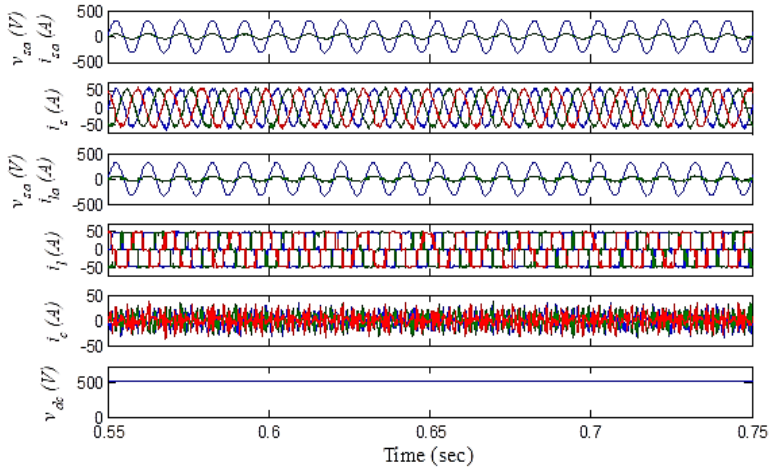
Also, 'w_p' and 'w_q' are the average value of active and reactive weighted components correspondingly. The clustered weights 'w_p' and 'w_q' doesn't give guarantee for tuned value. These restrictions are overwhelmed by offering low pass filter (LPF) as presented in Figure 4. The LPF diminish the harmonics component of higher order from these weights. Therefore, the load current active component (w_{spt}) and reactive component (w_{sqt}) tuned weight are obtained. Lastly, the proposed control technique is intended to get a filtered as well as tuned weight. For any disturbance, tuned weight becomes more stable and suitable because it is less affected by noise. It results in injection of the appropriate compensator current at the PCC. The total active components of the ref. source current is obtained by summing output of PI controller and weighted average value of the active power component.

$$w_{spt} = w_{dp} + w_{lp} \tag{11}$$

In similar procedures, computation of total reactive components is given by:

$$w_{sqt} = w_{qq} - w_{lq} \quad (12)$$

for filteration of active as well as reactive weighting factor of load current, 20 Hz cut off frequency LPF is used.



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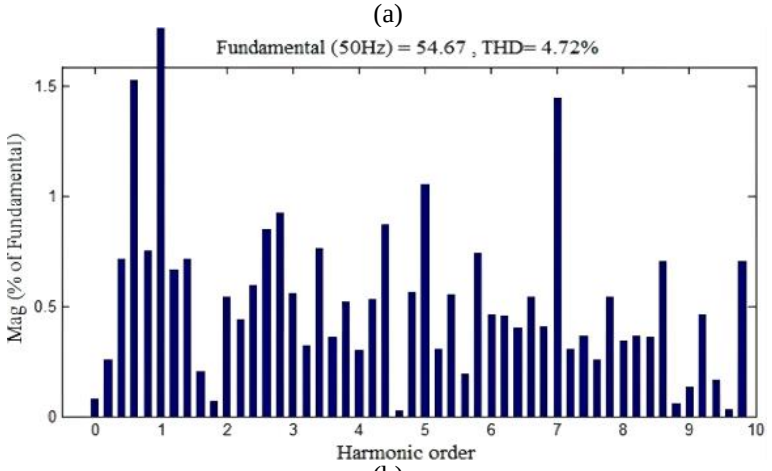

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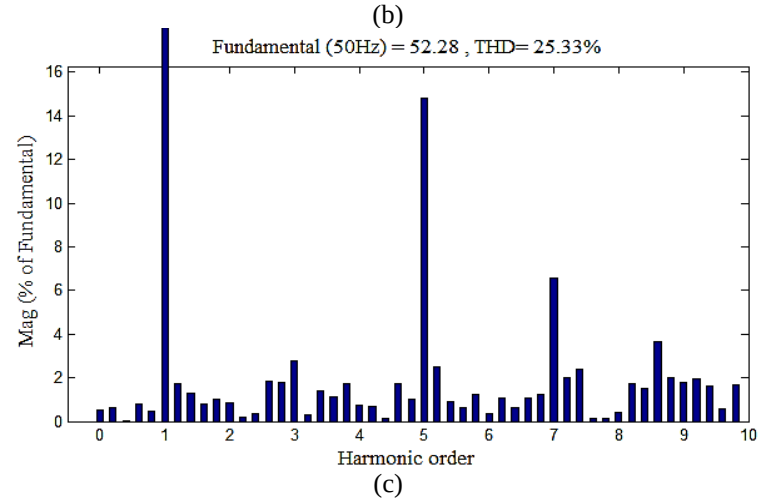


(c)

Figure 4. Simulation outcome for (a) performance considerations starting from a-phase source-side voltage and current, source-side current, a-phase source-side voltage and load-side current, load-side current, compensating currents, and DC-link voltage using DC-DBC based DSTATCOM; (b) source-side current THD; and (c) load-side current THD

Instantneous value of the active source currents i_{sp}, can be obtained as (13).

$$\begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} = w_{spt} \begin{bmatrix} u_{ap} \\ u_{bp} \\ u_{cp} \end{bmatrix} \quad (13)$$

Instantneous reactive source current values i_{sq}, can be calculated as (14).

$$\begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} = w_{sqt} \begin{bmatrix} u_{aq} \\ u_{bq} \\ u_{cq} \end{bmatrix} \quad (14)$$

Both i_{sp} and i_{sq} component are processed through the BC. The output of the BC for both active and reactive component are represented by i_{sp}^* and i_{sq}^* respectively.

In conclusion, reference source current values are demonstrated as (15).

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} i_{sap}^* \\ i_{sbp}^* \\ i_{scp}^* \end{bmatrix} + \begin{bmatrix} i_{saq}^* \\ i_{sbq}^* \\ i_{scq}^* \end{bmatrix} \quad (15)$$

Both actual (i_{sa}, i_{sb}, i_{sc}) as well as the reference ($i_{sa}^*, i_{sb}^*, i_{sc}^*$) source currents of the corresponding phases are equated, subsequently error signals of current are fed to HCC. At this point, HCC is commonly used for easier implementation and hardware complexities curtailment. It functions as follows:

- When $i_{sa} < i_{sa}^*$, s_1 is ON and s_4 is OFF
- When $i_{sa} > i_{sa}^*$, s_1 is OFF and s_4 is ON

Their outputs are used to produce the single VSC switching signal and proposed VSC based DSTACOM.

5. SIMULATION OUTCOMES

To validate the different strategies, system presented in the Figure 1 has been simulated in MATLAB/Simulink by using toolbox of sim power system. The simulated system is a 3-phase power system in which sinusoidally balanced three phase 230 V (rms)/phase source having a 2 mH inductance and 0.5 **Ω** resistance is used. Table 1 portrays various parameters use for simulating the three case studies of DC-DBC based DSTATCOM, IC-DBC based DSTATCOM, and BC supported IC-DBC based DSTATCOM with PF using *icosϕ* algorithm. The selection of appropriate topology for PDS is carried out through the simulation work. These performances are analyzed and presented in the below sub-sections.

Table 1. Performance parameters of proposed system for simulation study

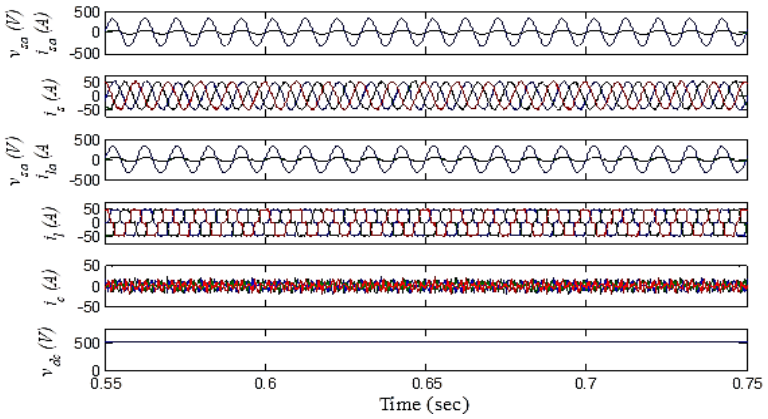
Grid-side	Load Side	Controller		VSC
v_s= 230V	3-ϕ diode bridge	α= 0.4	k_{pa}= 0.7	v_{dc}= 2 × 10^{-3} F
(L-N)	rectifier	γ= 0.01	k_{ia}= 0.1	R_C= 0.25 Ω
f_s= 50 Hz	R_l= 10 Ω	$v_{dc\,(ref)}$= 600V	k_{pq}= 0.5	L_C= 1.5 × 10^{-3} H
R_s= 40 × 10^{-3} Ω	L_l= 20 × 10^{-3} H	v_t= 325V	k_{iq}= 0.02	
L_s= × 10^{-3} H				

5.1. Simulation outcomes of DC-DBC based DSTATCOM

The simulation behavior of the DC-DBC based DSTATCOM in PDS is investigated to demonstrate effectiveness and feasibility in the Figure 4. This observation was obtained in response to the balanced non-linear uncontrolled rectifier loading in between 0.55 sec to 0.75 sec. In this Figure 4(a), all the subplots are arranged as source-side voltage and current, source-side current, source voltage and load current, compensating current, DC-link voltage correspondingly. Due to shunt compensation, the power factor is upgraded to 0.94 and THD% decreased to 4.72 which is shown in Figure 4(b). Load-side current THD% of 25.33 is shown in Figure 4(c). Additionally, voltage of DC link is retained with an acceptable voltage regulation of 550.25 V under this observation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures the better power to end-users in the PDS.

5.2. Simulation outcomes of IC-DBC based DSTATCOM

The simulation study of the IC-DBC based DSTATCOM in PDS is analyzed to show the effectiveness and feasibility in the Figure 5. This observation was obtained in response to the balanced nonlinear uncontrolled rectifier loading in between 0.55 sec to 0.75 sec. In this Figure 5(a), all the subplots are arranged as source-side voltage and current, source-side current, source-side voltage, and load-side current, compensating current, DC-link voltage correspondingly. Due to shunt compensation, power factor is upgraded to 0.99 and THD% decreased to 4.34 as painted in Figure 5(b). Load-side current THD% of 20.81 is shown in Figure 5(c). Moreover, the DC-link voltage is maintained with a tolerable voltage regulation of 536.16 V under this observation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures the better power to end-users in the PDS.



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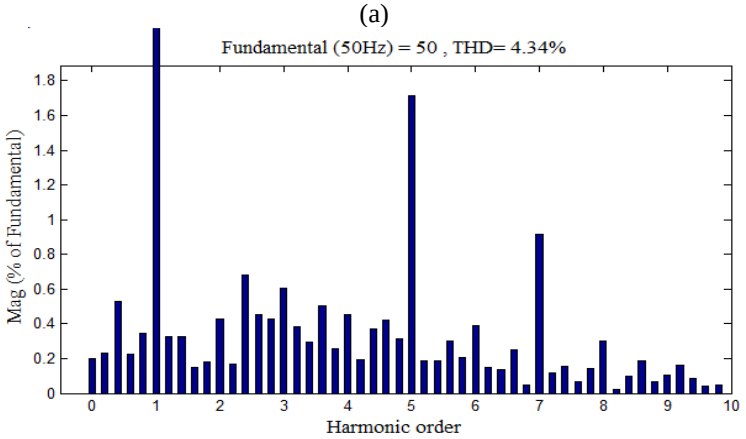

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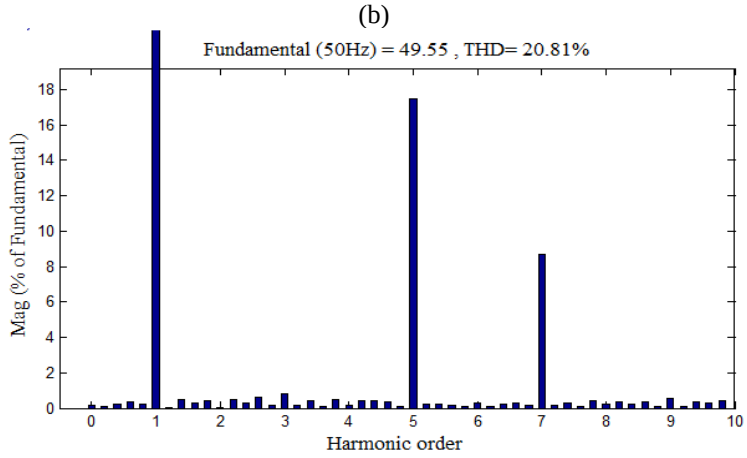

(c)

Figure 5. Simulation outcome for (a) performance considerations starting from a-phase source-side voltage and current, source-side current, a-phase source-side voltage and load-side current, load-side current, compensating currents, and DC-link voltage using IC-DBC based DSTATCOM; (b) source-side current THD; and (c) load-side current THD

5.3. Simulation outcomes of BC supported IC-DBC based DSTATCOM with PF

The simulation study of the BC supported IC-DBC based DSTATCOM with PF in PDS is analyzed to show the effectiveness and feasibility in the Figure 6. This observation was obtained in response to the balanced non-linear uncontrolled rectifier loading in between 0.55 sec to 0.75 sec. In this Figure 6(a), all the subplots are organized starting from voltage and current from source side, source currents for all three phases, source voltage and load current, compensating current, DC-link voltage respectively. Because of shunt compensation, power factor is upgraded to 0.99 and THD% shrinkages to 3.00 which is painted in Figure 6(b). Load current THD% 7.71 is shown in Figure 6(c). Furthermore, the DC link voltage is maintained with an acceptable voltage regulation of 559 V under this observation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures the better power to end-users in the PDS. Finally, the comparative study is presented for the selection of the system among the DC-DBC based DSTATCOM and IC-DBC based DSTATCOM and BC supported IC-DBC based DSTATCOM with PF in the Table 2.

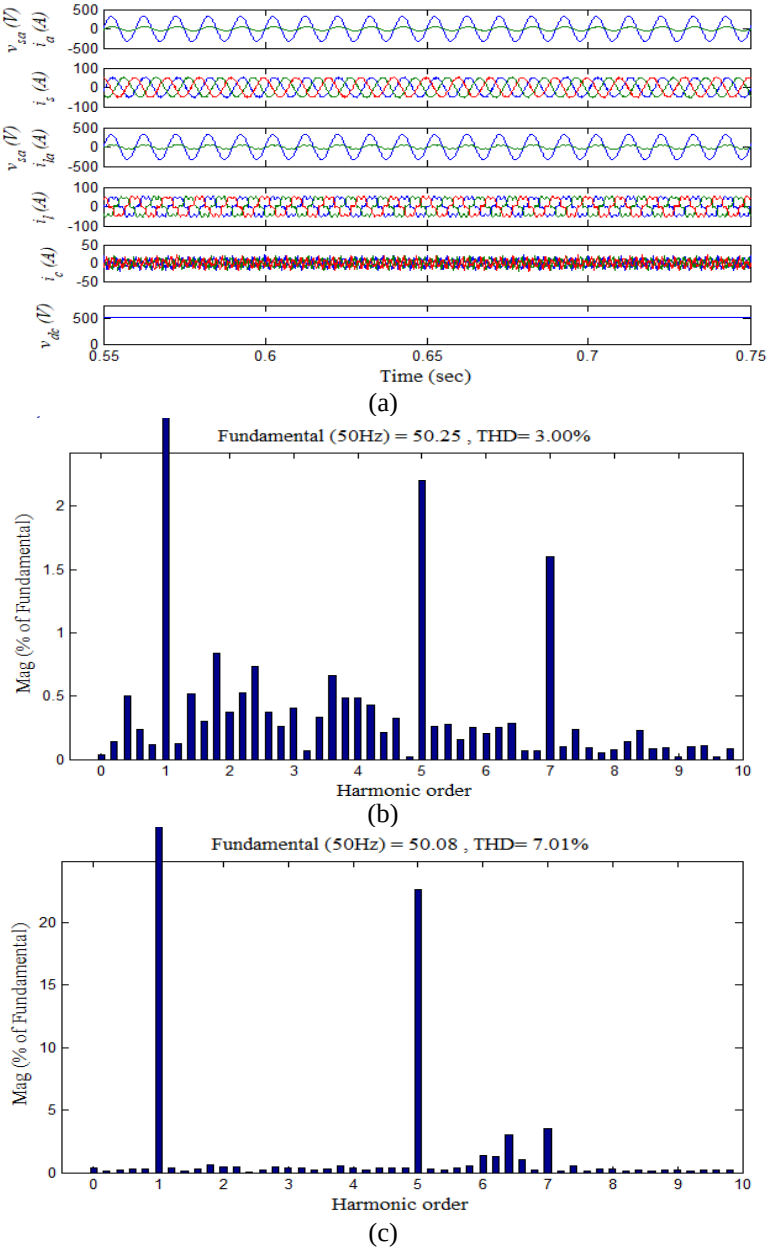

Figure 6. Simulation outcome for (a) performance considerations starting from a-phase source-side voltage and current, source-side current,a-phase source-side voltage and load-side current, load-side current, compensating currents, and DC-link voltage using BC supported IC-DBC based DSTATCOM with PF; (b) source-side current THD; and (c) load-side current THD

Table 2. Performance parameters of DC-DBC based DSTATCOM and IC-DBC based DSTATCOM and BC supported IC-DBC based DSTATCOM with PF

Performance Parameter	DC-DBC based DSTATCOM	IC-DBC based DSTATCOM	BC supported IC-DBC based DSTATCOM with PF
i_s (A), %THD	54.52, 4.72	50, 4.34	50.25, 3.00
v_s (V), %THD	325.26, 2.23	325.26, 1.42	325.26, 1.42
i_l (A), %THD	53.09, 25.60	49.55, 20.81	50.08, 7.01
Power Factor	0.94	0.99	0.99
v_{dc} (V)	550.25	536.16	537.18

5. CONCLUSION

The presented BC supported IC-DSTATCOM with PF is utilize for PQ improvement including flexible protection against harmonics over current. The realization of proposed 3-Φ topology has the subsequent features such as the over-all power supplied to the load by coupling transformer, BC and PF provides increased relibility, better utilization of power, reduce in filter size of the inverter as well as reduce the harmonics over current.

Also, BC principle employs the independent control performance immune to the filter parameter unbalance. Additionally, PF performers selective harmonics elimination rather than global harmonics elimination. Dual buck converter results in less switching surges, over voltage protection, realibility improvement. The over load risk owing to the current harmonics of non-linear loads is eliminated by the hybrid filters. Moreover, it is considered as the of the proposed configuration provides the virtues such as diminution in component stress, ease in maintenance, modularity and incorporating. In overall, designed topology as well as controller demonstrations admirable reference tracking, rejection in harmonic distortion and property of balancing in power sharing.

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