An Adaline model predictive control strategy based DSTATCOM for power quality enhancement

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ABSTRACT

This paper represents a least mean square (LMS) built Adaline current estimator in conjunction with model predictive control (MPC) approach (Adaline-MPC) employed for distribution-static-compensator (DSTATCOM) to enrich power quality within power distribution network. The real fundamental frequency components of load currents are estimated via LMS-built Adaline adopting instantaneous weight computation and reference currents are further formed by means of multiplying these weights with unit vector templates. A proportional-integral (PI) controller is engaged in support of continual maintenance of DC-capacitor voltage. Moreover, the switching signals of voltage source converter (VSC) are created via applying MPC wherein source currents should track the reference currents, which is derived from Adaline current estimator. Both MATLAB based simulation and Opal-RT based real-time experimental outcomes are demonstrated and the effectiveness of the proposed Adaline-MPC based DSTATCOM towards power quality improvement has been verified.

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1. INTRODUCTION

In contemporary electrical distribution system, explosion of non-linear loads for example, adjustable speed drives (ASDs), switched mode power supply (SMPS), rectifiers, arc furnaces, computers, and printers are the primary cause behind harmonic deformation that grows towards power quality (PQ) crises [1]. Load adjustment can resolve the PQ issues for instance, harmonic eradication along with reactive power compensation. Distribution-static-compensator (DSTATCOM) [2], [3] is being sustained to be an appropriate custom power device, which sustains eradication of harmonics and re-compensation of reactive power within distribution system. DSTATCOM remains to be built upon power converter, proper control tactic (reference creation) and current regulation design (current regulator) [4].

Wide-ranging control of DSTATCOM governs two foremost actions: the primary one incorporates taking out of reference currents and the subsequent one includes generation of switching signals. The reference current extraction schemes reported in the literature comprise instantaneous reactive-power theory (IRPT), instantaneous symmetrical components theory (ISCT), instantaneous symmetrical component active power theory (ISCAP), unit vector method, neural network and fuzzy logic control-based scheme, Synchronous reference frame (SRF) and per phase calculation [5]-[8]. The ISCAP, which gives explicit option of choosing power factor, is used to compute reference source currents [5]. The IRPT comprises active

and reactive power computation via alteration of phases from three to two and falls short of performing underneath distorted utility surroundings. Further, Akagi's p-q theory is employed to decide alpha-beta quantities of reference supply currents [6]. The in phase and in quadrature component of the current and unit current vectors are employed to determine component of the reference supply current [7]. Subsequently, the SRF concept is built upon separating DC constituents of current through a low pass filter (LPF) inside synchronous rotating framework. A coordinated voltage control scheme is maintained in [9], utilizing on-load tap changer and DSTATCOM and likewise active power curtailment is used as an emergency control action. Several soft computing methodologies [10], [11] have been functioned over active power filter to extract reference current. Moreover, neural-network built systems necessitate off-line training meant for an array of loads that make the system appropriate for specific loads [12]-[15]. Some authors have offered an Adaline-built methodology to evaluate reactive power as well as harmonic for the current [15]. However, this approach becomes unsuccessful at unbalance compensation and at DC-voltage self-maintenance of DSTATCOM.

Concerning the aforementioned drawbacks, this paper recommends an appropriate control strategy for DSTATCOM comprising self-maintenance of DC-bus along with adjustment for harmonics, reactive power and imbalanced loading. The withdrawal of source reference currents is supported by employing least mean square (LMS)-built Adaline, which is an extremely common and quick methodology designed for current removal. Merely three Adaline are consumed to obtain the three-phase positive sequence fundamental frequency for load currents. The LMS set of rules [16] accompanied by online computation of weights respond well at extreme load deviances. Further, the DC-capacitor voltage remains self-supported via a proportional-integral (PI) controller that provides a loss constituent of the current signal. Additionally, in-phase unit vector templates for the synchronized signals are created by utilizing filtering through a fourth-order digital filter, and the delay of filtered signal is adjusted by means of the ISCAP.

Most recently, model predictive control (MPC) is being well-known in numerous appliances owing to its proficiency at fast operational outcomes, improved control precision and quite reliable through digital control conditions [17]-[19]. The leading characteristic of MPC lies within the system model that predicts the forthcoming action of control parameters. Together with this scenario, MPC has been employed towards a category of arrangement including multi-variables, constraints as well as non-linearities [20]-[22]. The advancement of fast-rate digital regulators empowers MPC to be employed towards power electronics mechanisms incorporating grid-connected converters, active power filters, motor drives, and rectifiers [23], [24].

The aforesaid discussion motivates towards implementation of the proposed Adaline-MPC-based DSTATCOM in this paper for alleviation of harmonics as well as compensation of reactive power in three-phase distribution network underneath unbalanced linear and nonlinear load. The paper is arranged as follows. A structural configuration of the suggested scheme is offered in section 2. A brief report of the suggested reference generation scheme and a general MPC methodology is detailed in sections 3 and 4 respectively. In section 5, the performance indicators employed for valuation are deliberated. Finally, simulation combined with experimental outcomes is expressed followed by the conclusion.

2. SYSTEM ARRANGEMENT OF DSTATCOM

A DSTATCOM [3] coupled to a non-linear load through a three-phase, three-wire distribution is shown in Figure 1. A nonlinear load is defined by a three-phase full diode-bridge rectifier. Considerably, six insulated-gate-bipolar transistors (IGBTs) and anti-parallel diodes are used to make a three-phase voltage source converter (VSC)/DSTATCOM. Interface inductors are employed to filter high-frequency compensatory currents and are placed adjacent to the point of common coupling (PCC). The Adaline-MPC is employed to create switching signals via a variable structure algorithm (methodology), not including any modulator as recommended for traditional methods such as deadbeat current control, linear PWM scheme.

In order to represent the dynamics of the VSC, differential equations that manage two-level types of inverters need to be resolved. The VSC model is established upon discrete type switching variables gt_a, gt_b, gt_c, where a, b, and c represent three-phase system. Accordingly, voltages exerted by the inverter such as v_{ka}, v_{kb}, v_{kc} are expressed below.

$$\begin{bmatrix} v_{ka} \\ v_{kb} \\ v_{kc} \end{bmatrix} = \frac{V_{dc}}{\sqrt{3}} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} gt_a \\ gt_b \\ gt_c \end{bmatrix} \tag{1}$$

Where V_{dc} represents DC-link voltage. Further, the R–L arrangement via the AC part of the converter is signified by following three differential calculations.

$$L_k \frac{di_{ka}}{dt} = -i_{k_a}.R_k + v_{sa} - v_{ka} \\ L_k \frac{di_{kb}}{dt} = -i_{kb}.R_k + v_{sb} - v_{kb} \\ L_k \frac{di_{kc}}{dt} = -i_{k_c}.R_f + v_{sc} - v_{kc}$$ (2)

Here L_k, R_k indicate filter inductance together with resistance. The current through filter inductor and the source voltages are denoted as i_{ka}, i_{kb}, i_{kc} and v_{sa}, v_{sb}, v_{sc} respectively. Moreover, the DC region calculations are expressed in (3) and (4).

$$i_{dc} = gt_a.i_{ka} + gt_b.i_{kb} + gt_c.i_{kc}$$ (3)

$$-C_{dc}.\frac{dv_{dc}}{dt} = i_{dc}$$ (4)

Where i_{dc} and C_{dc} signify current and capacitance across the DC-link side of Figure 1.
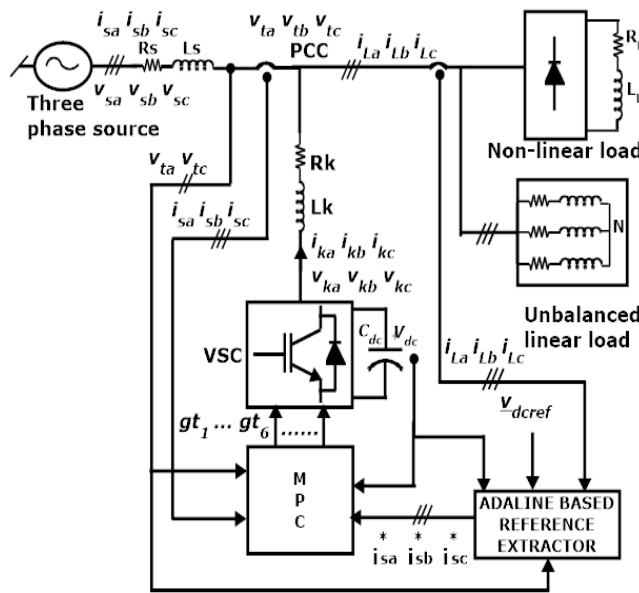

Figure 1. Structural arrangement of DSTATCOM

3. LMS ADALINE-BASED REFERENCE EXTRACTION

AC main is essential to supply real power demanded for compensation of losses such as switching losses, reactor losses as well as dielectric losses within a DSTATCOM system used in distribution network. Consequently, the supply currents are employed to adopt switching arrangement of VSC. For this accomplishment, two elements are involved; one exists as the load current's real fundamental frequency element being obtained through Adaline and the other one exists as DSTATCOM's losses being assessed via PI controller. The PI-controller's output is combined together with the weight evaluated via Adaline for preserving the capacitor voltage constant.

3.1. Removal of load current's real positive sequence fundamental frequency component

The fundamental concept behind suggested control strategy is LMS set of rules and its training over Adaline, that follows the unit vector template for preserving the least error. Figure 2(a) depicts the Adaline control structure. The load current i_L consisting of active-current (i_p^+), reactive-positive-sequence current (i_q^+), negative-sequence current (i^-) and harmonic current (i_h), is specified as (5).

$$i_L = i_p^+ + i_q^+ + i^- + i_h$$ (5)

The control process is established upon the drawing out of current element in phase with unit voltage template. To evaluate the load current's real fundamental positive sequence constituent, the unit vector template ought to be in phase with the system voltage of unity magnitude. The unit vector template (u_p) is originated with reference to the PCC voltage as expressed in (6).

$$u_p = \frac{v_t}{V} \tag{6}$$

Where v_t stands for filtered instantaneous PCC voltage and 'V' stands for its amplitude.

In order to conduct an accurate analysis of the components of the load current, the unit vector template must stay uninterrupted. Furthermore, in facilitating the creation of unit vector templates, the sampled phase voltage must be passed through a butter-worth filter of the fourth order. The load current's active power component is calculated by multiplying weight together with unit vector template and this weight (j_p) is assessed via LMS algorithm tuned Adaline method. The weight estimation approach depicted in Figure 2(b) is expressed as (7).

$$j_{p(k+1)} = j_{p(k)} + \xi\{i_{L(k)} - j_{p(k)}u_{p(k)}\}u_{p(k)} \tag{7}$$

The convergence co-efficient ξ decides estimation accuracy. The value of ξ lies between 0.01 and 1. High value of ξ leads to inaccurate result with high rate of convergence of weights whereas small value of ξ improves accurateness of estimation with small weight convergence. The reasonable trade-off noticed in terms of precision and speed of convergence for value ξ is 0.25. Three phase currents analogous to the load current's real positive sequence component, are estimated via multiplication of three phase unit templates together with average weight (j_p^+).

$$j_p^+ = (j_{pa}^+ + j_{pb}^+ + j_{pc}^+)/3 \tag{8}$$

For suitable assessment of reference currents, the suggested weights designed for three phases ($j_{pa}^+, j_{pb}^+, j_{pc}^+$) are getting averaged to calculate the correspondent weight for positive sequence current appearing in decomposed form. The weight's average quantity removes unbalance contained inside the current constituents.
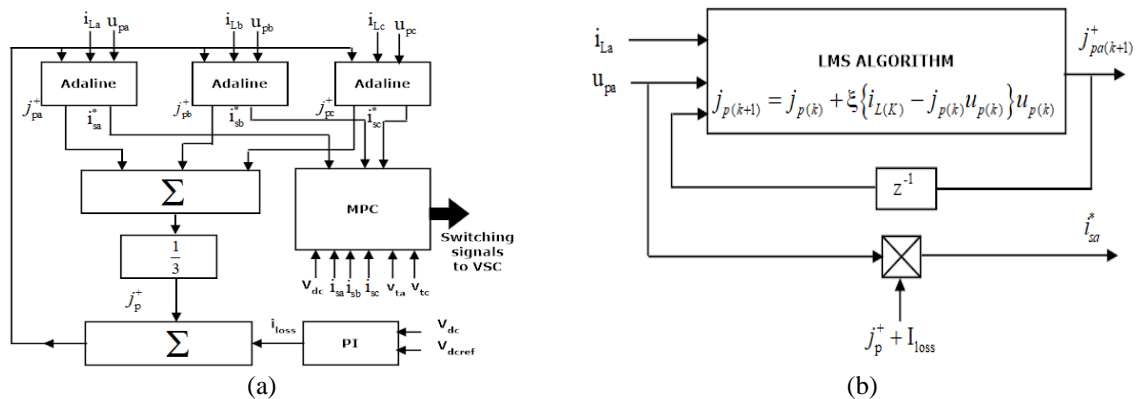

Figure 2. Control methodology of DSTATCOM (a) Adaline control structure and (b) reference extractor

3.2. PI controller for preserving steady DC-link voltage

The second constituent of reference current is calculated by relating reference DC-capacitor voltage (V_{dcref}) with sensed DC-capacitor voltage (V_{dc}) for DSTATCOM. Assessment of actual and sensed DC-capacitor voltage results in voltage error which is processed by PI controller and the outcome of PI controller ($i(n)$) is stated at nth sampling time (sampling period = T_s).

$$i(n) = i(n-1) + k_p\Delta e(n) + \frac{T_s}{2}k_i e(n) \tag{9}$$

At this point, k_p and k_i stand for proportional as well as integral constants of PI controller, $\Delta e(n) = e(n) - e(n-1)$ and $e(n) = V_{dcref} - V_{dc}$.

The outcomes of PI controller count on behalf of the losses in DSTATCOM which are added together with the weights determined via Adaline concerning load current's fundamental positive sequence real part. The whole real reference current has a part analogous to load and another part analogous to losses in DSTATCOM, which are provided as (10).

$$\left.\begin{aligned} i_{sa}^* &= \left(j_{pa}^+ + i(n)\right)u_{pa} \\ i_{sb}^* &= \left(j_{pb}^+ + i(n)\right)u_{pb} \\ i_{sc}^* &= \left(j_{pc}^+ + i(n)\right)u_{pc} \end{aligned}\right\} \tag{10}$$

$i_{sa}^*, i_{sb}^*, i_{sc}^*$ and u_{pa}, u_{pb}, u_{pc} signify reference source currents and unit vector templates of PCC voltage respectively. The reference source currents $i_{sa}^*, i_{sb}^*, i_{sc}^*$ as well as detected source currents i_{sa}, i_{sb}, i_{sc} are served towards MPC to decide the switching state. The switching signals are created via MPC controller.

4. MPC STRUCTURE

The predictive model control structure is established upon finite quantity of switching conditions as illustrated inside Figure 3. The system is managed to expect the behaviour of switching components for every single situation. A cost function 'q' remains utilised to improve and pick out a situation permitting least possible error. Further, this situation is operated over converter for similar moment.

4.1. Converter model

Figure 4 illustrates the switching situations for the converter, which are decided via the gating indicators g_a, g_b, g_c as provided below.

$$gt_a = \begin{cases} 1 & \textit{if S1 on and S4 off} \\ 0 & \textit{if S1 off and S4 on} \end{cases} \quad gt_b = \begin{cases} 1 & \textit{if S3 on and S6 off} \\ 0 & \textit{if S3 off and S6 on} \end{cases} \quad gt_c = \begin{cases} 1 & \textit{if S5 on and S2 off} \\ 0 & \textit{if S5 off and S2 on} \end{cases}$$

The vectorial form (g_v) of the switching variables g_a, g_b, g_c may be stated as (11).

$$gt_v = p1[gt_a + agt_b + a^2gt_c] \tag{11}$$

Here $a = e^{j2\pi/3}$ and p1=2/3. Below is an illustration of the voltage space vector intended for the convert (v_{kv}).

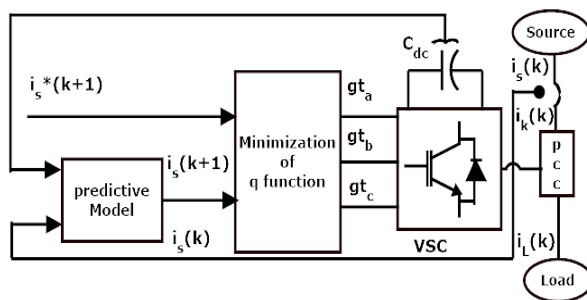$$v_{kv} = V_{dc} * g_v \tag{12}$$

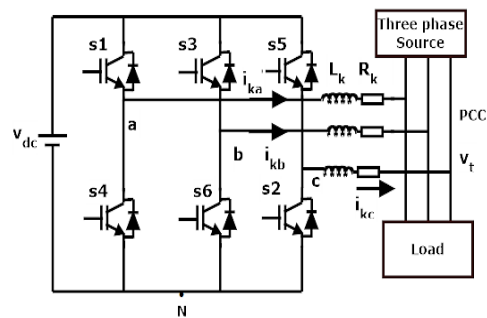Figure 3. Predictive model configuration   Figure 4. Power circuitry for VSC

4.2. Discrete-time model for the supply current

A power circuitry defining the recompensing current model is exhibited within Figure 4. A discrete arrangement of supply current meant for a sampling time T_s is applied to assess the estimate value along with computed PCC voltage v_t and inverter voltage v_k by k_{th} sample moment.

$$i_s(k+1) = \zeta\left\{\left(1 - \frac{R_kT_s}{L_k}\right)i_s(k) + \frac{T_s}{L_k}[v_{kv}(k) - v_t(k)]\right\} \tag{13}$$

$$i_s(k + 1) = \zeta\{d_1 i_s(k) + d_2[v_{kv}(k) - v_t(k)]\} \tag{14}$$

Where $d_1 = (1 - \frac{R_k T_s}{L_k})$, $d_2 = \frac{T_s}{L_k}$, and ζ = gain factor for compensating losses. The following can be used to represent the vectorial form of terminal voltage.

$$v_t = p2[v_{ta} + av_{tb} + a^2 v_{tc}] \tag{15}$$

Where p2=$\sqrt{2/3}$.

The inverter is responsible for controlling the voltage vector that, out of the seven prospective voltage vectors that result in seven different compensating current computations, has a current calculation that is closest to the reference compensating current. The following cost function can be used to determine the voltage vector.

$$q = |i_{s\alpha}^*(k + 1) - i_{s\alpha}(k + 1)| + |i_{s\beta}^*(k + 1) - i_{s\beta}(k + 1)| \tag{16}$$

Where $i_{s\alpha}$ and $i_{s\beta}$ represent the real in addition to imaginary quantities meant for the predicted current $i_s(k + 1)$, $i_{s\alpha}^*$ and $i_{s\beta}^*$ designate the real as well as imaginary quantities meant for the future reference current. Owing to unknown value of the forthcoming reference current, it may be approximated via utilization of Lagrange second order extrapolation that is defined as (17).

$$i_s^*(k + 1) = 3i_s^*(k) - 3i_s^*(k - 1) + i_s^*(k - 2) \tag{17}$$

4.3. Set of rules for the proposed MPC
A set of rules for model predictive controller is demonstrated in subsequent stages:
- Employ the new switching condition.
- Compute capacitor voltage, compensating current in addition to terminal voltage.
- Determine the whole seven probable vectors for VSC.
- Calculate compensating current.
- Assess forthcoming reference current for next sampling moment T_s.
- Employ optimization method by means of cost function q.
- Choose $g(i_{op})$ in such a way that calculated compensating current is nearer towards reference value.

The entire probable switching conditions are operated to create the switching pulses to perform over six IGBTs existing inside VSC. To analyze calculation over forthcoming currents, the entire probable voltage vectors have been taken. Individual predictions are assessed for the cost-function, and the index of the voltage-vector, which lowers the cost-function, is preserved. Commencement of the subsequent sampling moment deals with utilization of index value towards reading the table for switching parameters and creating reliable gate pulses to support IGBTs.

5. RESULTS AND DISCUSSIONS
With regard to validation, a wide-ranging simulation is adopted in MATLAB/Simulink in addition to real-time Opal-RT phase [25]. Simulation as well as real-time outcomes for conventional PI-MPC along with proposed Adaline-MPC built DSTATCOM scheme are represented below in subsequent portions.

5.1. Simulation output
DSTATCOM along with its control arrangement has been verified with MATLAB/Simulink. In order to verify its efficacy, a balanced three-phase voltage supply is applied to an unbalanced non-linear load that includes both a three-phase star-based unbalanced-linear R-L load and a three-phase diode-bridge rectifier supporting R-L load. The parameters applied for simulation as well as real-time are précised (Table 1) to accomplish simulation as well as real-time investigation.

The steady behaviour for the PI-MPC built DSTATCOM approach is illustrated within Figure 5. At compensation beforehand, the supply current remains similar to load current as depicted through Figure 5(a). Figure 5(b) signifies the supply current at compensation afterwards, that is freed from disruption and the total harmonic distortion (THD) is perceived as 3.0454%. The compensating current's waveform is represented in Figure 5(c). The DC-capacitor voltage grows towards fixed point (140 V) and remains stable during 0.0141 s as represented through Figure 5(d).

The supply current at compensation afterwards, keeps same phase association with supply voltage signifying unity power factor (Figure 5(e)). The waveforms for active-power and reactive-power, for instance, "p_a" and "q_r", the compensation beforehand and afterwards, are illustrated through Figure 5(f). The supply current's harmonics meant for compensation beforehand and compensation afterwards are revealed within Figures 5(g) and 5(h) correspondingly. The steady behaviour for the suggested Adaline-MPC built DSTATCOM is revealed through Figure 6. The waveform of the supply current at compensation beforehand, remains similar to the load current shown within Figure 6(a). Figure 6(b) denotes compensated supply current, that remains sinusoidal and likewise the THD is achieved as 2.9223%. Further, the compensating current's waveform is demonstrated within Figure 6(c). The DC-capacitor voltage increases towards a fixed point (140 V) and remains stable at 0.0132 s, which signifies a smaller amount than traditional method illustrated within Figure 6(d).

Henceforth it is obvious that the suggested Adaline-MPC reveals superior functioning as associated with traditional PI-MPC method. The supply current at compensation afterwards, possesses same phase link with supply voltage (Figure 6(e)) and also the waveforms for active and reactive power are demonstrated through Figure 6(f). The supply current's harmonics intended for compensation beforehand and compensation afterwards are shown within Figures 6(g) and 6(h) correspondingly. This extensive simulation reveals satisfactory performance in terms of harmonic eradication as well as reactive-power compensation. The comprehensive simulation makes observations on the appropriateness of contributing to the elimination of harmonics and compensating for reactive power. This leads in a reduction in the levels of accuracy that may be achieved. the reference current is essentially followed by the supply current.
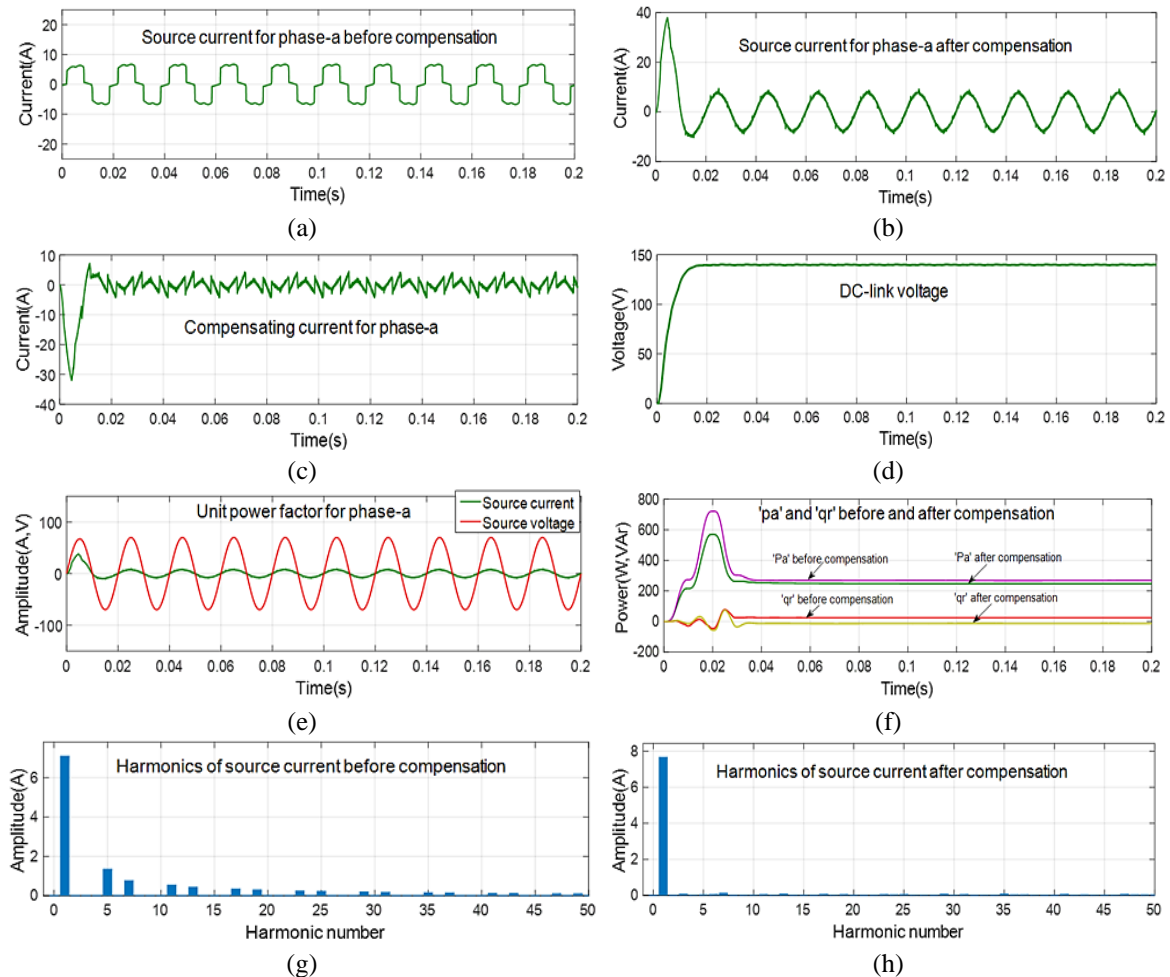

Figure 5. Simulation results (steady state) for PI-MPC built DSTATCOM: (a) supply-current of phase-a, prior to compensation, (b) phase-a supply current after compensation, (c) phase-a compensating-current, (d) DC-capacitor voltage, (e) phase-a unity power-factor, (f) both p_a and q_r prior and post compensation, (g) harmonics-spectrum of phase-a supply-current prior compensation, and (h) harmonics-spectrum of phase-a supply-current post compensation
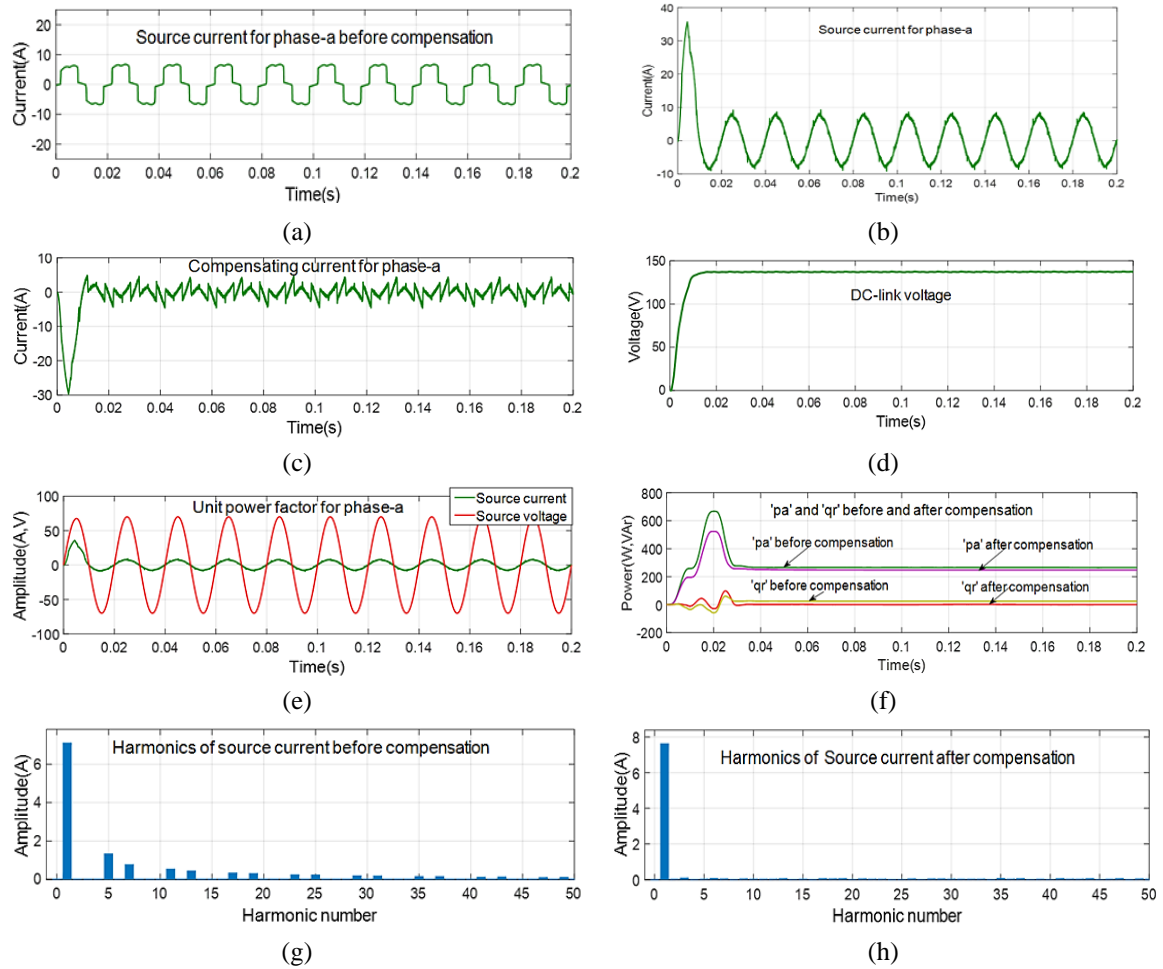
Figure 6. Simulation results (steady state) for proposed Adaline-MPC built DSTATCOM: (a) phase-a supply-current prior compensation, (b) phase-a supply-current post compensation, (c) phase-a compensating-current, (d) DC-capacitor voltage, (e) phase-a unity power-factor, (f) both pa and qr prior and post compensation, (g) harmonics-spectrum of phase-a supply-current prior compensation, and (h) harmonics-spectrum of phase-a supply-current post compensation

Table 1. Simulation and real-time parameters

Parameters	Value
Supply voltage	Three-phase balanced, 50 Vrms (L-N), 50 Hz,
Source-line impedance	R_s=0.11 Ω and L_s=0.18 mH
Nonlinear load	Three-phase full diode bridge rectifier including load (L=10 mH, R_L=20 Ω)
DC-Link-Capacitor	C_{dc}=1600 µF
Interfacing inductor	L_k=1.8 mH, R_k=0.09 Ω
DC-Capacitor voltage	V_{dc}=140 V
Unbalanced Linear load	Z_a=68+j33.41 Ω, Z_b=38+j19.56 Ω, Z_c=27.6+j13.46 Ω
PI regulator parameters	k_p=10, k_i=150
MPC parameters	C_1=0.9867, C_2=0.0133, ψ=3.51
Switching-frequency	f_{swmax}=26 kHz
Low-pass butter-worth filter	Order-4th (2xsecond order), structure: direct form-II, sampling frequency fs=50 kHz,
LPF1	cut-off frequency fc1=100 Hz
Adaline convergence coefficient	ξ=0.25

5.2. Experimental results and analysis

A real-time structure for suggested Adaline-MPC based DSTATCOM is implemented in Opal-RT [25]. Figure 7(a) displays the Opal-RT configurational arrangement. Substantially, the outcomes are exhibited in digital-storage oscilloscope (DSO) that remains associated via Opal-RT arrangement. OP5142 depicted within Figure 7(b) is utmost building blocks inside modular OP5000 I/O scheme from Opal-RT skill. To attain and create analog as well as digital signals, Opal-RT offers a straightforward stage.

Figure 7(c) refers to the jumpers and also interfaces accompanied within OP5142 card. Figure 8 exhibits real time steady state waveforms in traditional PI-MPC built DSTATCOM. Figures 8(a) and 8(b) deliberate load current behavior before and after compensation. The waveform generated for compensation of harmonics is depicted in Figure 8(c). Accordingly, the stabilization action of DC-capacitor voltage is maintained in Figure 8(d). As a result, the phase correlation between supply voltage and supply current gets improved (Figure 8(e)) and a significant reduction of THD (from 25.76% to 3.04%) is perceived in Figure 8(f). It is apparent from Figure 8 that the response curves are very nearer to simulation outcomes illustrated in Figure 5.
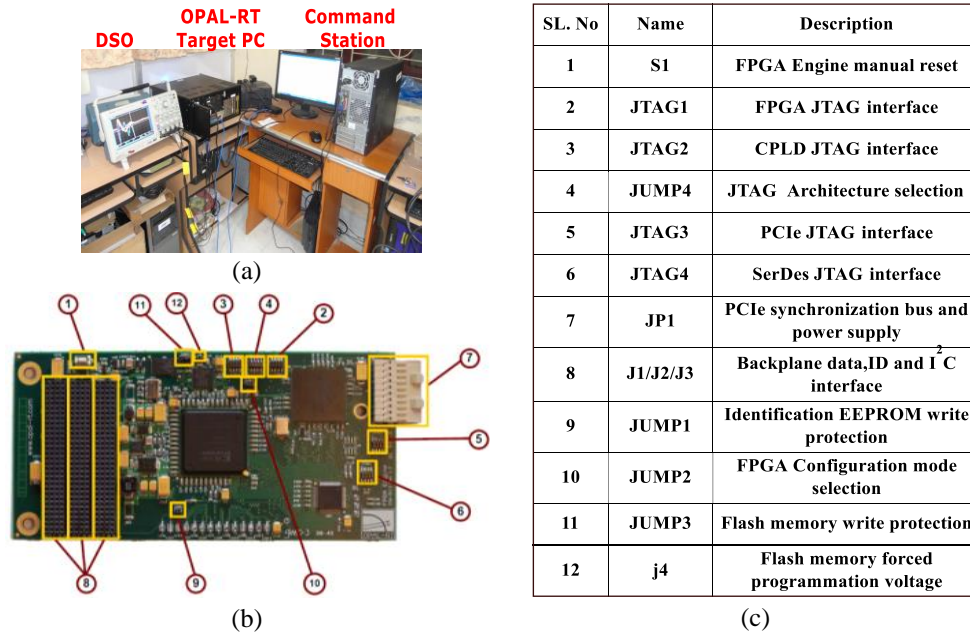

(a)

SL. No	Name	Description
1	S1	FPGA Engine manual reset
2	JTAG1	FPGA JTAG interface
3	JTAG2	CPLD JTAG interface
4	JUMP4	JTAG Architecture selection
5	JTAG3	PCIe JTAG interface
6	JTAG4	SerDes JTAG interface
7	JP1	PCIe synchronization bus and power supply
8	J1/J2/J3	Backplane data,ID and I^{2}C interface
9	JUMP1	Identification EEPROM write protection
10	JUMP2	FPGA Configuration mode selection
11	JUMP3	Flash memory write protection
12	j4	Flash memory forced programmation voltage

(b)   (c)

Figure 7. Setup for experimenting with Opal-RT: (a) RTDS-hardware set up, (b) outline of OP5142, and (c) connectors-OP5142

(a)   (b)   (c)

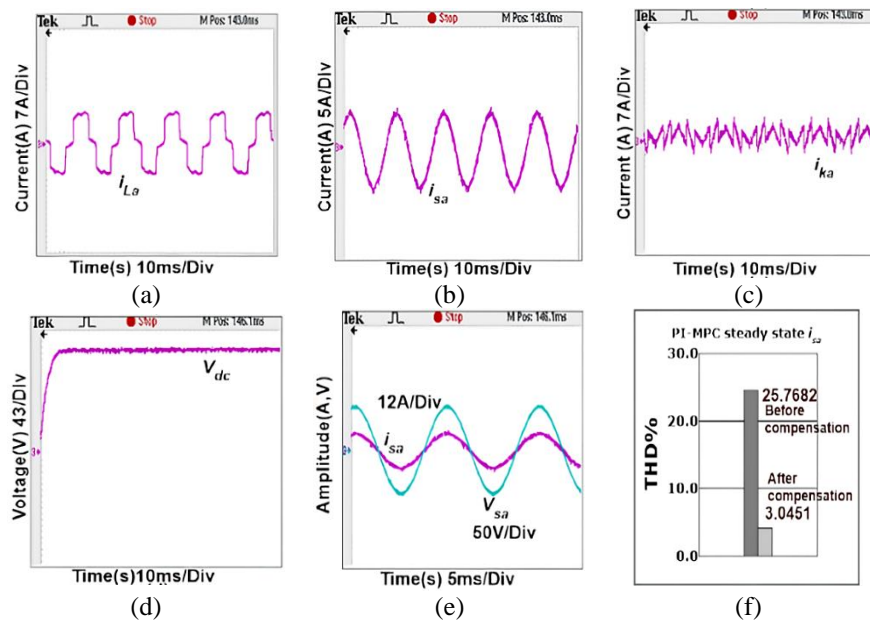(d)   (e)   (f)

Figure 8. Real time results (steady state) for PI-MPC built MPC: (a) phase-a supply-current prior compensation, (b) phase-a supply-current post compensation, (c) phase-a compensating-current, (d) DC-capacitor voltage, (e) phase-a unity power-factor, and (f) THD of phase-a supply current prior and post compensation

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Figure 9 presents real time steady state outcomes in case of proposed Adaline-MPC based DSTATCOM. Figures 9(a) and 9(b) demonstrate the load current's outcome meant for prior and post compensation respectively. The arisen compensation current is shown in Figure 9(c) to neutralize the harmonics in load current. Moreover, the stabilization outcome of DC-capacitor voltage and phase correlation outcome between supply voltage and supply current are clearly evident from Figures 9(d) and 9(e) correspondingly. As a consequence, THD is lessened notably from 25.76% to 2.92% as observed in Figure 9(f). The aforementioned outcomes remain almost similar with the simulation outcomes as revealed within Figure 6. Thus, it is realized that following compensation, the supply current has a lower level of distortion, and the DC-capacitor voltage quickly stabilizes towards the reference line.

The performance indicators, for instance THD, power factor, active as well as reactive power have been analyzed in Table 2 employing both conventional and proposed approach. Moreover, the DC-capacitor voltage constraints such as rise time, settling time, peak time, peak voltage, peak overshoot and undershoot have been summarized in Table 3. The proposed Adaline-MPC based DSTATCOM system has been evaluated to be better as observed through Tables 2 and 3.
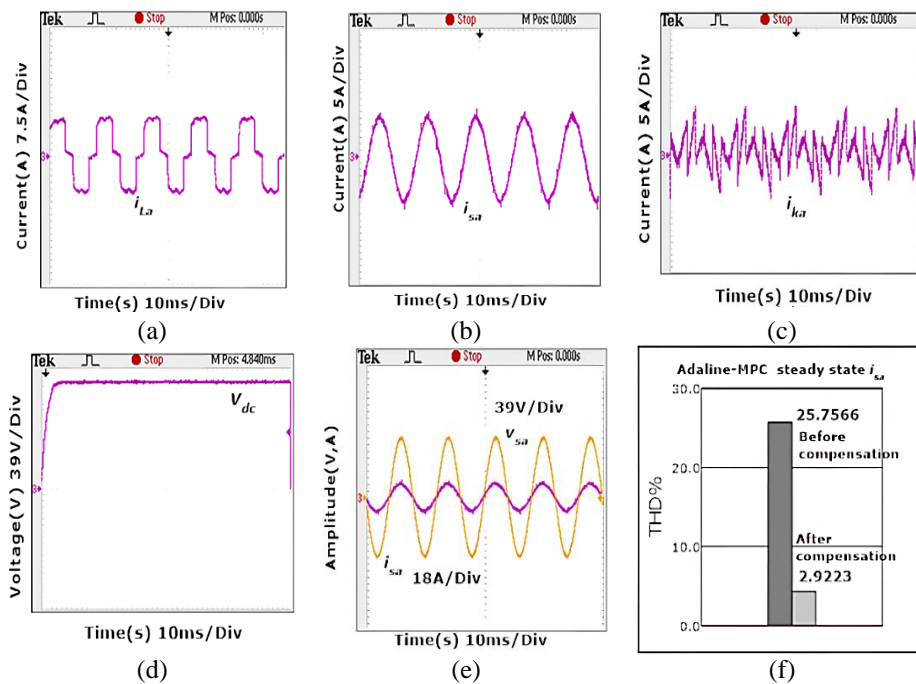

Figure 9. Real time results (steady state) for proposed Adaline-MPC built DSTATCOM: (a) phase-a supply-current prior compensation, (b) phase-a supply-current post compensation, (c) phase-a compensating-current, (d) DC-capacitor voltage, (e) phase-a unity power-factor, and (f) THD of phase-a supply current prior and post compensation

Table 2. Phase-a performance indicators and measurements

DSTATCOM	THD%		Prior to compensation, active power, reactive power, and power-factor			Post compensation of active power, reactive power, and power-factor		
	i_{La}	i_{sa}	p_a	q_r	pf	p_a	q_r	pf
Traditional PI MPC	25.7682	3.0454	248	24	0.9953	267.5	0.6	1
Proposed Adaline MPC	25.7566	2.9223	247	24	0.9953	266	0.1	1

Table 3. Time-dependent DC-capacitor voltage

Control structure of DSTATCOM	Rise-time in seconds	Settling-time in seconds	Percentage of overshoot	Percentage of undershoot	Peak in volts	Peak-time in seconds
PI based MPC	0.0084	0.0141	0.3878	3.3505E-003	140.3364	0.0658
Adaline based MPC	0.0078	0.0132	0.2018	3.2191E-004	137.5431	0.1757

6. CONCLUSION

In this study, a DSTATCOM system built upon Adaline-MPC has been suggested. The leading benefit behind this approach is straightforward application of switching pulses towards the IGBTS while avoiding modulators. Additionally, a comparative assessment of the suggested system's performance is carried out in steady state situation to investigate its efficacy. Evidence from both simulation and real-time testing shows that the suggested Adaline-MPC built DSTATCOM reveals an exceptional control methodology which advances power quality more effectually via harmonic mitigation, power factor correction and speedy DC-capacitor voltage stabilization above conventional PI-MPC.

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