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Power quality conditioning using two-level buck inverter based DSTATCOM

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ABSTRACT

A two-level buck inverter is derived from the voltage source inverter, by replacing the additional power devices and suitable combination of inductor circuits respectively. Novel isolated buck inverter, featuring each-phase conversion and soft-switching within wide operation range, is developed. An optimized control strategy is employed to realize isolated buck conversion. By utilizing the buck inverter, the voltage stress on the power devices and passive components, the self-supported capacitor and filter inductance, is reduced to the half of the output voltage. Moreover, it is proven that the thyristor-controlled series capacitor (TCSC) equipped with a well-designed distributed static compensator (DSTATCOM) can effectively improve source current harmonics reduction, power factor correction in the source side, load compensation, regulation of load voltage and upholding constant voltage across the DC-link capacitor. In order to verify the effectiveness of the proposed DSTATCOM, its performance is compared with the two level DSTATCOM. The extensive simulations are carried out using MATLAB/Simulink to analyze the results. Experimental results using dSPACE-1104 prototype verify the appropriate DSTATCOM.

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1. INTRODUCTION

In point of common coupling (PCC), the proper sharing of both real and reactive power can be made by tapping suitable custom power devices (CPD) to maintain the power quality (PQ) [1]–[4]. Including this, the fixed as well as variable cost of the CPD should be incurred less in order to maintain the same overall cost of the distribution system [5]–[7]. Finally, the proposed CPD may be chosen as the best solution for the utility suppliers and consumers.

Among all varieties of CPD, distributed static compensator (DSTATCOM) is common types of shunt compensator [8]–[10]. In view of improved design aspect, the LC coupled buck voltage source inverters (VSI) based DSTATCOM is proposed for providing the actual and reactive power in the PCC for the PQ improvement [11], [12]. This buck inverter is designed by considering the aspect of modular design, suitable selection of inductor, variable output power, and flexible for additional connection of the elements [13]–[15]. Apart from these, the variable switching frequency can be attained by using this proposed inverter. Most important of all, it does not possess shoot through problems as happens in conventional VSI [16]–[19].

The literature has recently provided a comprehensive review on various types of inverters. In particular, DSTATCOM is considered as the cased study for power quality (PQ) analysis. Keeping in the view of further improvement, buck inverter topology is proposed.

To control LC-DSTATCOM, preliminary care has been taken for the design of inductor and capacitor to reduce the steady-state error. Therefore, this paper proposes an LC-DSTATCOM, which can maintain supply active power with all other power quality (PQ) solution, which furthermore reduces the input voltage of the inverter part. Subsequently, the initial cost and switching noise are minimized. Hence, LC-DSTATCOM is expected to provide better compensation for a wide range of unbalanced conditions as compared to the other solutions.

Yet, different types of conventional and adaptive control algorithms are developed for VSI based DSTATCOM. But, considering the advantages of faster convergence, less output error, tuned weight behavior and better tracking capability, adaptive least mean square algorithm (ALMS) was interfaced for the LC coupled buck VSI based DSTATCOM [20]–[22]. Finally, automatic adjustment for the weight gain required for the switching signals are utilized for the improved DSTATCOM for PQ improvement. Finally, the PQ performance for the different loading conditions is maintained as per IEEE 519-2017 and IEC-41000 guideline [23]–[25]. The proposed LC-DSTATCOM is a cost-effective solution and provides better source current harmonics reduction, power factor correction in the source side, load compensation, regulation of load voltage and upholds constant voltage across the DC-link capacitor. To analyze the performance, the experimental study is analyzed by using dSPACE 1104 [26]–[30]. This ALMS technique is utilized to track the load current and simultaneously perform the weight updating process using learning rule which also performs smooth operation for the real time implementation.

The design considerations of controller for the proposed inverter are explained in sections 2 to 4. Section 4 describes about the experimental analysis under various state of the loading. Finally, the summary of the research is presented in the section 5. The detailed description of this research study is presented in the subsequent section.

2. DESIGN OF THE PROPOSED DSTATCOM

The schematic diagram of the DSTACOM is shown in the Figure 1. It can be observed that this structure consists of conventional power distribution utility and uncontrolled bridge rectifier with R and L load. This load is regarded as nonlinear steady state and dynamic load based upon the switching operation.

The VSI utilized for the DTATCOM is shown in Figure 2, which also consists of DC link capacitor and interfacing inductor. Finally, the LC coupled DSTATCOM system is shown in the Figure 3. The dynamic assessment on power quality under the different loading is explained in subsequent section.

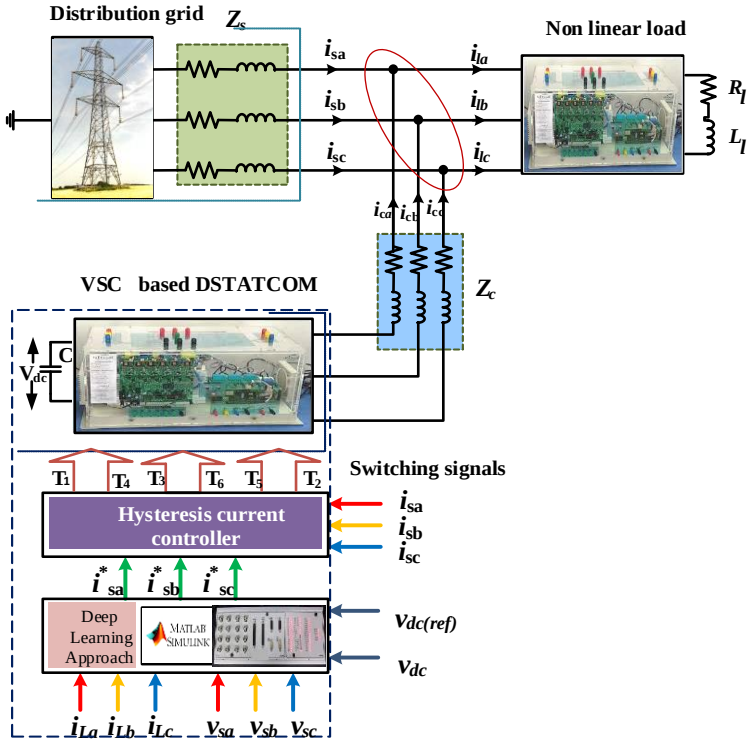


Figure 1. Schematic diagram for DSTATCOM with distribution system

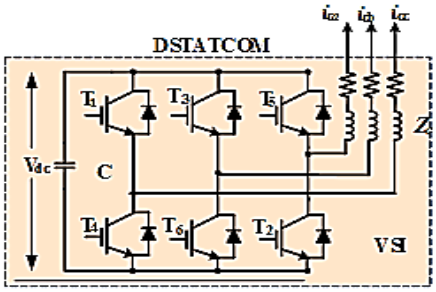


Figure 2. Two level VSC

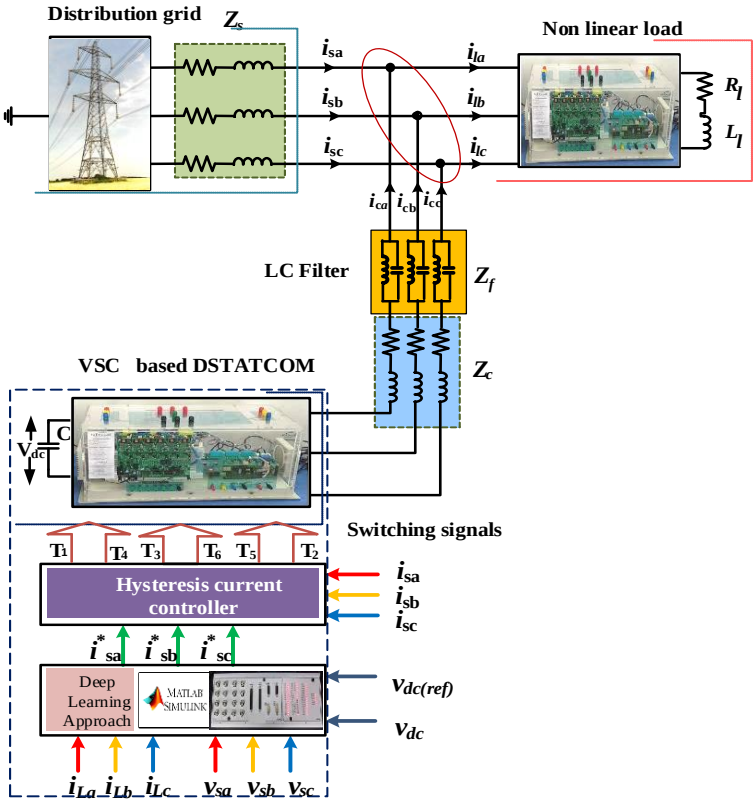


Figure 3. Schematic diagram for LC coupled DSTATCOM system

2.1. Understanding of the controller

2.1.1. ALMS control algorithm

ALMS algorithm is implemented considering the various parameters like load current, step size, learning rate, initial weight and bias. These parameters are utilized in the learning rules used in this algorithm to generate the switching signals required for the proposed inverter. The complete ALMS algorithm is shown in the Figure 4.

Finally, the complete procedure is presented by using mathematical equation from (1) to (20). The weights of the active and reactive parts of the load current are listed:

$$w_{pa}(n) = \alpha\gamma\{i_{la}(n) - w_{pa}(n-1)u_{pa}(n)\}u_{pa}(n) + w_{pa}(n-1) \quad (1)$$

$$w_{pb}(n) = \alpha\gamma\{i_{lb}(n) - w_{pb}(n-1)u_{pb}(n)\}u_{pb}(n) + w_{pb}(n-1) \quad (2)$$

$$w_{pc}(n) = \alpha\gamma\{i_{lc}(n) - w_{pc}(n-1)u_{pc}(n)\}u_{pc}(n) + w_{pc}(n-1) \quad (3)$$

$$w_{qa}(n) = \alpha\gamma\{i_{la}(n) - w_{qa}(n-1)u_{qa}(n)\}u_{qa}(n) + w_{qa}(n-1) \quad (4)$$

$$w_{qb}(n) = \alpha\gamma\{i_{lb}(n) - w_{qb}(n-1)u_{qb}(n)\}u_{qb}(n) + w_{qb}(n-1) \quad (5)$$

$$w_{qc}(n) = \alpha\gamma\{i_{lc}(n) - w_{qc}(n-1)u_{qc}(n)\}u_{qc}(n) + w_{qc}(n-1) \quad (6)$$

the average weight (w_a) and reactive component (w_r) was calculated:

$$w_a = \frac{w_{pa}+w_{pb}+w_{pc}}{3} \quad (7)$$

$$w_r = \frac{w_{qa}+w_{qb}+w_{qc}}{3} \quad (8)$$

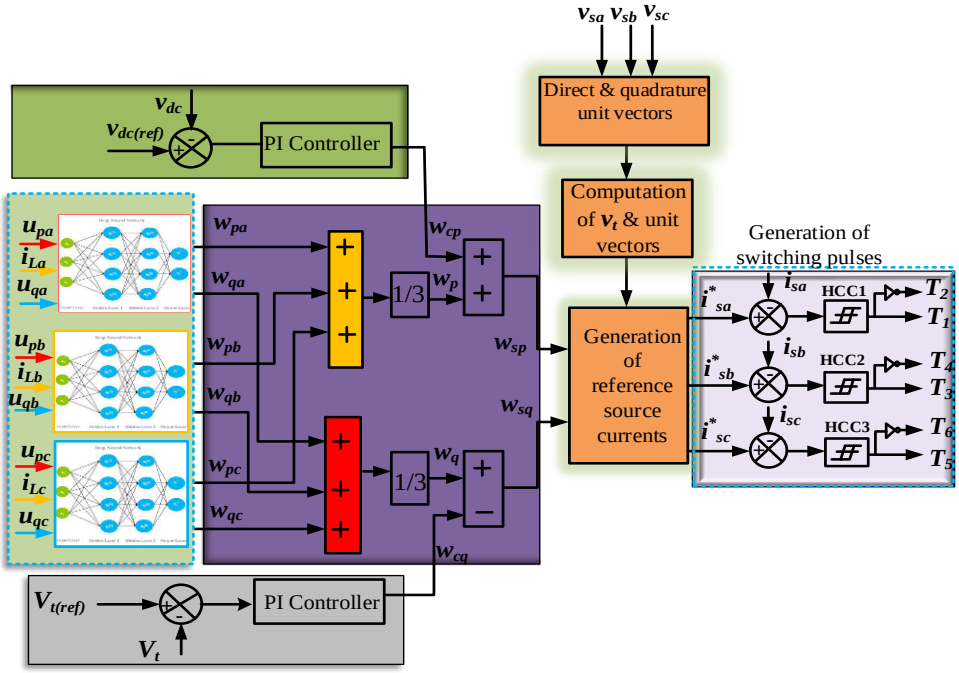


Figure 4. Control structure of ALMS learning

2.1.2. Computation of active and reactive unit voltage template

The voltages of active and reactive templates are approximated as:

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \quad (9)$$

$$u_{qa} = \frac{u_{pb}+u_{pc}}{\sqrt{3}}, u_{qb} = \frac{3u_{pa}+u_{pb}-u_{pc}}{2\sqrt{3}}, u_{qc} = \frac{-3u_{pa}+u_{pb}-u_{pc}}{2\sqrt{3}} \quad (10)$$

where v_t can be expressed as (11).

$$v_t = \sqrt{\frac{2(v_{sa}^2+v_{sb}^2+v_{sc}^2)}{3}} \quad (11)$$

2.1.3. Active component of reference source currents

The difference in between reference and actual DC link voltage is regarded as the error voltage which is processed through the DC side PI controller to find out the active component used for the reference source current.

$$v_{de} = v_{dc\,(ref)} - v_{dc} \quad (12)$$

$$w_{cp} = k_{pa}v_{de} + k_{ia}\int v_{de}dt \quad (13)$$

The reference source current active component is calculated as (14).

$$w_{sp} = w_a + w_{cp} \tag{14}$$

2.1.4. Reactive component of reference source currents

The difference in between reference and actual AC voltage is regarded as the error voltage which is processed through the AC side PI controller to find out the reactive component used for the reference source current. The AC voltage error (v_{te}) is represented as:

$$v_{te} = \ v_{t\,(ref)} - v_t \tag{15}$$

$$w_{cq} = k_{pr} v_{te} + \ k_{ir} \int v_{te} dt \tag{16}$$

$$w_{sq} = w_r - w_{cq} \tag{17}$$

2.1.5. Switching pulses generation

The relation between unit voltage template and weighting component of both active and reactive component of reference source current hold the following relation which are (18) and (19).

$$i_{aa} = w_{sp} u_{pa}, i_{ab} = w_{sp} u_{pb}, i_{ac} = w_{sp} u_{pc} \tag{18}$$

$$i_{ra} = w_{sq} u_{qa}, i_{rb} = w_{sq} u_{qb}, i_{rc} = w_{sq} u_{qc} \tag{19}$$

Finally, the total reference source currents are determined by (20).

$$i_{sa}^* = i_{aa} + i_{ra}, i_{sb}^* = i_{ab} + i_{rb}, i_{sc}^* = i_{ac} + i_{rc} \tag{20}$$

3. SIMULATION ANALYSIS

In order to analyze the simulation results, ALMS control strategy on a DSTATCOM and LC coupled buck inverter based DSTATCOM is presented by using MATLAB/Simulink. The source current, compensating and load current ALMS control strategy on a DSTATCOM and LC coupled buck inverter based DSTATCOM are illustrated in Figures 5(a)-5(f) and Figures 6(a)-6(f) corresponding to different loading conditions respectively. The source, compensator and load current are 56 A, 25 A, and 51 A is maintained during balanced conditions using ALMS technique based DSTATCOM as shown in the Figures 5(a)-5(c). As expected, the source current remains balanced and resulted sinusoidal component as shown in the Figure 5(a). Moreover, the compensator current varies from 0 to 25 A which aggregates the filtering performance of the DSTATCOM caused to inject in the distribution grid as shown in the Figure 5(b). It is worth noting that the load current, which remains same as before DSTATCOM used. Also, create the lagging p.f with the supply voltage due to distorted behavior as shown in the Figure 5(c).

Similarly, the source, compensator and load current are 52 A, 45 A, and 51 A is maintained during unbalanced conditions using ALMS technique based DSTATCOM as shown in the Figures 5(d)-(f). In this Figure 5(d), the magnitude of the source current is reduced but maintained sinusoidal. Due to switching of the a-phase load increase in filter current shown in the Figure 5(e). Also, the corresponding load current for three phases are shown in the Figure 5(f).

Similarly, the source, compensator and load current are 54 A, 22 A, and 51 A is maintained during balanced conditions using ALMS technique-based LC coupled DSTATCOM as shown in the Figures 6(a)-6(c). As expected, the source current remains balanced and resulted sinusoidal component in the Figure 6(a). Moreover, the compensator current varies from 0 to 20 A which aggregates the filtering performance of the DSTATCOM in the Figure 6(b). It is worth noting that the load current shown in the in the Figure 6(c) which remain same as before the proposed DSTATCOM used. In this same way, the following unbalanced loading is explained for this proposed system. Hence, the source, compensator and load current are 52 A, 44 A, and 51 A is maintained during unbalanced conditions using ALMS technique based DSTATCOM as shown in the Figures 6(d)-6(f). In this Figure 6(d), the magnitude of the source current is reduced but maintained sinusoidal. Due to switching of the a-phase load increase in filter current shown in the Figure 6(e). Also, the corresponding load current for three phases are shown in the Figure 6(f).

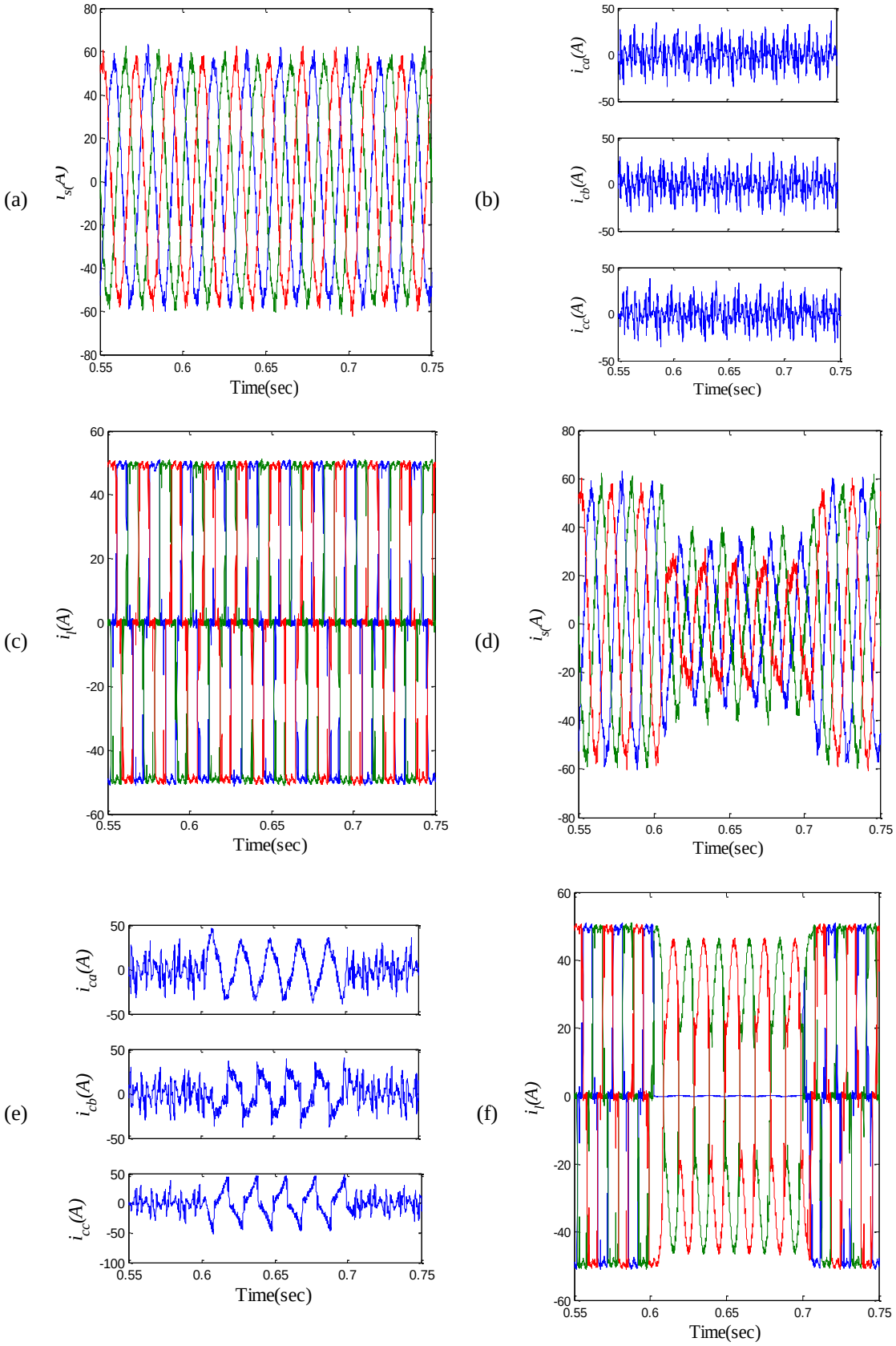


Figure 5. Simulation waveform of source current, compensator current, and load current using ALMS control technique based DSTATCOM (a) the source current, (b) the compensator current, (c) create the lagging p.f, (d) the source current, (e) load increase in filter, and (f) load current for three phases

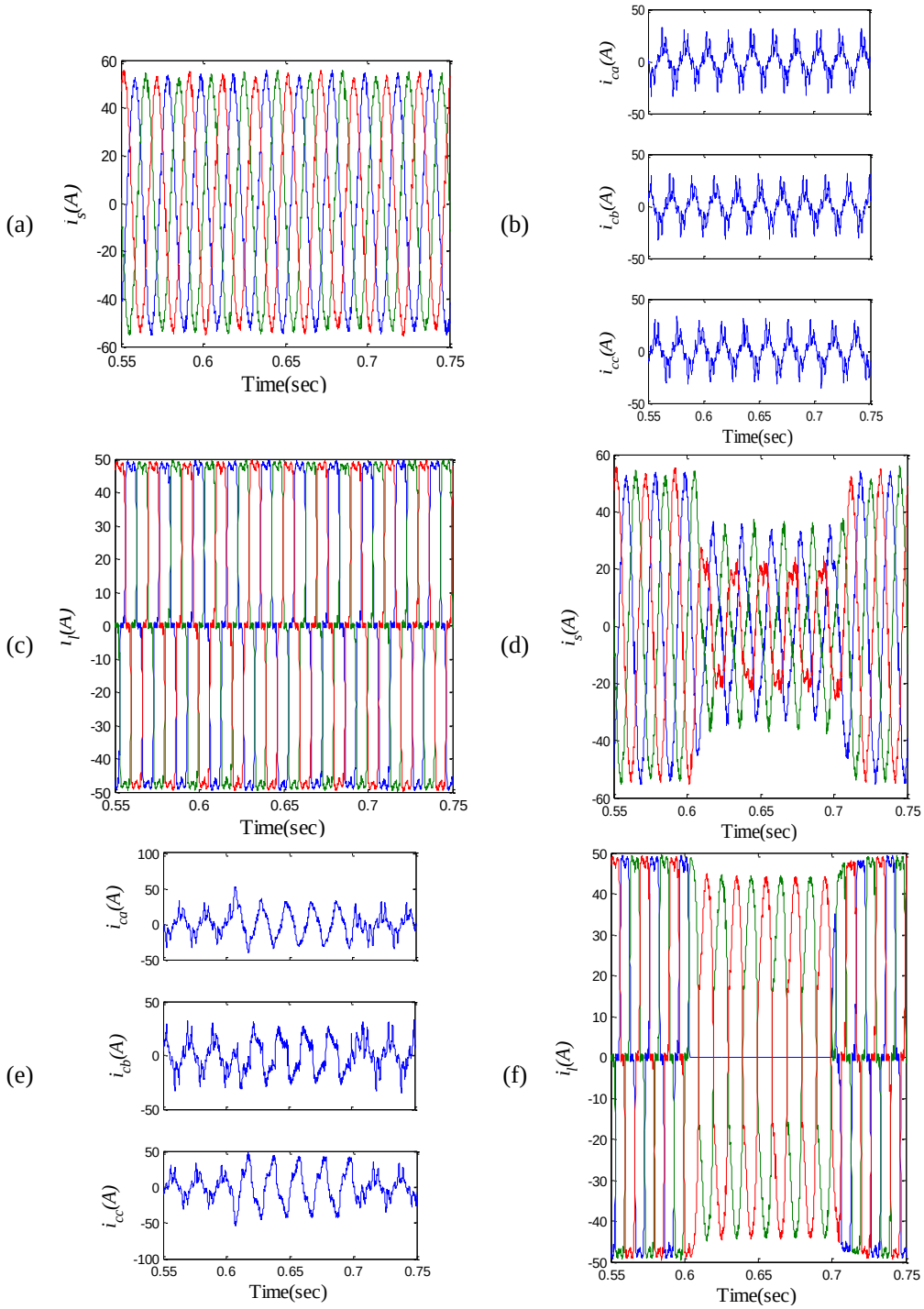


Figure 6. Simulation waveform of source current, compensator current and load current using ALMS control technique-based LC coupled DSTATCOM (a) resulted sinusoidal component, (b) the compensator current varies, (c) the load current, (d) the magnitude of the source current is reduced, (e) load increase in filter, and (f) load current for three phases

4. EXPERIMENTAL ANALYSIS

The experimental test bench is realized shown in Figure 7, configuration system parameters used in experiment set up of the ALMS based LC-DSTATCOM are given by Table 1. This experimental testing system is utilized to validate the ALMS control strategy on a DSTATCOM and LC coupled DSTATCOM. Simulink is used to implement the control strategy before being applied to a programmable processor type dSPACE-1104 by automatic code generation [29]–[35]. The power module switches of the buck inverter adopted IGBTs (Inneon BSM50GB60DLC). Digital storage oscilloscope (scientific DSO-5100) to analyze

the wave form with sampling time 20 µs and voltage scale (200 V/div) and current scale (25 A/div), The remaining part of the experimental analysis detailed is presented in the sub's sections.

The source, compensator and load current during balanced and unbalanced loading conditions using ALMS technique based DSTATCOM as shown in the Figures 8(a)-8(f) respectively. The source current has contributed significant performance whose magnitude 56 A which is in phase with grid voltage as shown in the Figure 8(a). The corresponding compensator 25 A which is injected by the DSTATCOM at the grid as shown in Figure 8(b). Finally, the distorted nonlinear load current 51 A is shown in the as shown in the Figure 8(c). Similarly, the source current has contributed significant performance whose magnitude 56 A which is in phase with grid voltage as shown in Figure 8(d). The corresponding compensator 25 A which is injected by the DSTATCOM at the grid as shown in Figure 8(e). Finally, the distorted nonlinear load current 51 A is shown in the as shown in the Figure 8(f).

Table 1. Simulation and experimental data

Notation	Description	Value
v_s	Source voltage	230 V/phase
f_s	Frequency	50 Hz
C_{dc}	Capacitor	2000 µF
K_{ir}	AC Integral controller	1.1
R_c	VSC resistance	0.25 Ω
L_s	Source inductance	2 mH
R_s	Source resistance	0.5 Ω
K_{pr}	AC Proportional controller	0.2
K_{pa}	DC Proportional controller	0.01
L_c	VSC inductance	1.5 mH
v_{dc}	DC link voltage	600 V
K_{ia}	DC Integral controller	0.05

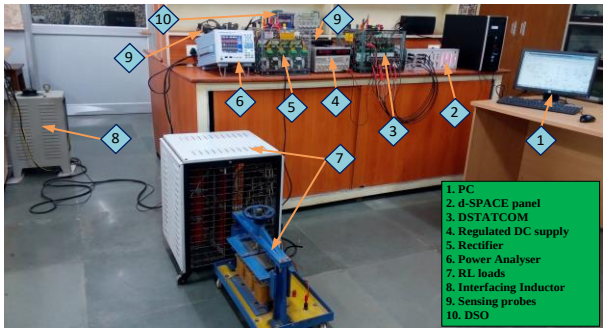


Figure 7. Hardware setup of the ALMS based LC-DSTATCOM

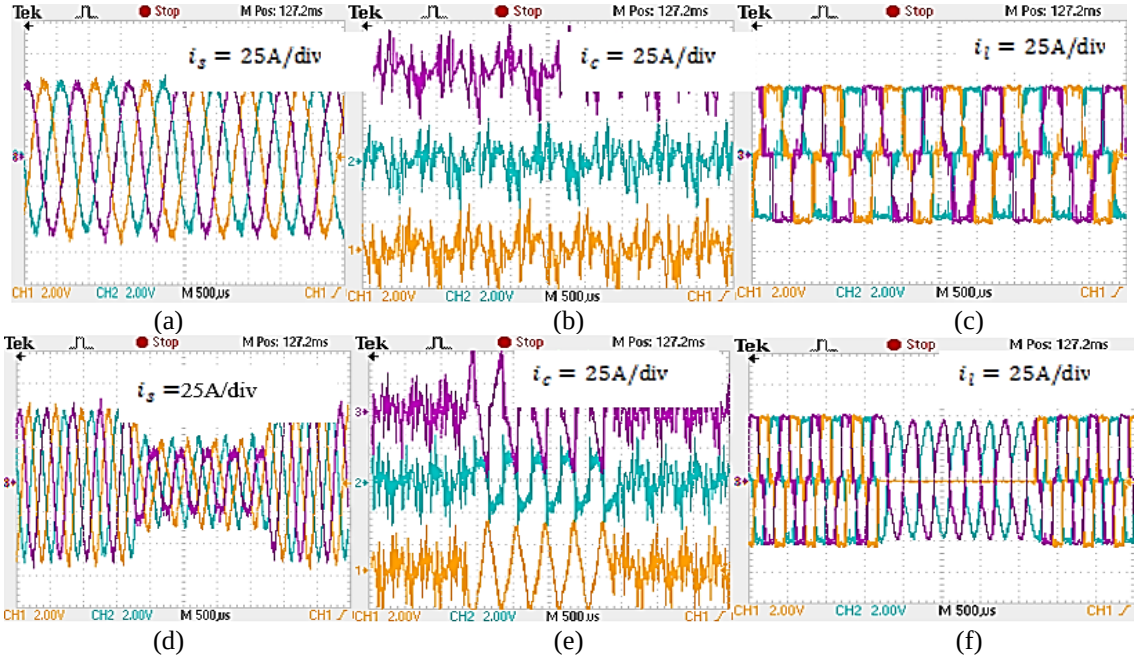


Figure 8. Experimental waveform of source current, compensator current, and load current using ALMS control technique (a) the source current, (b) the corresponding compensator 25 A, (c) the distorted nonlinear load current 51 A, (d) the source current, (e) the corresponding compensator 25 A, and (f) the distorted nonlinear load current 51 A

The source, compensator and load current is maintained during balanced and unbalanced loading conditions using ALMS technique-based LC coupled DSTATCOM as shown in Figures 9(a)-9(f) respectively. The source current has contributed significant performance whose magnitude 56A which is in

phase with grid voltage as shown in the Figure 9(a). The corresponding compensator 25 A which is injected by the DSTATCOM at the grid as shown in Figure 9(b). Finally, the distorted nonlinear load current 51 A is shown in the as shown in Figure 9(c). Similarly, the source current has contributed significant performance whose magnitude 52 A which is in phase with grid voltage as shown in the Figure 9 (d). The corresponding compensator 22 A which is injected by the DSTATCOM at the grid as shown in Figure 9(e). Finally, the distorted nonlinear load current 51 A is shown in the as shown in the Figure 9(f). Owing to the source side compensation principle, the real time implementation of proposed technique based DSTATCOM is realized as a better solution for the power quality improvement in terms of source side power factor correction, THD reduction, voltage regulation and voltage balancing. But, load current magnitude and THDs (in %) obtained from experimental results are presented in Figure 10 which is maintained same for all conditions.

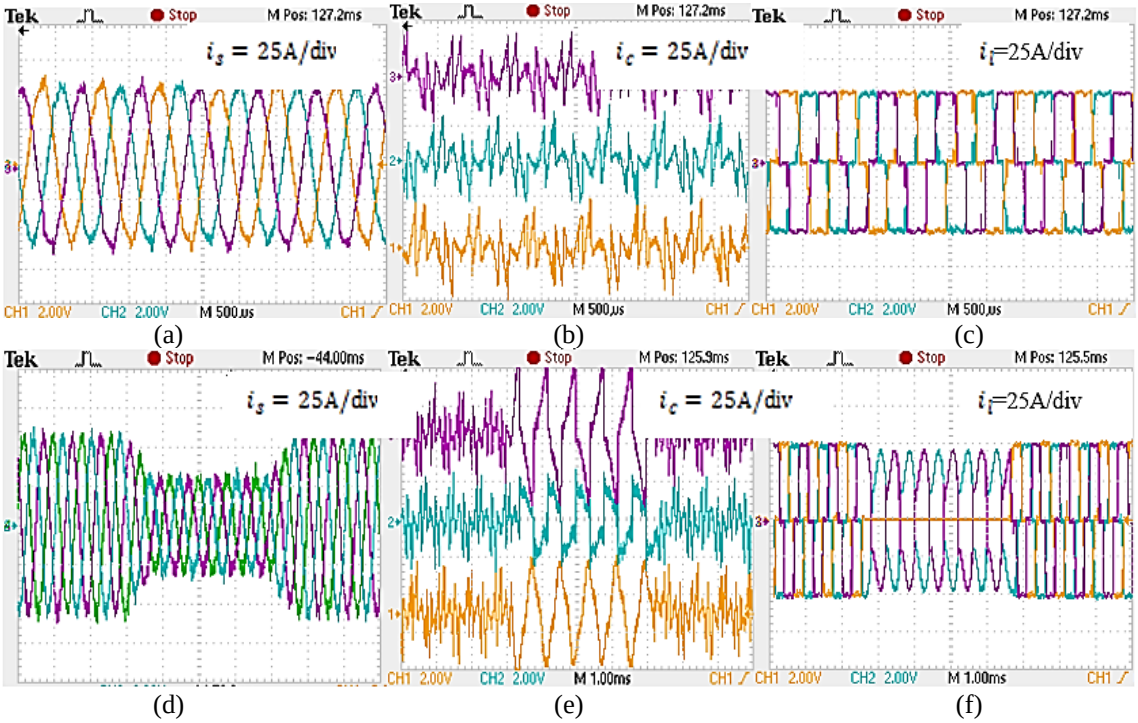
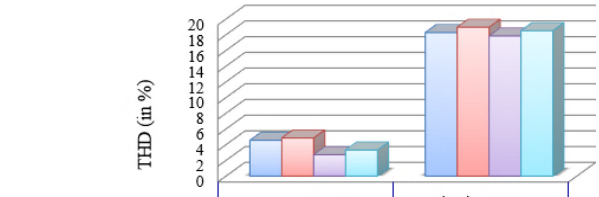


Figure 9. Experimental waveform of source current, compensator current and load current using ALMS control based proposed technique (a) the source current, (b) the corresponding compensator 25 A, (c) the distorted nonlinear load current 51 A, (d) the source current, (e) the corresponding compensator 22 A, and (f) the distorted nonlinear load current 51 A



	source current	load current
ALMS based DSTATCOM under constant loading [20]	4.56	18.28
ALMS based DSTATCOM under diversity loading [20]	4.85	18.96
ALMS based LC coupled DSTATCOM under constant loading	2.72	17.84
ALMS based LC coupled DSTATCOM under diversity loading	3.32	18.51

Figure 10. Source and load current THDs (in %) obtained from experimental analysis

5. CONCLUSION

This research study described about PQ conditioning using two-level buck inverter based DSTATCOM. The buck inverter based DSTATCOM using ALMS algorithm has been studied in detail for better shunt compensation. Finally, the experimental studies are analyzed using the real time dSPACE experimental set ups. The theoretical as well as hardware analysis indicated for shunt compensation for such condition as required by IEEE 1547. Hence, evaluated studies can be considered for further better analysis in other applications.

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