Nine level switched capacitor inverter with level shifted pulse width modulation approach

Vijayakumar Arun¹, Thunga Nageswara Prasad¹, Sundaramoorthy Prabhu¹, Nagarajan Ashokkumar²

¹Department of Electrical and Electronics Engineering, School of Engineering, Mohan Babu University, Tirupati, India ²Department of Electronics and Communication Engineering, School of Engineering, Mohan Babu University, Tirupati, India

Article Info	ABSTRACT
Article history: Received May 26, 2023 Revised Aug 8, 2023 Accepted Aug 31, 2023	This article proposes a nine-level switched capacitor inverter (NLSCI) with a minimum number of switches. In recent years, switching capacitor (SC) multilevel inverters (MLIs) have become one of the most common inverter topologies. These proposed nine level switched capacitor inverter (NLSCI) do not deserve any external control unit for capacitor control. Since, the charging and discharging of the capacitors are controlled by the on and off
<i>Keywords:</i> Inverter MLI NLSCI POD	states of switches. Furthermore, by employing fewer switches and DC voltage sources, the suggested design produces a greater amount of resultant voltage. Additionally, pulse width modulation (PWM) is recommended as a method to enhance output quality and power level quality. The switched-capacitor two-output multilevel inverter (SCMLI) structure's viability and effectiveness have been demonstrated using MATLAB simulation.
SPWM THD	This is an open access article under the <u>CC BY-SA</u> license.
Corresponding Author:	
Vijayakumar Arun Department of Electrical and Electro	nics Engineering, School of Engineering, Mohan Babu University

Tirupati, India Email: varunpse@yahoo.com

1. INTRODUCTION

A switching capacitor (SC) circuit facilitates the generation of a DC voltage waveform having multiple levels, which can be employed to a drive a full-bridge inverter. The optimized inverters in [1], can produce an output waveform with similar total harmonic distortion (THD) as conventional multilevel inverters but with a lower count of circuit elements. The fundamental switching frequency multilevel inverters have a special feature of low switching loss because very few power device commutations take place during one cycle of the output voltages, whereas the staircase waveforms have an additional level to achieve low harmonic distortion [2]. In comparison with the conventional voltage-balancing circuit diodeclamped five-level inverter is capable of decreasing its inductor to one tenth in volume [3]. The architecture of the multilevel circuit based on the switched capacitor converter and diode clamped converter can converted to any type of n-level converter and can proficiently use in three-phase system. The SC circuit supports to generate the output voltage level and balance the voltage of dc link capacitors and flying capacitors under any load circumstances [4]. By using switched capacitor, a charge pump is capable of creating voltage that is higher than the incoming voltage. The charge pump creates a combination of the input voltage supply and the capacitor voltages [5]. It is suggested to use an innovative switched-capacitor layout and H-bridge backend to build a cascaded multilevel inverter (MLI). The SC will enhance the number of different voltages through the conversion of series and parallel connections, and the output harmonics and component counter can be minimized by a rising variety of voltage levels [6].

Electric vehicles (EVs) also have electric motor drive systems that transform electric power using power converters like pulse width modulation (PWM) inverters and DC/DC converters [4], [5]. Inverter

technology performs a major part in these networks [7]. In further to the proposed design, simple techniques can be used to balance the capacitor voltage. The hybrid source SC layouts can be employed in PV systems and electric car applications [8]. The quantity of SC cells determines how many output stages are present. The issue of capacitor voltage balancing is also addressed in [9], and only one DC voltage source is required. In [10], the proposed SCC unit is used in alternate arrangement as a stateful multi-layer inspection (SMLI) and then in each SMLI unit rather than using a full H-bridge cell, which helps to reduce the overall cost by using fewer switches. Without the help of a voltage or current sensor, a straightforward pulse width modulator built on logic-form equations is created to keep the FC voltage at its reference value. So, the layout recommended can be controlled with very little complexity [11]. This structure can be used where the DC input sources are un-even. As the voltage sources are not stacked in series, voltage balancing is not required in this configuration. For example, in case of the ac micro grids based on renewable energy sources and present-day electric vehicles, the harmonic content in the waveform is evaluated and found to be very little [12]. In order to increase system stability and standardize the control technique in [13], the topology consists of DC-DC and DC-AC steps with a separate controller for each stage. A single-stage switchedcapacitor module (S3CM) technology for cascaded MLI assures that the peak inverse voltage across all switches exists within the DC source voltage [14].

Switched-capacitor single-source CMI (SCSS-CMI) is the title provided to the suggested layout, which substitutes some capacitors for the DC sources. Typically, a SC cell's capacitor charging method is followed by some current surges that seriously damage both the capacitor and the charging switch and also it offers the zero-current switching condition for the charging switch [15]. This modulation method generates high rms voltage and the minimum THD. This kind of configurations are generated in the nine-level CSCMLI with single DC source and two capacitors [16]. A collection of multiport switched-capacitor twooutput multilevel inverter (SCMLI) uses asymmetric dc voltage sources with a common ground, making it perfect for use in solar energy farms and contemporary electric cars [17]. There are two improved switchedcapacitor integrated MLI designs, they resolve the high voltage pressure issue that their counterparts. Additionally, it has plenty of benefits, such as a decrease in the amount of DC sources and an increase in the voltage boosting gain [18]. The major benefits of this structure are a smaller number of switches and capacitors with the capable of boosting. To determine whether the converter can be used for high-power applications, an efficiency factor for capacitor usage is specified. Without using an output filter, the converter has a high efficiency (>90%) and a low THD (3.7%). Due to these characteristics, both standalone and gridconnected PV systems can use the suggested converter [19]. A brand-new SC-based MLI structure is suggested, along with related mixed PWM modulation methods. Two half-bridge modular SC circuits are organized on the left and the right corners of the dc input source which have a high rate of efficiency with a maximum value over 97% [20]. In [21], discusses a family of novel enhanced-boost quasi-Z-source inverters. In [22], a configuration using series-connected switched DC sources along with an optimized H-bridge circuit is presented, providing a comprehensive analysis of the operating modes and modelling process of the proposed converter. An interesting aspect of this design is that it eliminates the need for DC-link capacitors. In [23], a new inverter topology is proposed, specifically tailored for renewable energy and fuel cell applications that require high magnitude output AC voltage. The use of switched capacitors in [24] enables efficient voltage boosting without the necessity for additional boost DC-DC converters. The topology presented in [25] demonstrates the ability to produce thirteen voltage levels using a single DC source, highlighting its voltage boosting and self-balancing features, making it a promising solution for high magnitude output AC voltage needs.

The objective of this paper is to present an innovative inverter configuration employing the switched-capacitor technique. The primary focus lies in leveraging a single DC voltage source, thus eliminating the necessity for extra diodes and floating capacitors. By employing just 11 switches and two capacitors, this configuration can produce up to nine distinct voltage states. Additionally, it ensures a voltage gain twice that of the input voltage, while also guaranteeing self-balancing of the switched capacitor voltage. Furthermore, it effectively reduces the voltage rating of the switching elements. This paper proposed and describes a nine level switched capacitor inverter (NLSCI) with eleven switch, two capacitors and a DC source. The simulations were performed using MATLAB/Simulink.

2. NLSCI CIRCUIT TOPOLOGY

The suggested nine level switched capacitor inverter (NLSCI) is shown in Figure 1. This topology minimizes the total number of sources in the circuit by managing the capacitor charging and discharging. The capacitors can self-balance by controlling with the parallel and series mode. By employing this characteristic of the SC structure, we can able to avoid the supply of extra power. This topology uses switched capacitors and PWM to generate a multi-level output voltage. It consists of DC voltage sources, capacitors, electrical switches, control circuits, and auxiliary bidirectional switches. Different voltage levels are produced by

switching the capacitors, and the power switches are modulated by level shifted - sinusoidal PWM (LSPWM) signals. This topology provides high-quality output voltage with low harmonic distortion, making it suitable for various applications. It can output nine levels of voltage (± 2 Vdc, ± 1.5 Vdc, ± 0.5 Vdc, \pm Vdc, and 0 Vdc) determined by the polarity conversion circuit's switching components.

The operational states of various devices are mentioned in Table 1, including the on and off phases of power switches and the charging and discharging states of capacitors. The functioning modes of switches are indicated by 1/0, and the charging, discharging, and idle states of capacitors are denoted by "C", "D," and "-," respectively. Figures 2(a)-2(i) shows the nine-level inverter's current paths, with the forward current path represented by the Plum solid line and the backward current path represented by the green line. This analysis assumes that the power switches' on-state resistance and voltage drop are both zero, the capacitor is sufficiently large, the voltage ripple is minimal, and the inverter has reached steady state. The reverse current paths are indicated with green dotted lines when the load is inductive. The forward current path corresponds to a particular path in each of the inverter's operational states, so inductive loads can be integrated into the suggested architecture without the need for additional voltage regulation.



Figure 1. Proposed NLSCI circuit topology



Figure 2. Current path for proposed inverter: (a) 2 Vdc level, (b) 1.5 Vdc level, (c) Vdc level, (d) 0.5 Vdc level, (e) 0 Vdc level, (f) -0.5 Vdc level, (g) -Vdc level, (h) -1.5 Vdc level, and (i) -2 Vdc level

It has a total of nine switches in the arrangement, but only 4 of them must remain active in order to produce the desired result. Losses will be minimized, and the switching process will be very simple. Two DC sources (100 V and 300 V) are often used to supply the essential dc voltage to the circuit. Important to this design is its ability to produce a wide range of voltages for both directions without turning to an H-bridge circuit. To prevent sources from being accidentally shorted out, the switches are designed so that the anti-parallel diodes within them are not forward biased. The proposed topology avoids source short-circuiting by selecting a switching state that accounts for all possible scenarios as possible. The suggested MLI's different operation modes are displayed in Table 1. The states of operation of 2 Vdc, 1.5 Vdc, Vdc, 0.5 Vdc, and 0 Vdc similarly for negative voltages are being depicted in Figures 2(a)-2(i).

O/P C Switches **S**1 S2 **S**3 **S**4 **S**5 S6 **S**7 **S**8 **S**9 S10 S11 C1 C2 D D 2 Vdc 1.5 Vdc D С С Vdc С D 0.5 Vdc С С D С -0.5 Vdc С С -Vdc D -1.5 Vdc -1 D -2 Vdc D

Table 1. NLSCI switching sates NLSCI

3. CONTROL STRATEGY

In the level shifted-sinusoidal PWM technique (LSPWMT), an N-level inverter was built using (N-1) carriers that had the identical frequency and maximal amplitude. The below zero axis carriers have in phase with each other and similarly the above zero axis carriers also arranged in phase with each other, as demonstrated by the carrier signal in Figure 3(a) (see Appendix). The technique used to arrange these carriers in consecutive phases is known as phase disposition (PD). Consequently, by matching a sinusoidal modulating wave to a triangle-shaped carrier wave utilizing comparator, the preliminary activating pulse is created instantaneously if the pulse is larger than the carrier signal. Following that, the required logical circuits are used to make relevant switching signals. There are 9 switches engaged in the NLSCI, and their respective gate pulses are being depicted in Figure 3(b) (see Appendix).

4. FINDINGS THROUGH SIMULATION

In MATLAB/SIMULINK, the NLSCI arrangement is developed and simulated using the level shifting phase disposition pulse width modulation (LS-PDPWM) technique for performance verification. The resulting 9-level waveform can be represented by voltages of $0, \pm 100 \text{ V}, \pm 200 \text{ V}, \pm 300 \text{ V}, \text{ and } \pm 400 \text{ V}$. For the simulation investigation, the relevant parameters are taken into account: 100 ohm-25 mH RL load, capacitor (C1 and C2) of 2200 F and V=200 V. Figures 4(a) and 4(b) display the NLSCI results form and the associated voltage harmonic bands with a modulation index (MI) of 1. At a highest fundamental voltage of 390 V, the voltage output waveform has a THD of 14.76%. Figures 5(a) and 5(b) depict the wave patterns of the voltage and current in addition to the harmonic voltages of NLSCI spectrum response for MI 0.9, accordingly. Peak voltage for NLSCI is 360 V, with a 16.74% THD in its voltage. The peak voltage for NLSCI is 319.9 V produced by NLSCI and NLSCI spectrum response of the harmonic voltage for MI of 0.8 have been portrayed in Figures 6(a) and 6(b), correspondingly. The generated voltage waveform exhibits a total harmonic content of 17.15% and a highest fundamental voltage of 319.9 V. The output obtained by NLSCI are laid out in Figures 7(a) and 7(b) and NLSCI spectral response of the harmonic voltage for MI 0.7, respectively. NLSCI has a peak voltage has 280 V with a total harmonic distortion (THD) of 21.24 percent.

As per the findings in Table 2, the suggested non-linear switched capacitor inverter (NLSCI) exhibits improved efficiency (98.85%) compared to other systems due to its lower power loss. The power loss of the NLSCI was evaluated using PLECS software, and the net losses were recorded at a power output of 521.9 W. Specifically, the effective switching loss of the N9LI was found to be 0.14%, while the conduction loss was 1.01%. Additionally, the % η (efficiency) and power loss of the N9LI were analyzed for various power ratings through simulation and experimental setups, and the outcomes are summarized in Table 2. From Table 2, it is evident that the NLSCI outperforms other systems at 521.9W, achieving an efficiency value of 98.85% in simulation and 98.84% in experimental testing.



134

Figure 4. NLSCI with LS-PDPWM (a) load voltage and current with modulation index of 1 and (b) load voltage FFT



Figure 5. NLSCI with LS-PDPWM (a) load voltage and current with modulation index of 0.9 and (b) load voltage FFT



Figure 6. NLSCI with LS-PDPWM (a) load voltage and current with modulation index of 0.8 and (b) load voltage FFT



Figure 7. NLSCI with LS-PDPWM (a) load voltage and current with modulation index of 0.7 and (b) load voltage FFT

Load rating	Simulation			Measured		
	Output power	%η	% loss	Output power	%η	% Loss
150Ω	521.9	98.85	1.15	521.7	98.84	1.16
120 Ω	652.4	98.81	1.19	652.3	98.80	1.2
100Ω	782.9	98.74	1.26	782.8	98.72	1.28
80Ω	977.9	98.71	1.29	977.9	98.68	1.32
60Ω	1307	98.71	1.29	1306.9	98.69	1.31
50Ω	1568	98.69	1.31	1567.9	98.66	1.34
40Ω	1960	98.61	1.39	1958	98.58	1.42

Table 2. Power loss comparison and efficiency of the NLSCI different output power

5. CONCLUSION

This study presents NLSCI with LS-PDPWM techniques. The recommended NLSCI has a plenty benefit over numerous different MLI topologies. In comparison to certain other MLI topologies, the NLTSI generated 9 levels of voltage with the fewest switching devices and input power sources. Increased output voltage, reduced harmonics, and an improved voltage profile are all benefits of the NLSCI that has been suggested. The efficiency of NLSCI is assessed with various MI. The MI one results in 14.96% THD. The results of the simulations show that the suggested NLSCI is effective. By expanding the basic units, a wider range of output values can be accommodated by adding to the NLSCI layout.

APPENDIX



Figure 3. PD approach switching pattern of NLSCI: (a) carrier pattern and (b) switching pulses

REFERENCES

- B. Axelrod, Y. Berkovich, and A. Ioinovici, "A cascade boost-switched-capacitor-converter two level inverter with an optimized multilevel output waveform," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 52, no. 12, pp. 2763–2770, Dec. 2005, doi: 10.1109/TCSI.2005.852205.
- [2] M. S. W. Chan and K. T. Chau, "A New Switched-Capacitor Boost-Multilevel Inverter Using Partial Charging," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 12, pp. 1145–1149, Dec. 2007, doi: 10.1109/TCSII.2007.905352.
- [3] K. Sano and H. Fujita, "Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1768–1776, 2008, doi: 10.1109/TIA.2008.2006291.
- [4] J. Zhao, Y. Han, X. He, C. Tan, J. Cheng, and R. Zhao, "Multilevel Circuit Topologies Based on the Switched-Capacitor Converter and Diode-Clamped Converter," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2127–2136, Aug. 2011, doi: 10.1109/TPEL.2010.2104330.
- [5] Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012, doi: 10.1109/TIE.2011.2158768.
- [6] J. Liu, K. W. E. Cheng, and Y. Ye, "A Cascaded Multilevel Inverter Based on Switched-Capacitor for High-Frequency AC Power Distribution System," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4219–4230, Aug. 2014, doi: 10.1109/TPEL.2013.2291514.
- [7] A. Tsunoda, Y. Hinago, and H. Koizumi, "Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4011–4021, Aug. 2014, doi: 10.1109/TIE.2013.2286559.
- [8] E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014, doi: 10.1109/TIE.2013.2290769.
- [9] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014, doi: 10.1109/TIE.2014.2314052.
- [10] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series–Parallel Conversion With Less Number of Components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016, doi: 10.1109/TIE.2016.2529563.
- [11] N. Sandeep and U. R. Yaragatti, "A Switched-Capacitor-Based Multilevel Inverter Topology With Reduced Components," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5538–5542, Jul. 2018, doi: 10.1109/TPEL.2017.2779822.
- [12] S. R. Raman, K. W. E. Cheng, and Y. Ye, "Multi-Input Switched-Capacitor Multilevel Inverter for High-Frequency AC Power Distribution," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5937–5948, Jul. 2018, doi: 10.1109/TPEL.2017.2742525.
- [13] L. He and C. Cheng, "A Bridge Modular Switched-Capacitor-Based Multilevel Inverter With Optimized SPWM Control Method and Enhanced Power-Decoupling Ability," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6140–6149, Aug. 2018, doi: 10.1109/TIE.2017.2784375.
- [14] S. S. Lee, "Single-Stage Switched-Capacitor Module (S 3 CM) Topology for Cascaded Multilevel Inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.
- [15] H. Khoun Jahan, M. Abapour, and K. Zare, "Switched-Capacitor-Based Single-Source Cascaded H-Bridge Multilevel Inverter Featuring Boosting Ability," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019, doi: 10.1109/TPEL.2018.2830401.
- [16] J. S. Mohamed Ali and V. Krishnasamy, "Compact Switched Capacitor Multilevel Inverter (CSCMLI) With Self-Voltage Balancing and Boosting Ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019, doi: 10.1109/TPEL.2018.2871378.
- [17] S. R. Raman, Y. C. Fong, Y. Ye, and K. W. Eric Cheng, "Family of Multiport Switched-Capacitor Multilevel Inverters for High-Frequency AC Power Distribution," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4407–4422, May 2019, doi: 10.1109/TPEL.2018.2859030.
- [18] V. Arun, S. Prabhu, A. A. Stonier, and B. Shanthi, "Design of Novel Structure Nine Level Trinary Source Inverter," in 2023 9th International Conference on Electrical Energy Systems (ICEES), IEEE, Mar. 2023, pp. 175–178. doi: 10.1109/ICEES57979.2023.10110112.
- [19] S. Ramaiah, N. Lakshminarasamma, and M. K. Mishra, "Multisource Switched Capacitor Based Boost Multilevel Inverter for Photovoltaic-Based Systems," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2558–2570, Mar. 2020, doi: 10.1109/TPEL.2019.2924649.
- [20] V. Arun, S. Prabhu, N. Prabaharan, and B. Shanthi, "Modified Structure 9-Level Inverter (MS9LI) With Reduced On-State Switches," *IEEE Can. J. Electr. Comput. Eng.*, vol. 46, no. 1, pp. 15–23, 2023, doi: 10.1109/ICJECE.2022.3222215.
- [21] V. Jagan, M. K. R. Alpuri, M. Neeharika, C. Swetha, P. Mahendar, and S. Das, "A family of switched-impedance network enhanced-boost quasi-Z-source inverters," *Int. J. Power Electron. Drive Syst.*, vol. 13, no. 1, pp. 309–321, Mar. 2022, doi: 10.11591/ijpeds.v13.i1.pp309-321.
- [22] S. Pachipala, A. Guda, M. S. Babu, V. B., K. V. S. R. Murthy, and A. Tirupathi, "A series-connected switched source and an Hbridge based multilevel inverter," *Indones. J. Electr. Eng. Comput. Sci.*, vol. 24, no. 2, pp. 673–679, Nov. 2021, doi: 10.11591/ijeecs.v24.i2.pp673-679.
- [23] M. Al Gabalawy, R. M. Hossam, S. A. Hussien, and N. S. Hosny, "Switched capacitor based multi-level boost inverter for smart grid applications," *Int. J. Electr. Comput. Eng.*, vol. 11, no. 5, pp. 3772–3781, Oct. 2021, doi: 10.11591/ijece.v11i5.pp3772-3781.
- [24] S. Kakar, S. M. Ayob, M. S. Bin Arif, N. M. Nordin, Z. Daud, and R. Ayop, "A new multilevel inverter topology based on switched-capacitor technique," *Int. J. Power Electron. Drive Syst.*, vol. 12, no. 1, pp. 627–636, Mar. 2021, doi: 10.11591/ijpeds.v12.i1.pp627-636.
- [25] K. K. Deepika, J. V. Kumar, and G. K. Rao, "Enhancement of voltage regulation using a 7-Level inverter based electric spring with reduced number of switches," *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 2, pp. 555–565, Jun. 2020, doi: 10.11591/ijpeds.v11.i2.pp555-565.

BIOGRAPHIES OF AUTHORS



Vijayakumar Arun **(D) (S) (S)** received the B.Tech. degree in Electrical and Electronics Engineering from SRM University, Chennai, India, in 2007 and the M.E. degree in Power Systems Engineering from the Anna University of Technology, Coimbatore, India, in 2009, and the Ph.D. degree from the Annamalai University, India, in 2016. He is a professor with the Electrical and Electronics Engineering Department, Mohan Babu University, Tirupati, India. His current research interests include power converters and applications, control techniques, and the integration of renewable energy into the smart grid. He can be contacted at email: varunpse@yahoo.com.



Thunga Nageswara Prasad D S S D obtained a B.Tech. from Vellore Institute of Technology, Vellore, and a M.Tech. from JNTUCE, Hyderabad. He pursued his doctoral studies in Faculty of Electrical Engineering, Sri Venkateshwara University, Tirupati. Currently, he is working as a Professor of Electrical and Electronics Engineering at Mohan Babu University, Tirupati, Andhra Pradesh, India. He has more than two decades of experience in academics. His area of interest includes power quality, power system operation & control, and application of optimization techniques. He is a life member of IEEE, IE(I), and ISTE. He can be contacted at email: nprasad.thunga@gmail.com.



Sundaramoorthy Prabhu b s s c is currently working at Mohan Babu University (formerly Sree Vidyanikethan Engineering College) in Tirupati as an associate professor of electrical and electronics engineering since 2019. He completed his master of engineering from Arunai Engineering College, affiliated to Anna University in 2011, and he obtained Ph.D. from Anna University, Chennai, in 2020. He published 30 research papers in refereed journals and conferences. His areas of interest are electrical drives, machine design, and finite element analysis. He can be contacted at email: prabu.s@vidyanikethan.edu.



Nagarajan Ashokkumar b K c received a B.E. degree in Electronics and Communication Engineering from Anna University, Chennai, in 2007, a M.E. degree in Applied Electronics from Anna University Trichy in 2010, and Ph.D. degree in the title of Performance Analysis of 2D and 3D Network-On-Chip Architectures from Anna University, Chennai, in 2017. Currently, he is an Associate Professor in the department of Electronics and Communication Engineering at Mohan Babu University, Tirupati, Andhra Pradesh, India. His research interests include network-on-chip, system-on-chip, and low-power and digital VLSI design. He can be contacted at email: ashoknoc@gmail.com.