International Journal of Applied Power Engineering (IJAPE)
Vol. 13, No. 2, June 2024, pp. 269~281
ISSN: 2252-8792, DOI: 10.11591/ijape.v13.i2.pp269-281

Performance evaluation of novel 9-level RSMLI topology for grid-tied solar-PV system

Pidatala Prabhakara Sharma, Lingineni Shanmukha Rao, Goddanti Amulya
Department of Electrical and Electronics Engineering, Kallam Haranadhareddy Institute of Technology, Guntur, India

Article Info

Article history:

Received Jun 9, 2023
Revised Aug 12, 2023
Accepted Aug 31, 2023

Keywords:

DC-DC boost converter
Micro-grid system
Reduced-switch multilevel
Solar-PV arrays
Total harmonic distortions

ABSTRACT

The shortage of traditional fossil fuels like coal, petrol and natural-gas are increased day-by-day, fulfills the most of energy demand. Most of engineers are trying to maximize the energy demand by employing renewable energy with existing micro-grid system. Owing to merits, the solar-PV system plays a significant alternative among all other renewable energy sources due to abundant and virtuous nature. For grid-tied solar-PV system, the cascaded H-bridge multilevel inverter is the most significant over the classical 2-level inverter due to provision of isolated input DC sources. But the cascaded H-bridge topology is designed for limited voltage levels due to its larger number of switches for higher voltage levels, high cost, large-size, and more weight. To alleviate these demerits, a reduced-switch multilevel inverter has been generally preferable for higher voltage levels. In this work, a novel 9-level reduced-switch multilevel inverter (RSMLI) topology has been proposed by utilizing low number of switching devices. The performance of proposed novel 9-level RSMLI topology has been verified in grid-tied solar-PV system by using MATLAB/Simulink tool, simulation results are presented with attractive comparisons.

Corresponding Author:

Lingineni Shanmukha Rao
Department of Electrical and Electronics Engineering, Kallam Haranadhareddy Institute of Technology
Guntur, Andhra Pradesh, India
Email: lsrlingineni@gmail.com

1. INTRODUCTION

At present, the solar-PV plants can produce bulk electrical energy which is fed to existing micro-grid for ease of controlling by employing maximum-power point tracking (MPPT) algorithm [1]–[4]. Moreover, it is highly fragile because of various solar-PV cells are connected as series or parallel to generate rated power to drive the requisite demand. The power of solar-PV system is varies during varying temperature and irradiance levels, for extraction of maximum power an incremental-conductance MPPT algorithm has been employed [5]–[7]. The obtained solar-PV energy is directly connected to standalone grid system by using advanced power conversion devices. It consists of DC-DC boost converter and DC-AC inverter modules.

In recent days, the classical 2-level or 3-level square-wave inverter modules are replaced with multilevel inverter (MLI) topologies for medium-voltage and high-power industrial and domestic applications [8]. Among the classical square-wave inverters, the MLI topologies offer favorable merits such as good quality RMS voltage, reduced common-mode voltage, low dv/dt stress, low harmonic profile, low switching stress and increased efficiency, etc. In general, the MLI topology generates staircase output voltage at load terminals from several input DC sources by regulating the switching action of respective switches using feasible switching pulses [9].

The block diagram of grid-integrated solar-PV system is depicted in Figure 1. To alleviate these demerits, a reduced-switch multilevel inverter (RSMLI) has been generally preferable for higher voltage levels [10]–[15]. According from various literature studies, a single-phase 5-level RSMLI topology is proposed in [16], by using 7 switches for medium-voltage applications without using any transformers. A new single-stage solar-PV integrated 7-level MLI topology is explored in [17], for standalone applications by using 12 switches and without any extra clamping circuits. A single-phase 7-level RSMLI topology is proposed by using 6 switches employing a solar-PV connected multi-output DC-DC converter [18] is depicted in Figure 2.

But this topology is not suitable for higher voltage levels because it requires more high frequency transformers in DC-DC converter which increases the size and cost of overall topology. Bhanutej *et al*. [19], a novel 9-level RSMLI topology is proposed by using 11 switches for reducing the harmonic profile in a standalone micro-grid system. In fact, these MLI topologies are controlled by using regular sinusoidal pulse-width modulation (PWM) techniques such as phase-shift PWM and level-shift PWM techniques [20]–[25]. But it requires more carrier signals for generation of required voltage levels which increases the complex drive circuitry. Based on above problem statement, the major objective of this work is proposing the novel RSMLI topology for grid-tied solar-PV system with fewer switching devices and it doesn't requirement of any high frequency transformers. In this work, a novel 9-level RSMLI topology has been proposed by utilizing 7 switches and controlled by novel reduced-carrier PWM technique. The performance of proposed novel 9-level RSMLI topology with RCPWM technique has been verified in grid-tied solar-PV system by using MATLAB/Simulink tool, simulation results are presented with attractive comparisons.

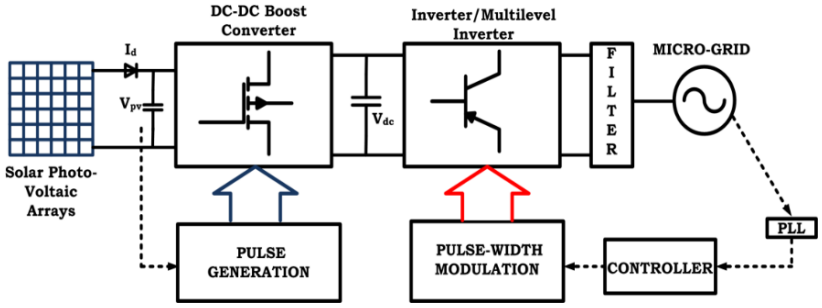


Figure 1. Block diagram of grid integrated solar-PV system

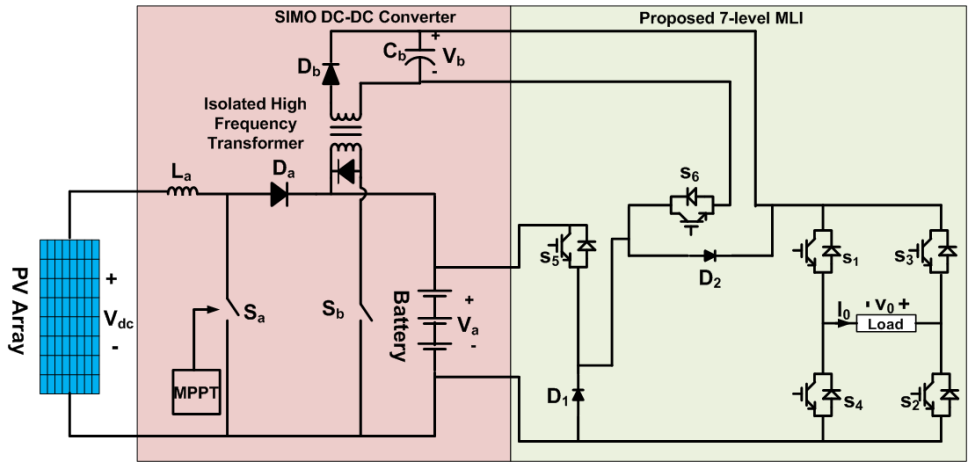


Figure 2. Conventional 7-level RSMLI topology using high-frequency transformer circuit [18]

2. PROPOSED 9-LEVEL RSMLI TOPOLOGY FOR GRID-TIED SOLAR-PV SYSTEM

Figure 3 shows the block diagram of proposed 9-level RSMLI topology. It consists of various elements such as input DC sources, IGBT switches, and resistive or inductive loads. Generally, it requires (n-2) operating switches named as S_{d1}, S_{d2}, S_{d3}, S_{d4}, S_{d5}, $S_{d6,}$ and S_{d7}, respectively. Also, ((n-1)/2) input DC sources named V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} as for energizing the proposed 9-level RSMLI topology to attain total 4 V_{dc} output voltage at load terminals. The synthetization of various output voltage V_o levels at load terminals

is comprising of 9 voltage levels such as $0V_{dc}$, $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, $+4V_{dc}$, and $-V_{dc}$ $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$, respectively. The mathematical relations of proposed 9-level RSMLI topology is illustrated as:

- Required number of switches (N_s):

$$N_s = (n-2) \tag{1}$$

- Required number of DC sources (NDC):

$$N_{DC} = \frac{(n-1)}{2} \tag{2}$$

- Required number of possible operating modes (Nm)

$$N_m = 2\left(\frac{n-1}{2}\right) + 1 \tag{3}$$

- Required number of voltage levels (VO) at output node

$$V_O = (n_{DC} \times 2) + 1 \tag{4}$$

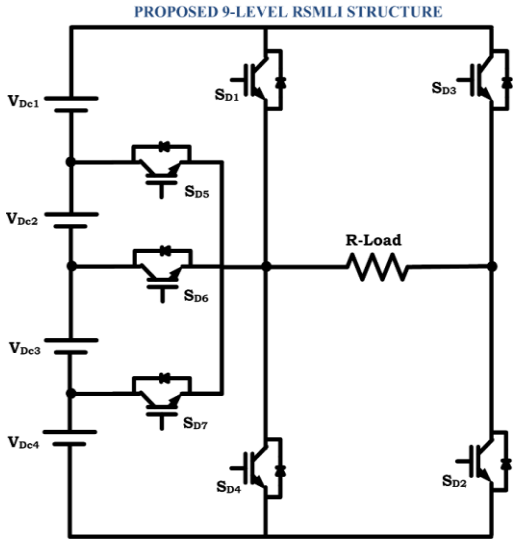


Figure 3. Block diagram of proposed 9-level RSMLI topology

The switching states of proposed 9-level RSMLI topology are illustrated in Table 1. In that, "1" expresses the ON-state of respective switch and "0" expresses the OFF-state of respective switch, accordingly. In fact, the proposed RSMLI topology is controlled by using reduced-carrier PWM technique; it requires low carrier signals for generation of required 9-voltage levels which decreases the complex drive circuitry over the phase-shifted pulse-width modulation (PSPWM) and level-shifted multicarrier modulation (LSPWM) techniques. For generation of 9-voltage levels, the proposed RSMLI technique requires only 1 sinusoidal reference signal V_{ref} with a frequency of 50 Hz. And also, 4 triangular carrier signals are needed such as V_{c1}, V_{c2}, V_{c3} and V_{c4}, with the carrier frequency of 3050 Hz which are vertically disposed and slight variations in magnitude of carrier signals. The switching pattern and switching pulses of proposed RCPWM technique is depicted in Figures 4 and 5.

The feasible switching pattern is processed based on possible mathematical expressions which are stated in (5).

$$\begin{aligned}
S_{d1} &= D \cdot E \\
S_{d2} &= (A \cdot \bar{E}) \\
S_{d3} &= (\bar{A} \cdot E) + (D \cdot \bar{E}) \\
S_{d4} &= (\bar{A} \cdot \bar{E}) + E \\
S_{d5} &= (C \cdot E \cdot \bar{D}) + (A \cdot \bar{E} \cdot \bar{B}) \\
S_{d6} &= B \cdot \bar{C} \\
S_{d7} &= (C \cdot \bar{D} \cdot \bar{E}) + (A \cdot E \cdot \bar{B})
\end{aligned} \tag{5}$$

The overall schematic diagram of proposed 9-Level RSMLI topology with RCPWM technique for grid-tied solar-PV system is shown in Figure 6.

Table 1. Switching states of proposed 9-level RSMLI topology

Mode	Load voltage (V_O)	Switching states						
		S_{da1}	S_{da2}	S_{da3}	S_{da4}	S_{da5}	S_{da6}	S_{da7}
Level-1	0 V_{dca}	0	1	0	1	0	0	0
Level-2	V_{dca}	0	1	0	0	0	0	1
Level-3	2 V_{dca}	0	1	0	0	0	1	0
Level-4	3 V_{dca}	0	1	0	0	1	0	0
Level-5	4 V_{dca}	1	1	0	0	0	0	0
Level-6	-V_{dca}	0	0	1	0	1	0	0
Level-7	-2 V_{dca}	0	0	1	0	0	1	0
Level-8	-3 V_{dca}	0	0	1	0	0	0	1
Level-9	-4 V_{dca}	0	0	1	1	0	0	0

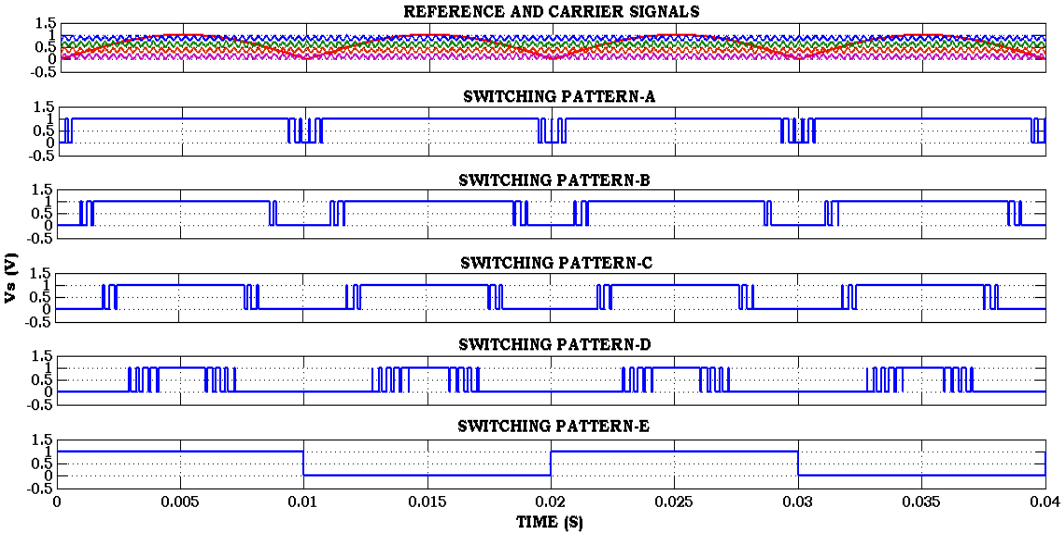


Figure 4. Switching pattern

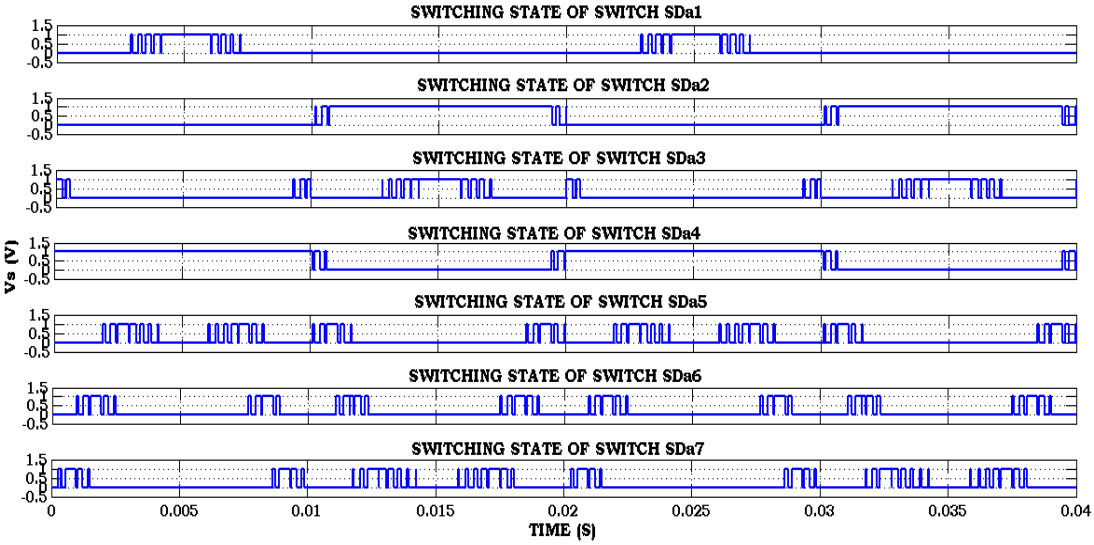


Figure 5. Switching states

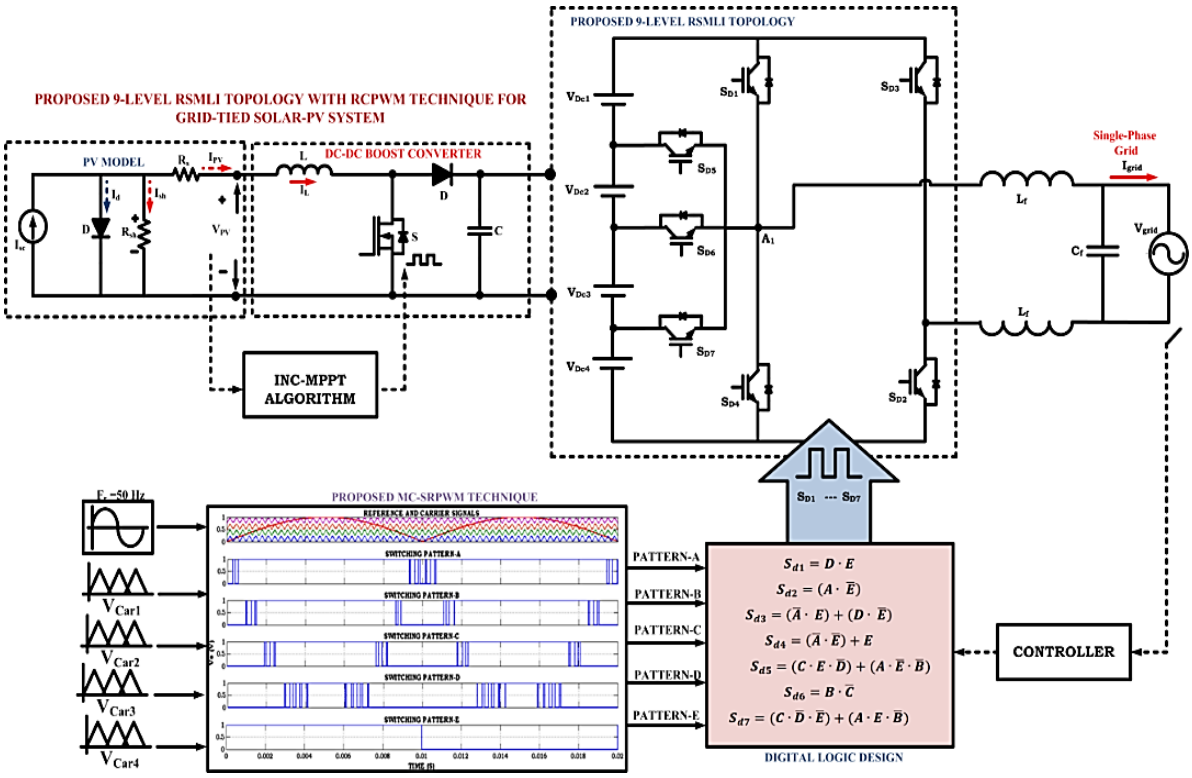


Figure 6. Overall schematic diagram of proposed 9-level RSMLI topology with RCPWM technique for grid-tied solar-PV system

3. MATLAB/SIMULINK RESULT AND DISCUSSION

3.1. Performance of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique

The performance of proposed novel 9-level RSMLI topology has been verified in R-load, RL-load and grid-tied solar-PV system by using MATLAB-Simulink tool, simulation results are presented with attractive comparisons. The specifications and values of proposed topology is illustrated in Table 2. Figure 7 (see in Appendix) shows the simulation results of proposed Solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage of 115 V during steady-state condition; a slight change in applied illumination implies the starting transient response occurred in solar-PV voltage of 240 V. The solar-PV current of 43 A and a slight change in applied illumination implies the starting transient response occurred in solar-PV power of 10.1 kW and solar-PV power of 5 kW during steady-state condition to drive the R-load system as depicted in Figure 7(a). The obtained solar-PV voltage of 115 V is converted into high step-up voltage DC output voltage of 230 V, with a current of 21 A and output power of 4.8 kW as depicted in Figure 7(b), by using front-end DC-DC boost converter to energize the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage at load terminals with a voltage of 230 V and the load current of 21 A, respectively as depicted in Figures 7(c) and 7(d). The IGBT switches in novel 9-level RSMLI topology are switched-ON/OFF by using proposed RCPWM technique. The total harmonics distortions (THD) spectrum of 9-level output voltage under R-load is measured as 14.09% and the THD spectrum of 9-level output current under R-load is measured as 14.09%, respectively as depicted in Figures 7(e) and 7(f).

Table 2. System specifications and values of proposed topology

S. No	Specifications	Values
1	Solar-PV voltage	V_{pv}-115 V (peak), I_{pv}-45 A, P_{spv}-5 kW
2	DC-DC converter	V_{in}-115 V, V_O-230 V, I_o-21A, P_o-4.8 kW, L_{dc}-0.33 mH, C_{dc}-148µF
3	Input DC-link capacitors	V_o-230 V, V_{dc1234}-1480 µF
4	Load Impedance	R-load R-11 Ω, RL-Load R-11 Ω, L-0.0169 mH
5	Switching frequency	F_c-3050 Hz
6	Micro-grid system	V_{grid}-230 V, I_{grid}-20A, P_{grid}-4.6 kW

3.2. Performance of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique

Figure 8 (see in Appendix) shows the simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage of 115 V during steady-state condition; a slight change in applied illumination implies the starting transient response occurred in solar-PV voltage of 240 V. The solar-PV current of 43 A and a slight change in applied illumination implies the starting transient response occurred in solar-PV power of 10.1 kW and solar-PV power of 5 kW during steady-state condition to drive the R-load system as depicted in Figure 8(a). The obtained solar-PV voltage of 115 V is converted into high step-up voltage DC output voltage of 230 V, with a current of 21 A and output power of 4.8 kW as depicted in Figure 8(b), by using front-end DC-DC boost converter to energize the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage at load terminals with a voltage of 230 V and the sinusoidal load current of 21 A, respectively as depicted in Figures 8(c) and 8(d). The IGBT switches in novel 9-level RSMLI topology are switched-ON/OFF by using proposed RCPWM technique. The THD spectrum of 9-level output voltage under RL-load is measured as 14.09% and the THD spectrum of sinusoidal output current under RL-load is measured as 1.33%, respectively as depicted in Figures 8(e) and 8(f). Thus, the THD spectrum of sinusoidal load current is well within IEEE-519/2014 standards.

3.3. Performance of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique

Figure 9 (see in Appendix) shows the simulation results of proposed Solar-PV powered novel 9-level RSMLI topology under grid-connected system using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage which energizes the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage (before LCL filter) is depicted in Figure 9(a) and single-phase grid voltage at grid terminals (after LCL filter) is measured with a voltage of 230 V and the sinusoidal single-phase grid current of 22.5 A is depicted in Figures 9(b) and 9(c). The grid current is in-phase with the grid voltage which represents the unity power-factor at grid terminals in depicted in Figure 9(d). The THD spectrum of grid voltage and grid current under grid-connected system is measured as 0.02% and 1.29%, respectively as depicted in Figures 9(e) and 9(f). Thus, the THD spectrum of grid voltage and grid current is well within IEEE-519/2014 standards. The THD comparisons of proposed 9-level RSMLI topology under R-load, RL-load and grid-connected system are illustrated in Table 3. The comparison of number of switching devices required for generation of 9-Level voltage under classical MLI topologies and proposed RSMLI topology is illustrated in Table 4. In that, the proposed novel 9-level RSMLI topology requires very less switching devices and no need of any high frequency transformer which reduces the size, cost and complex control circuitry.

Table 3. THD comparisons of proposed 9-level RSMLI topology under R-Load, RL-load, and grid-connected system

THD (%)	Output/grid voltage	Output/grid current
Proposed 9-Level RSMLI Topology under R-Load	14.09%	14.09%
Proposed 9-Level RSMLI Topology under RL-Load	14.09%	1.33%
Proposed 9-Level RSMLI Topology under Grid Connected System	0.02%	1.29%

Table 4. Comparison of number of switching devices required for generation of 9-level voltage under classical MLI topologies and proposed RSMLI topology

Topologies switching devices	Classical 9-Level MLI Topologies			Conventional 9-Level RSMLI Topology	Proposed 9-Level RSMLI Topology
	DCMLI Topology	FCMLI Topology	CHBMLI Topology		
Main IGBT Switches	16	16	16	10	7
Input DC Sources	8	8	8	4	4
Clamping Diodes	56	0	0	0	0
Balancing Capacitors	0	28	0	0	0
Body Diodes	16	16	16	7	7
High Frequency Transformers	0	0	0	3	0

4. CONCLUSION

The design and operation of proposed novel 9-level RSMLI topology has been evaluated and highly recognized for standalone R-load, RL-load and grid-connected system under the same voltage-power

specifications. Over the classical 9-level MLI topologies, the key merits of proposed RSMLI topology have fewer switches, compact size, good quality RMS voltage, low harmonic content, reduced common-mode voltage, low dv/dt stress, low switch losses, and increased efficiency. And also, the proposed RCPWM technique requires only carriers for generation of required switching pulses to novel RSMLI topology among the PSPWM and LSPWM techniques, which reduces the computational delay and complex gate-pulse generation unit, etc. Therefore, the proposed novel RSMLI topology requires very less switching devices and no need of any high frequency transformers which reduces the size, cost and complex control circuitry.

APPENDIX

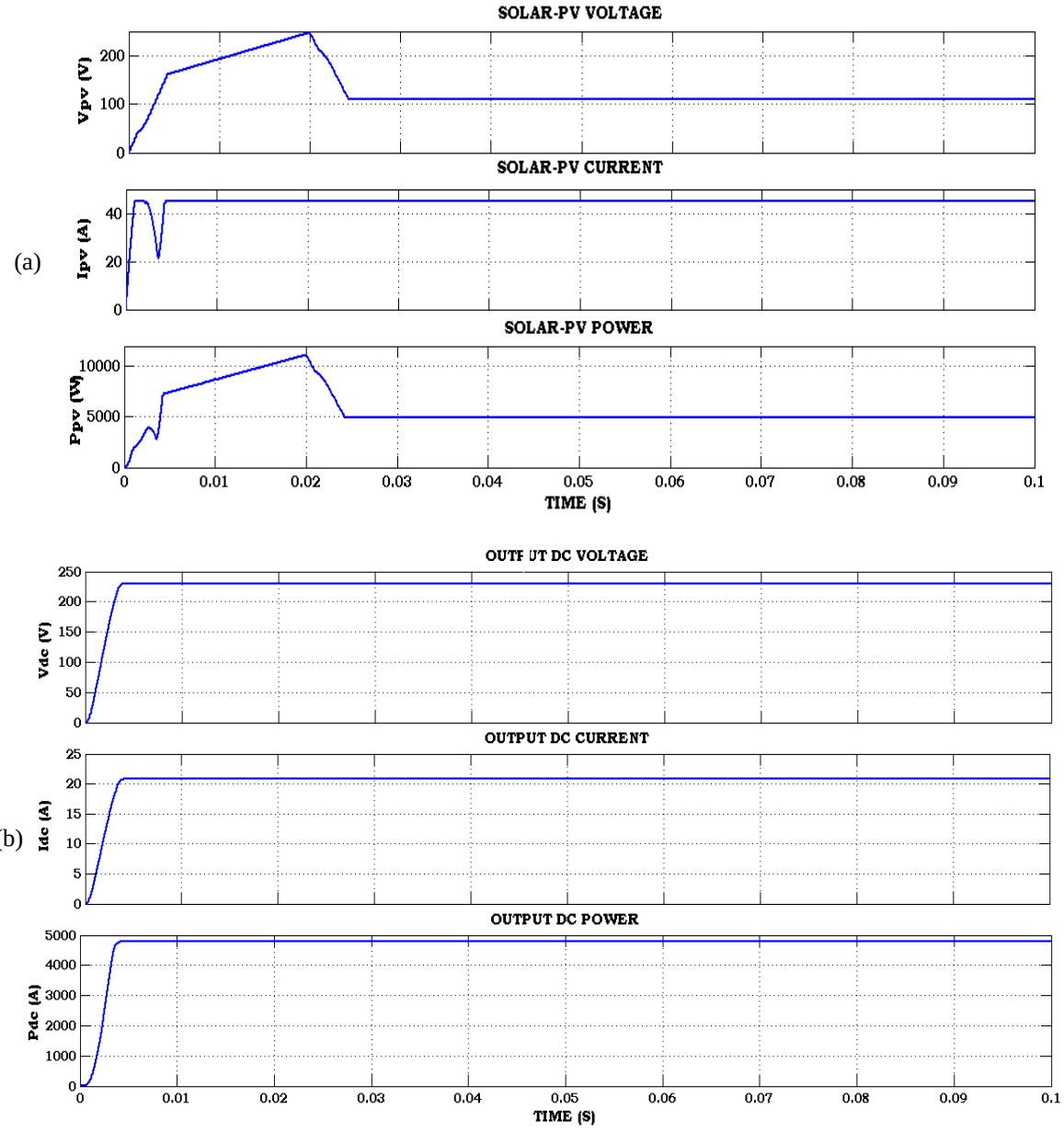
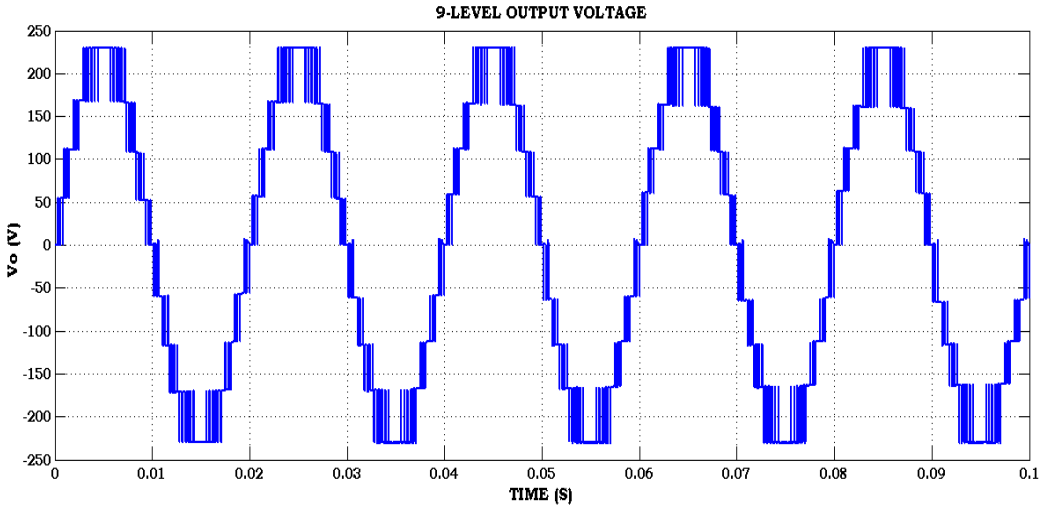
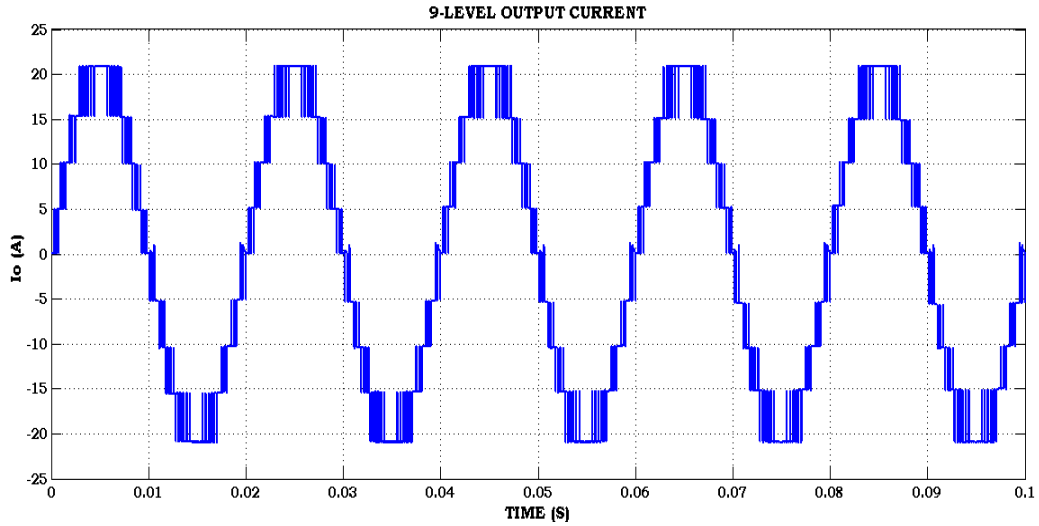


Figure 7. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique: (a) solar-PV input voltage, current, and power and (b) output DC-link voltage, current and power

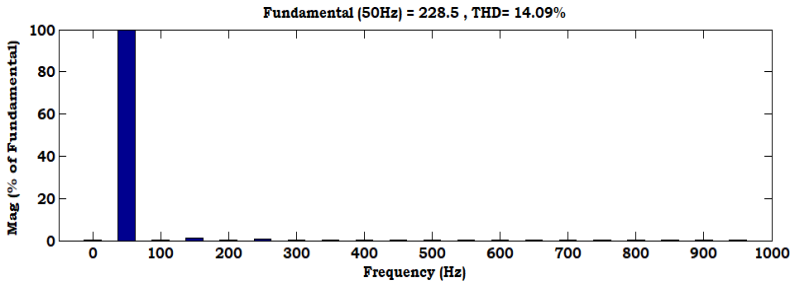
(c)



(d)



(e)



(f)

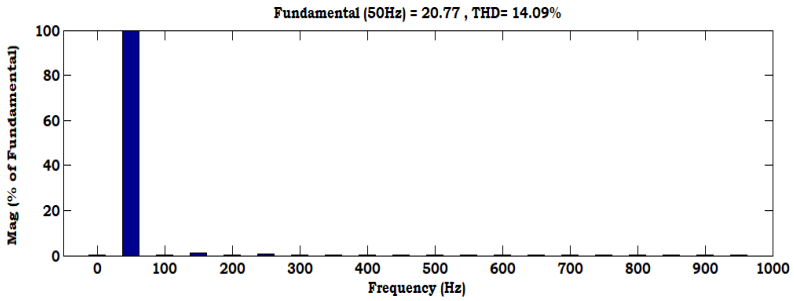


Figure 7. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique: (c) 9-level output voltage, (d) 9-level output current, (e) THD spectrum of 9-level output voltage, and (f) THD spectrum of 9-level output current (continued)

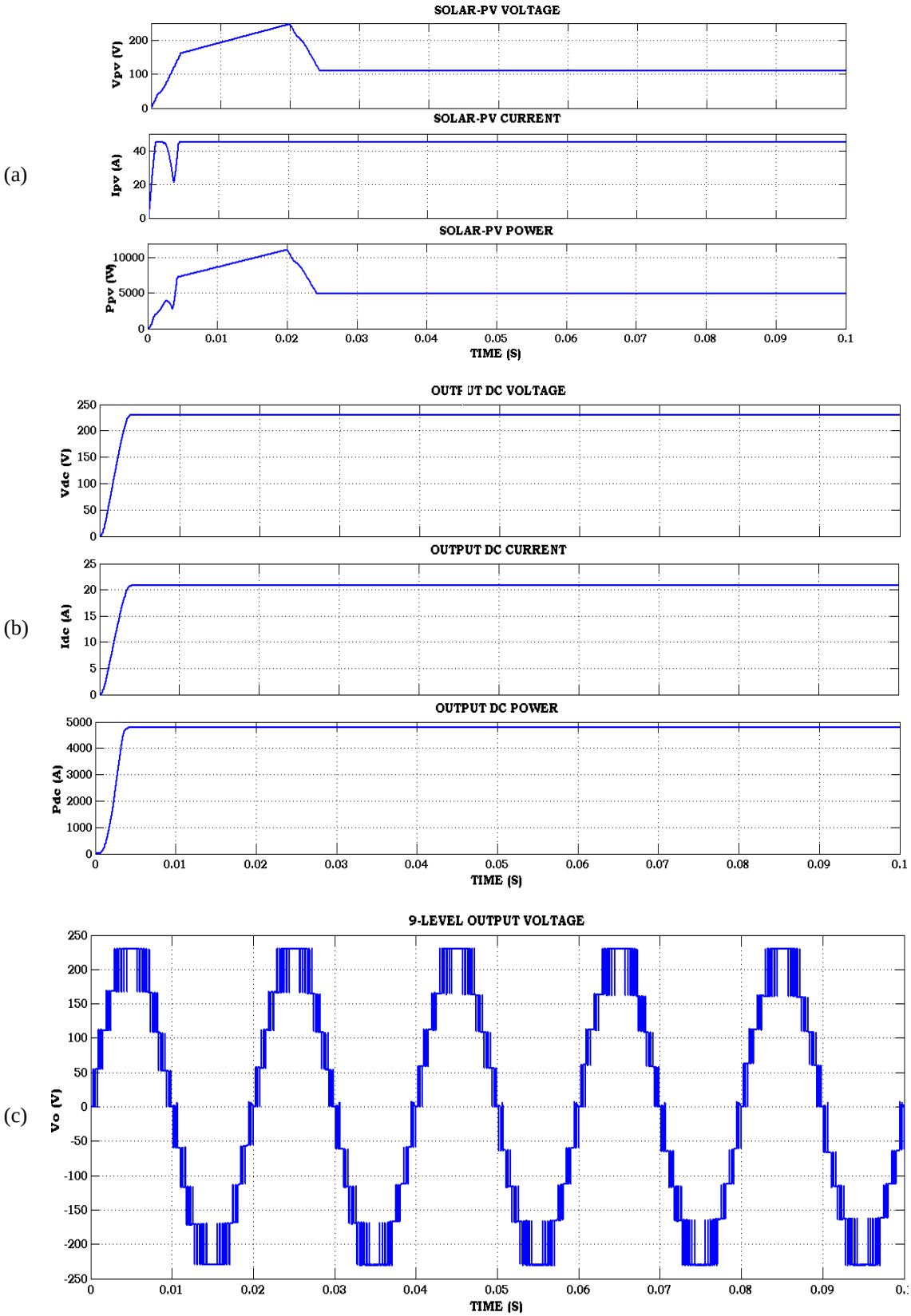


Figure 8. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique: (a) solar-PV input voltage, current, and power, (b) output DC-link voltage, current, and power, and (c) 9-level output voltage

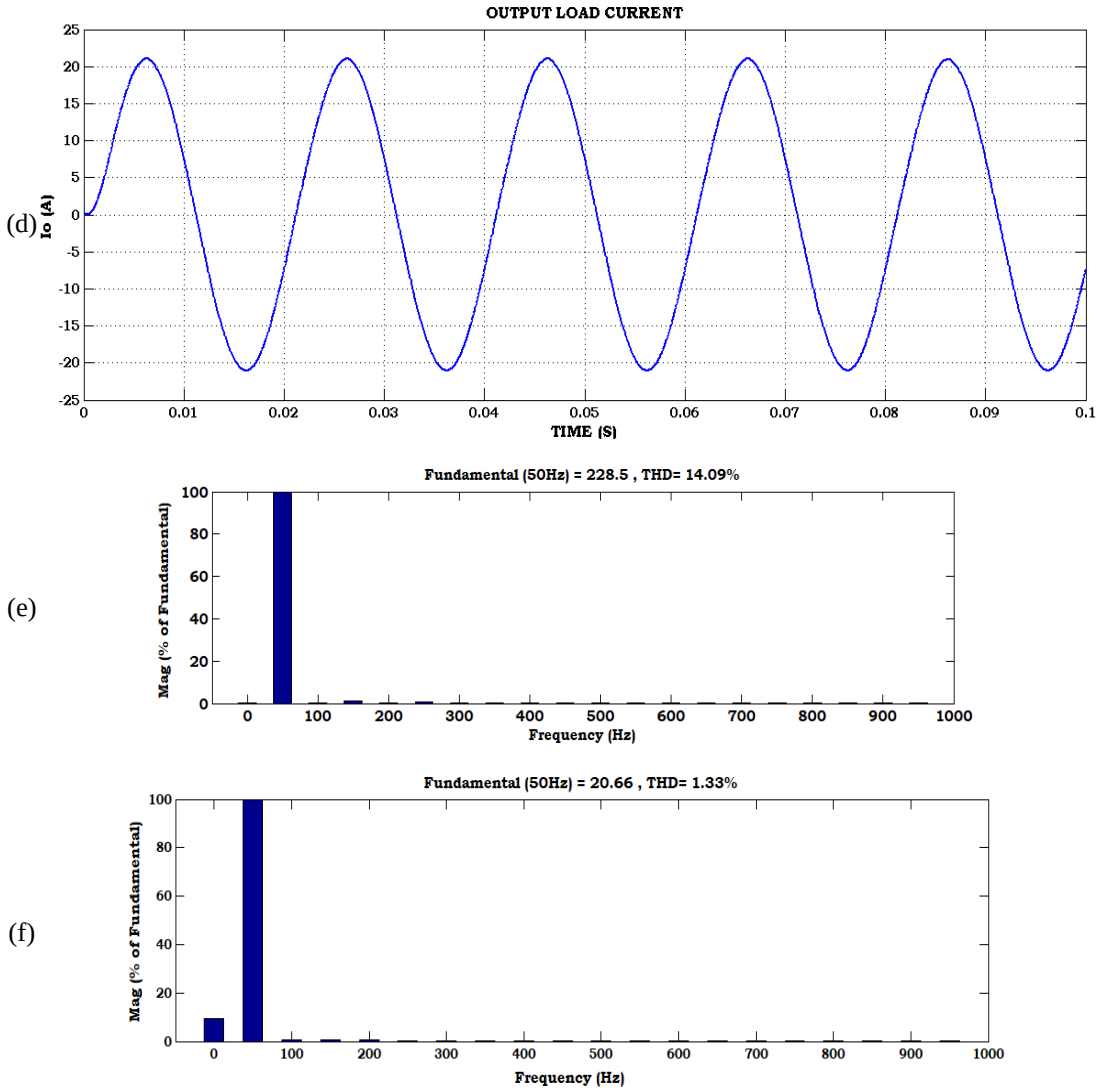


Figure 8. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique: (d) sinusoidal output current, (e) THD spectrum of 9-level output voltage, and (f) THD spectrum of sinusoidal output current (continued)

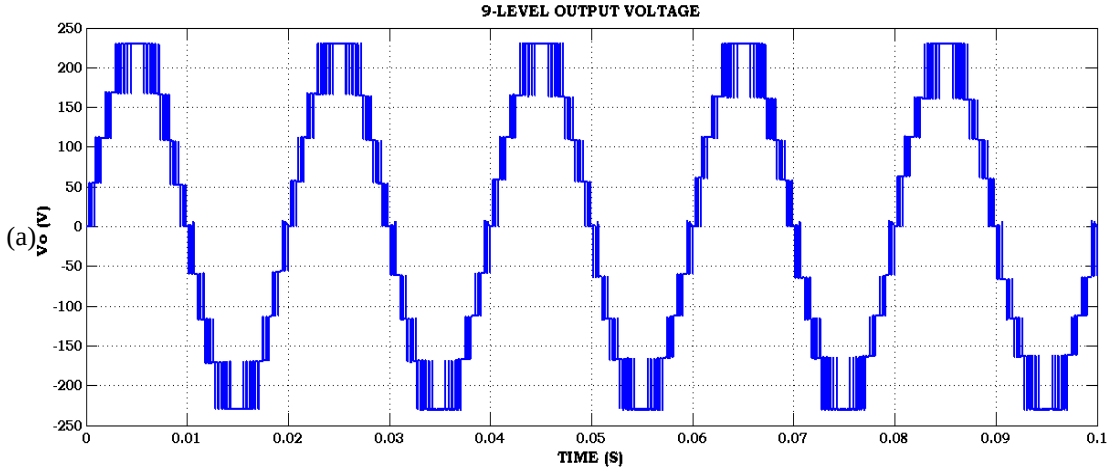


Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (a) 9-level output voltage

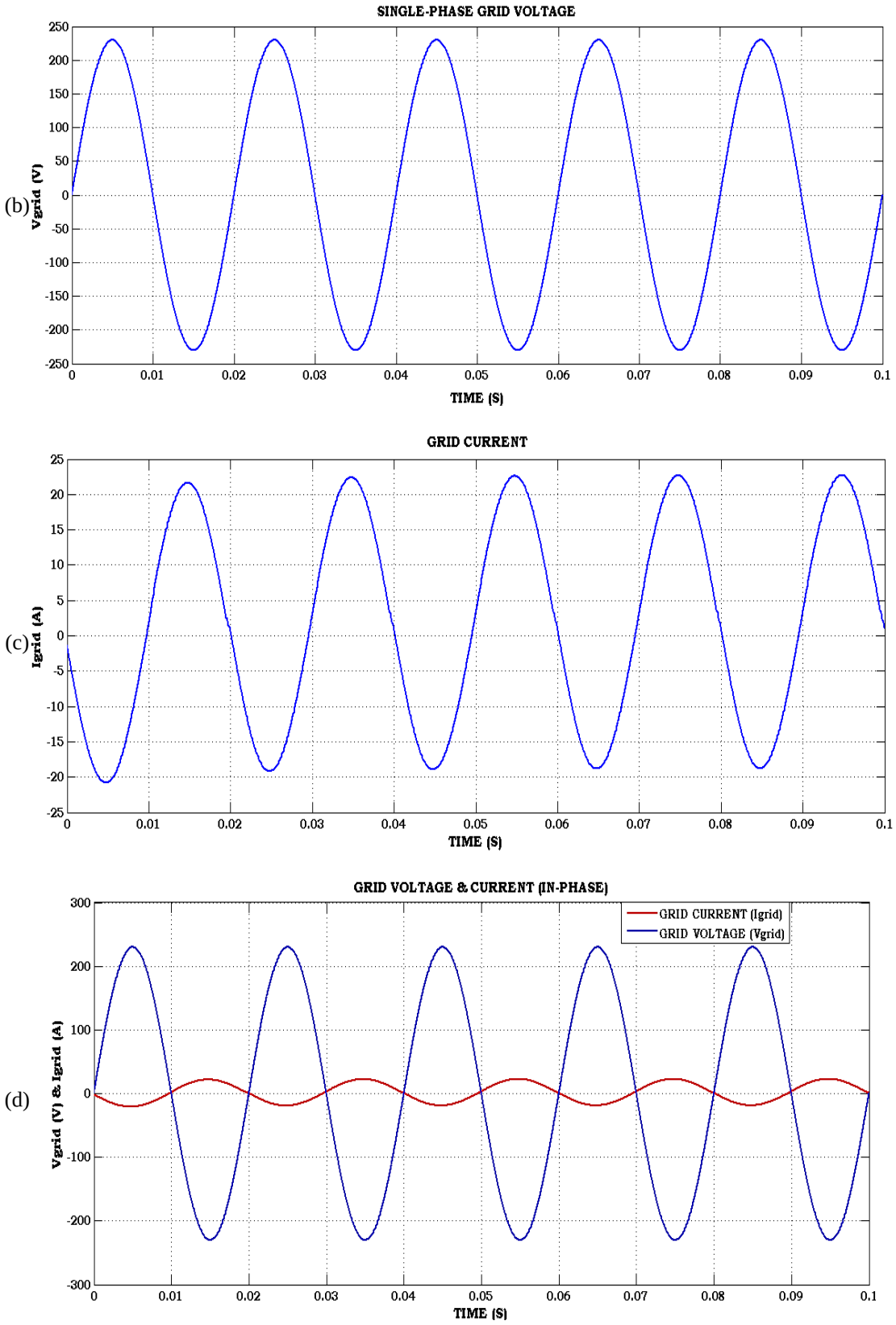


Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (b) single-phase grid voltage, (c) grid current, and (d) grid voltage and current (in-phase) (continued)

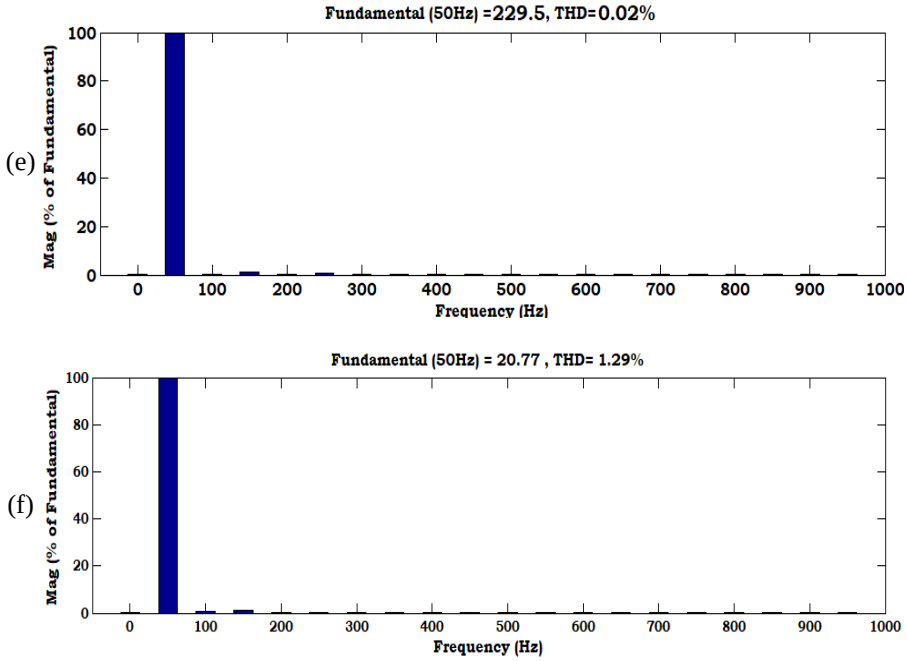


Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (e) THD spectrum of grid voltage and (f) THD spectrum of grid current (continued)

REFERENCES

[1] B. Banfield, P. Ciufo, and D. A. Robinson, "The technical and economic benefits of utility sponsored renewable energy integration," in *2017 Australasian Universities Power Engineering Conference, AUPEC 2017*, Nov. 2018, vol. 2017-November, pp. 1–6, doi: 10.1109/AUPEC.2017.8282489.

[2] M. Shafiullah, S. D. Ahmed, and F. A. Al-Sulaiman, "Grid Integration Challenges and Solution Strategies for Solar PV Systems: A Review," *IEEE Access*, vol. 10, pp. 52233–52257, 2022, doi: 10.1109/ACCESS.2022.3174555.

[3] R. Panigrahi, S. K. Mishra, and S. C. Srivastava, "Grid integration of small-scale photovoltaic systems-a review," in *2018 IEEE Industry Applications Society Annual Meeting, IAS 2018*, Sep. 2018, pp. 1–8, doi: 10.1109/IAS.2018.8544503.

[4] E. Mattos, A. M. S. S. Andrade, G. V. Hollweg, J. Renes Pinheiro, and M. Lucio Da Silva Martins, "A review of boost converter analysis and design in aerospace applications," *IEEE Latin America Transactions*, vol. 16, no. 2, pp. 305–313, Feb. 2018, doi: 10.1109/TLA.2018.8327380.

[5] N. Kakimoto and R. Asano, "Linear operation of photovoltaic array with directly connected lithium-Ion batteries," *IEEE Transactions on Sustainable Energy*, vol. 8, no. 4, pp. 1647–1657, Oct. 2017, doi: 10.1109/TSTE.2017.2698066.

[6] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1198–1208, May 2009, doi: 10.1109/TPEL.2009.2013862.

[7] A. K. Gupta *et al.*, "Effect of various incremental conductance MPPT methods on the charging of battery load feed by solar panel," *IEEE Access*, vol. 9, pp. 90977–90988, 2021, doi: 10.1109/ACCESS.2021.3091502.

[8] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters State of the art, challenges, and requirements in Industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010, doi: 10.1109/TIE.2010.2043039.

[9] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun. 2008, doi: 10.1109/MIE.2008.923519.

[10] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010, doi: 10.1109/TIE.2009.2032430.

[11] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a GaN-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12153–12165, Nov. 2020, doi: 10.1109/TPEL.2020.2989329.

[12] K. N. V. Prasad, G. R. Kumar, T. V. Kiran, and G. S. Narayana, "Comparison of different topologies of cascaded H-Bridge multilevel inverter," in *2013 International Conference on Computer Communication and Informatics, ICCCI 2013*, Jan. 2013, pp. 1–6, doi: 10.1109/ICCCI.2013.6466135.

[13] P. Omer, J. Kumar, and B. S. Surjan, "A review on reduced switch count multilevel inverter topologies," *IEEE Access*, vol. 8, pp. 22281–22302, 2020, doi: 10.1109/ACCESS.2020.2969551.

[14] M. Sarebanzadeh, M. A. Hosseinzadeh, C. Garcia, E. Babaei, S. Islam, and J. Rodriguez, "Reduced switch multilevel inverter topologies for renewable energy sources," *IEEE Access*, vol. 9, pp. 120580–120595, 2021, doi: 10.1109/ACCESS.2021.3105832.

[15] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019, doi: 10.1109/ACCESS.2019.2913447.

[16] V. Janaki Ramaiah and K. Siva Kumar, "A single-phase 5-level inverter topology with reduced semiconductor switches," in *Proceedings of 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems, PEDES 2018*, Dec. 2018,

pp. 1–5, doi: 10.1109/PEDES.2018.8707786.
[17] A. Srivastava and S. P. Singh, "Performance analysis of single stage standalone PV fed novel three level inverter," in *1st IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems, ICPEICES 2016*, Jul. 2017, pp. 1–5, doi: 10.1109/ICPEICES.2016.7853365.
[18] V. S. K. Prasadarao, S. Peddapati, and S. V. K. Naresh, "A single phase seven-level MLI with reduced number of switches employing a PV Fed SIMO DC-DC converter," in *2020 IEEE Students' Conference on Engineering and Systems, SCES 2020*, Jul. 2020, pp. 1–6, doi: 10.1109/SCES50439.2020.9236755.
[19] J. N. Bhanutej, C. Rani, A. Tamil Maran, L. Santhosh, Y. Wang, and K. Busawon, "Performance analysis of 9 level reduced switch cascaded multilevel inverter using phase disposition," in *7th IEEE International Conference on Computation of Power, Energy, Information and Communication, ICCPEIC 2018*, Mar. 2018, pp. 296–304, doi: 10.1109/ICCPEIC.2018.8525209.
[20] M. V. Krishna, G. Satyanarayana, K. L. Ganesh, and D. RaviKiran, "THD optimization of sequential switching technique based hybrid IPD modulation scheme for CMLI," in *2014 International Conference on Science Engineering and Management Research (ICSEMR)*, Nov. 2014, pp. 1–7, doi: 10.1109/ICSEMR.2014.7043573.
[21] K. V. K. Varma, K. Sirisha, G. Satyanarayana, and K. L. Ganesh, "Optimal PWM strategy for 11-level series connected multilevel converter using Hybrid PV/FC/BESS source," in *2014 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2014]*, Mar. 2014, pp. 686–691, doi: 10.1109/ICCPCT.2014.7055042.
[22] G. Satyanarayana and K. Lakshmi Ganesh, "Grid Integration of Hybrid Generation Scheme for Optimal Switching Pattern Based Asymmetrical Multilevel Inverter," in *Lecture Notes in Electrical Engineering*, vol. 326, 2015, pp. 295–303.
[23] K. Lakshmi Ganesh, N. Saida Naik, K. Narendra, and G. Satya Narayana, "A newly designed asymmetrical multi-cell cascaded multilevel inverter for distributed renewable energy resources," *International Journal of Recent Technology and Engineering*, vol. 7, no. ICETESM18, pp. 248–255, 2019.
[24] P. Revathi, K. Jhansi, L. S. Rao, P. Prabhakara Sharma, P. Ramajaneyalu, and S. N. Bashsa, "An improved system performance using ANN-FUZZY logic and MSHO control for BES-solar PV and wind plant based micro-grid system," in *ICISTSD 2022 - 3rd International Conference on Innovations in Science and Technology for Sustainable Development*, Aug. 2022, pp. 10–17, doi: 10.1109/ICISTSD55159.2022.10010644.
[25] G. Satyanarayana and K. L. Ganesh, "Incorporate of FB-MMCs converter topologies for hybrid PV/FC based EV applications," *Procedia Technology*, vol. 21, pp. 271–278, 2015, doi: 10.1016/j.protcy.2015.10.028.

BIOGRAPHIES OF AUTHORS

Pidatala Prabhakara Sharma received obtained his B.Tech. in EEE from KLCE, AP, India. He completed his Master of Technology in High Voltage Engineering from University College of Engineering, JNTUK- Kakinada. AP, India and pursing Ph.D. in Andhra University. He is currently working as Associate Professor in Electrical & Electronics Engineering Department in Kallam Haranadhareddy Institute of Technology, Guntur, AP, India, since 2013. He published more than 20 papers in international journals and conferences. He filed three patents. His area of interest includes Electrical Machines, HVDC, AC-DC Power Flows and Soft computing techniques. He can be contacted at email: prabhakarasharma@gmail.com.

Lingineni Shanmukha Rao received Ph.D. from Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, India in 2016 and M.Tech. in Electrical Power Engineering from Jawaharlal Nehru Technological University (J.N.T.U), Hyderabad, A.P, India in 2006. Now, he is working as Professor and Head of the Department Electrical and Electronics Engineering at Kallam Haranadhareddy Institute of Engineering and Technology, Guntur, A.P., India. He authored four books and published more than 25 research papers in international journals and conferences. His research interests include power system modeling and control, renewable energy sources and soft computing techniques. He can be contacted at email: lsrlingineni@gmail.com.

Goddanti Amulya is an Under Graduate student studying IV B.Tech. Electrical and Electronics Engineering from Kallam Haranadhareddy Institute of Engineering and Technology, Guntur, A.P., India. She is one of the topper at the college level who got meritorious scholarship and won many prizes in the technical events held at intra and inter college level. Her research interests include renewable energy sources. She can be contacted at email: amulya.goddanti@gmail.com.