International Journal of Applied Power Engineering (IJAPE)
Vol. 13, No. 3, September 2024, pp. 554~570
ISSN: 2252-8792, DOI: 10.11591/ijape.v13.i3.pp554-570

A new step-up DC-DC converter topology using switched inductor and switched capacitor networks for high negative DC voltage applications

A. Clement Raj, Ramaiyan Bensraj
Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology,
Annamalai University, Chidambaram, India

Article Info

Article history:

Received Sep 9, 2023
Revised Feb 11, 2024
Accepted Mar 8, 2024

Keywords:

Continuous conduction mode
High-gain Cuk converter
Renewable energy sources
Switched-capacitor
Switched-inductor

ABSTRACT

This study presents a novel topology for a high-gain Cuk converter without isolation, leveraging switched-inductor (SL) and switched-capacitor (SC) networks tailored for renewable energy sources. Unlike traditional Cuk converters that perform negative-to-positive boost DC-DC voltage conversion, this innovative design offers a significantly enhanced voltage-boosting capacity. They evolve from the conventional Cuk converter by integrating an SL instead of the singular inductor and substituting the energy-transferring capacitor with an SC. The standout benefits of the modified Cuk converters include a remarkable voltage conversion ratio and minimized voltage stress on the primary switch, allowing a low-voltage-rated switch for greater efficiency. Comparatively, the proposed designs surpass the classical Cuk and a few modified Cuk converters in voltage gain and reduced switch voltage stress. The converter also avoids the need for transformers or coupled inductors, resulting in minimized volume, loss, and expense. The converters' operation in continuous conduction mode is rigorously analyzed in this study. After deriving all the relevant equations, they are validated against outcomes. The proposed Cuk converter topology was simulated using the MATLAB/Simulink tool, and the findings are deliberated. The performance of the proposed converter is compared with the other converters, and the proposed converter's superiority is proved through the obtained results.

Corresponding Author:

A. Clement Raj
Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology
Annamalai University
Chidambaram 608002, Tamil Nadu, India
Email: clementlecturer1@gmail.com, clementlecturer@gmail.com

1. INTRODUCTION

In the modern era, the application of DC-DC converters has witnessed a significant upswing across various industries and sectors. Such converters are pivotal in various systems and devices, from computer systems, medical apparatuses, and servo motors to light emitting diode (LED) illumination solutions [1], [2]. Their reach extends further to other realms, such as power factor correction, telecommunication systems, auxiliary equipment in hybrid vehicles, and everyday portable devices like mobile phones and laptops [3]. One cannot overlook their immense contribution to ensuring uninterrupted power supplies and facilitating the operation of green energy systems. This includes systems powered by fuel cells, photovoltaic (PV) systems, and wind turbine setups [4], [5]. Over the years, the scientific community has displayed a growing interest in

renewable energy sources, particularly in PV systems, for electricity generation. This surge in interest stems from the global need to address persistent environmental problems and search for sustainable alternatives to traditional energy sources. However, one of the primary challenges associated with these renewable energy sources is their inherently low and unregulated DC output voltage. There is a demanding requirement to enhance this low voltage to a more usable, regulated, and higher level [6], [7]. To achieve this, power electronic conditioning is employed. The specifications of the power electronic interface play a crucial role. They are influenced by the characteristics of the renewable energy source and the broader implications on the overall power system's operation. Historically, the conventional non-isolated DC-DC converter was the choice to execute the voltage step-up function. Its simplistic design, ease of control, and affordability gained popularity. However, this conventional converter faced its own set of limitations. Specifically, its efficiency was curtailed due to the parasitic elements inherent in its design. This converter must operate at an exceptionally high-duty cycle to achieve a high voltage gain [8]–[10].

These advanced power electronic converters primarily operate under the guidance of pulse width modulation) and predetermined switching frequencies. Depending on the modus operandi of the pulse width modulated (PWM) technique, these converters are broadly bifurcated into two categories: isolated and non-isolated [9]–[11]. Isolated DC-DC converters integrate a high-frequency transformer, encompassing flyback, forward, half-bridge, full-bridge, and push-pull configurations [12], [13]. This inclusion enables achieving a high voltage, dictated primarily by altering the number of transformers turns. However, while these transformers can be instrumental, they introduce certain challenges. Predominantly, high-frequency transformers can inadvertently escalate the overall cost of the setup. Moreover, they might be responsible for high switching voltages and incur significant energy losses from the transformer's leakage inductance [14]. Non-dissipative snubber or active clamp circuits are often integrated to combat these issues. While they can mitigate some of the challenges the transformers pose, they unintentionally increase the converter's cost and size [15]. Furthermore, they tend to make the control process more intricate. On the other hand, non-isolated DC-DC converters, including configurations like buck, boost, buck-boost, Cuk, and single-ended primary inductor converter (SEPIC), function without needing a high-frequency transformer [16]–[19]. Consequently, these converters offer many advantages: they are generally more cost-effective, compact in size, and showcase reduced switching losses. This inherent design advantage also translates to higher operational efficiency.

This intense operational demand introduced a range of problems: significant voltage stress on the semiconductors, complications related to diode reverse recovery, and a substantial switching loss. These problems took a toll on the system's overall performance and efficiency. An attempt to counter these limitations was made by introducing the cascaded boost converter [20]. This converter was designed to address several challenges posed by its conventional counterpart. For instance, it could achieve a commendable voltage gain without operating at a drastically high duty cycle. Additionally, the voltage stress experienced by the switches in this converter was considerably less than the voltage experienced across the load. However, it was not without its drawbacks. The cascaded boost converter was associated with higher energy losses, reduced efficiency, and electromagnetic interference issues [21]. Further advancements in the field led to the development of switched-capacitor-based converters [17], [22], [23] and hybrids that combined switched capacitors and switched inductor [24]–[28] mechanisms. These advanced converters promised high-voltage gains even at smaller duty cycles and minimized voltage stress across their switches, making them suitable for a diverse power range. Yet, they faced challenges, such as increased energy losses, reduced efficiency, problems with electromagnetic interference, and persistent diode reverse recovery problems [29], [30].

A high-gain DC/DC converter [31], employs coupled inductor and voltage multiplier cell techniques. This converter notably achieves a high gain at a small duty ratio and ensures reduced voltage stress on semiconductor components. However, there are some challenges associated with this design. It operates based on hard switching, which can curtail the lifespan of its components. Additionally, including the voltage multiplier cell augments the system's overall size and cost. The authors of [32]–[34] introduce magnetically coupled inductor topologies. These topologies enhance the output voltage gain of the converter by transferring energy stored in coupled inductance. Additionally, they help in reducing the normalized voltage stress across the semiconductors. However, these systems necessitate a clamping circuit to counteract switching spikes and manage the leakage energy, which can induce voltage spikes and ringing. Another notable mention is the high voltage gain quasi-Z-source DC/DC converter [26]. It promises a high voltage gain with a low-duty cycle, keeping the voltage stress on the semiconductors to a minimum. However, the drawback is its operation with hard switching, leading to increased losses. This impacts overall system performance and efficiency. Moreover, its utility is limited to duty cycles under 0.3. The previous studies [35], [36], a single switch DC/DC converter incorporating non-coupled inductors has been introduced. It offers a high voltage gain paired with commendable efficiency. The downside is its reliance on many passive components, resulting in a bulkier and costlier system. The p-type DC/DC converter [37]–[39], boasts

advantages such as continuous input current, common ground, high gain at smaller duty cycles, and minimizing voltage stress on semiconductor devices. However, the model comes with its own set of challenges. It utilizes hard switching and demands many components, enlarging the system's footprint, and escalating its cost. The single switch three-Z-network converter [40], [41] stands out for its high voltage gain. But, similar to previous models, its reliance on numerous passive components amplifies losses and curtails efficiency. The impedance network DC/DC boost converter [42], [43], achieves a high voltage gain using a limited number of diodes and a small duty cycle. This design effectively sidesteps instability issues stemming from inductor saturation. However, efficiency remains a challenge for this converter. Duong *et al.* [44] and Shahir *et al.* [45] introduce a step-up DC/DC converter incorporating switched capacitor cells. The converter can achieve a high voltage gain at reduced duty ratios and keep voltage stress on switches and capacitors low. Furthermore, this design offers scalability. Nevertheless, the significant count of active and passive components boosts the converter's size and cost.

The studies documented in [46], [47], novel designs for non-isolated DC-DC boost converters have been presented. This technique has significantly augmented voltage gain, furnishing a robust method to elevate voltage levels. However, this method is not devoid of shortcomings. A noticeable trend is that as the voltage gains ascend to higher thresholds, there is a corresponding increase in the number of components utilized. Moreover, the voltage stress endured by the switches escalates, making the design of its control systems markedly intricate, thereby compounding the complexity of the entire setup. The developments have marked further progression in this domain showcased in [48], [49], where in efforts have been channeled to better the adverse voltage stress impacting the switches, thus aiming to augment the longevity and efficiency of the system. Expanding upon the methodologies, Luo *et al.* [50] and Farakhor *et al.* [51] introduce the application of a coupled inductor to bolster the voltage gain. This innovative approach promises not only heightened voltage gain but also superior efficiency. This is chiefly attained through the modulation of the coupled inductor's turns ratio and harnessing the energy recovery potential of leakage inductance. Additionally, this technique promises a low off-state voltage for the primary switch, as delineated in [50], which can potentially streamline the energy transition process. However, this method is accompanied by a series of limitations, including a pronounced input current ripple, which necessitates a substantial input filter, thus constraining its widespread application. Moreover, it is marred by issues such as an increase in both size and cost and a delayed diode reverse recovery time, engendered by the leakage inductance of the coupled inductor, as pointed out in [52]. Shifting the focus to the non-isolated DC-DC converters that employ series and parallel connections, as depicted in [52], [53], the primary objective is to attain heightened voltage levels and efficiency across a broad spectrum of alterations while restricting the number of active operational switches. This strategy has found a place in renewable energy applications, signifying its potential contribution to fostering sustainable energy solutions. Nonetheless, this technique is beleaguered by drawbacks, including high losses and pronounced current ripple across the switches. Moreover, the switches and semiconductor components are subject to elevated current and voltage stress levels, hindering optimal performance, especially at lower voltage levels. The intricacies of switch control, combined with the substantial size and high costs, pose significant challenges to achieving stability and economic viability. Attempts to mitigate the high-stress environments for switches and semiconductor components have seen the incorporation of coupled inductors [54], [55], thereby presenting a pathway to refine this technology further and possibly overcoming some of its inherent limitations.

The need for efficient and compact DC-DC converters with high voltage gain is ever-increasing in power electronic systems. The switched-inductor (SI) and switched-capacitor (SC) based high step-up converters are at the forefront in meeting high efficiency and high voltage gain demands in various applications such as renewable energy systems and electric vehicles. The SI converters, a subset of inductor-based converters, are renowned for achieving high step-up voltage conversion ratios. The following features generally characterize them: i) The SI converters usually provide high efficiency, particularly in high-power applications; ii) The SI converters more often operate in continuous conduction mode (CCM), offering reduced current ripple and stress on components; iii) The complexity in design increases with higher step-up ratios, potentially involving many magnetic components and complex control strategies; and iv) The SI converters associated with higher costs, especially when dealing with a higher number of components and more sophisticated control strategies. The SC converters have emerged as a promising alternative, offering several distinctive advantages: i) The SC converters eliminate the need for magnetic components, resulting in a potentially more compact and lightweight design; ii) The SC converters can be designed in a modular fashion, facilitating easy scalability; iii) The SC converters often operate in discontinuous conduction mode, which may introduce higher voltage ripple and require additional filtering; and iv) The control schemes can be simpler compared to SI converters, but optimizing performance still requires careful design.

Recent advancements have seen the integration of both SI and SC stages in a single converter to harness the benefits of both topologies. Such hybrid converters potentially offer: i) Even higher step-up ratios

by combining the merits of both topologies; ii) Optimization of both stages can lead to improved overall efficiency; and iii) Allows for a more flexible design approach, catering to specific application requirements. Therefore, the SI and SC-based high step-up DC-DC converters have unique attributes that make them suitable for different applications. These topologies continued evolution and integration signal a promising direction in high-step-up DC-DC converters, fostering innovation and efficiency in power electronic systems. The above discussions motivated this study to propose a new DC-DC converter topology by integrating both SI and SC networks with the traditional Cuk converter. Therefore, the proposed converter is named as modified Cuk (MCUK) converter. The proposed converter maintains important features of the Cuk converter, such as continuous input current and negative output voltage. In addition, the proposed converter provides high-voltage gain. The conversion efficiency of the proposed converter is much better than the original Cuk converter and a few other modified versions of the Cuk converter. The major contributions are listed as:

- Formulation of a new variant of Cuk-converter topology by integrating SC and SI approaches.
- Designed to produce the continuous input current and negative output voltage.
- Simulated the performance of the proposed converter.
- Performance comparison with the original Cuk converter and other variants of the Cuk converter.

The paper is structured as follows. Section 2 discusses the modes of operation of the proposed MCUK converter. Section 3 discusses the steady-state analysis of the proposed converter under CCM. Section 4 discusses the results obtained through the MATLAB/Simulink tool. Section 5 concludes the paper.

2. MODIFIED CUK DC-DC CONVERTER

This section briefly introduces the operation of the original Cuk converter. It also elaborately discusses the mode of operation of the proposed MCUK converter. The current path in each mode is highlighted in this section.

2.1. Cuk converter

Figure 1 introduces the schematic of the traditional Cuk converter. This intricate device can reduce the input voltage level while concurrently achieving a polarity inversion, a characteristic similar to the functionalities offered by the buck-boost converter. A closer inspection reveals that the core structure of this converter is constituted of several elements, including one active switch and a diode. The device incorporates two inductors and capacitors to facilitate optimal operation. These components collectively establish a platform where a negative output relative to the ground can be actualized, a requisite in regulated DC power supplies [40]. Further delving into its operational specifics, the voltage conversion ratio inherent to a conventional Cuk converter is shown in (1).

$$A = \frac{V_o}{V_i} = -\frac{D}{1-D} \tag{1}$$

Where D denotes the duty cycle of the semiconductor switch, V_o denotes the output voltage of the converter and V_i denotes the input voltage to the converter. This equation plays a pivotal role in establishing the working parameters of the converter, defining the constraints of the voltage levels and polarity inversions marked by a negative sign, as illustrated in (1). However, it is critical to note that there are certain limitations to the operational capabilities of these converters, particularly in terms of the maximum allowable value for the duty cycle, D.

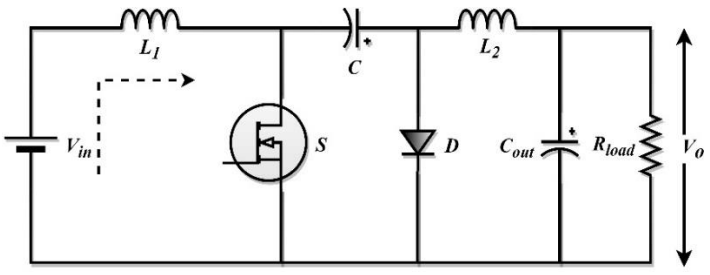


Figure 1. Schematic of the original Cuk converter

As stipulated in [56], maintaining a duty cycle beyond 0.8 could potentially impede the boost voltage capacities of these converters due to the detrimental effects of parasitic components that come into

play under such circumstances. In terms of operational versatility, the conventional Cuk converter can function under three distinct modes: the buck mode, boost mode, and the hybrid buck-boost mode [57], [58]. This multifaceted functionality gives several advantages, including incorporating an energy transfer capacitor, which contributes to optimal steady-state performance, continuous input and output currents, and minimized output voltage ripple, as testified by the findings [16], [57]. When subjected to a comparative analysis against various other converters, the Cuk converter exhibits distinct benefits, including the buck, boost, buck-boost, single-ended primary inductor converter, Luo, and Zeta. The Cuk converter stands superior to other conventional non-isolated DC-DC converters. Notably, it promises an open operational boundary, coupled with steady, non-pulsating input and output currents, which negate the necessity for external filtering mechanisms. Moreover, its switch control terminal is grounded, a design aspect that significantly streamlines the configuration of the gate drive circuitry. Despite its remarkable advantages, the references [59]–[61] indicate that variations of Cuk converters developed using different techniques have been confined to lower voltage conversion ratios. Nevertheless, promising advancements have been proposed to mitigate this limitation. The integration of SI and SC topologies has been explored as a viable strategy to achieve enhanced voltage gains, paving the way for developments in the field of DC-DC converters.

2.2. Proposed MCUK converter

The MCUK converter emerges as a variation of the traditional Cuk converter, undergoing modifications in two primary components, i.e., hybridization of SI and the SC at the output stage of the original Cuk converter. As depicted in Figure 2, this illustrates the updated power circuit diagram representative of the MCUK configuration. Upon comparison with the Cuk model, the new design presented in Figure 2 incorporates additional elements to enhance its functionality. Specifically, the expansion includes an extra inductor and capacitor, complemented by four additional diodes, thereby promising to elevate the efficacy. The suggested modifications to the Cuk converters are being inspected under the CCM. Within this operational framework, the functionality of the proposed MCUK can be divided into two distinct modes. The first is the ON mode, characterized by the conduction of switch S, and the second is the OFF mode, witnessed when switch S1 stops to conduct electricity.

2.2.1. Mode 1

In the specified scenario where the switch labelled as S is actively conducting, a deeper examination of the current pathway can be observed in the representation provided in Figure 3(a). Here, the prominent role played by the inductor, denoted as $L1$, becomes evident. Initially, the inductor $L1$ undergoes a charging phase, where it is energized by the input supply voltage, designated as V_{in}. This process occurs through the direct involvement of the switch S, facilitating the energy transfer from the voltage source to the inductor $L1$. As this emerges, it is noteworthy that a synergy involves the discharged energy harnessed from the capacitors labelled $C1$ and $C2$. Now, focusing on the comprehensive dynamics of the energy transfer, it becomes evident that the discharged energy of capacitors $C1$ and $C2$ collaborates with the input supply voltage V_{in} to fulfil a dual role. Primarily, it provides the necessary energy supply to the load, ensuring the sustenance of the operational requisites. Concurrently, it also energizes the inductors denoted as $L2$ and $L3$, initiating a charging phase. This particular segment of the circuit illustrates a parallel connection between the said inductors, facilitating their simultaneous charging through the direct mediation of diodes $D3$ and $D4$ in conjunction with the actively conducting switch. In this operation phase, it is essential to highlight the status of the diodes labelled $D1$, $D2$, and $D5$.

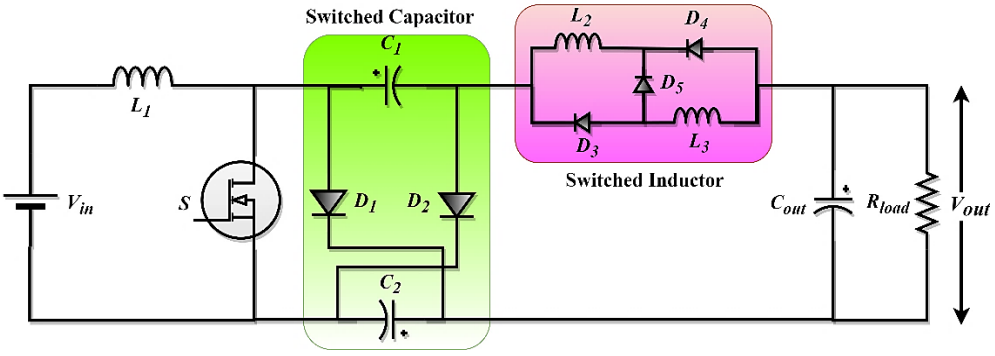


Figure 2. Schematic of the proposed MCUK converter

As the circuit navigates through this mode, these diodes assume a reversed-biased, effectively becoming non-conductive and isolating the components or pathways they are connected to from the current flow occurring in this cycle phase. A critical aspect that merits attention here is the uniformity in the current distribution involving inductors $L2$ and $L3$. These inductors are identical in their properties and characteristics, facilitating an even distribution of current, channeling an equal amount of current flow through each. This characteristic embodies synchronicity in the energy transfer process, ensuring a balanced and efficient operational mechanism during the phase where the switch is actively conducted.

2.2.2. Mode 2

In the alternate phase of the operational cycle, where the switch ceases to conduct, the specific pathway followed by the current is vividly illustrated in Figure 3(b). This depiction allows us to delve deeper into the nuanced dynamics of the circuit during this non-conductive phase of the switch. At this juncture, the primary energy source, designated as the input supply voltage V_{in}, plays a pivotal role, joining forces with the energy released from the discharge of the inductor $L1$. This conjoint energy now seeks to facilitate the charging of the capacitors labelled $C1$ and $C2$, arranged in a parallel configuration within the circuit. This setup allows for an efficient and simultaneous charge accumulation in both capacitors, setting the stage for the subsequent stages of the cycle. Simultaneously, another critical energy transfer involves the inductors $L2$ and $L3$. The energy stored in these inductors, now in a discharged state, channelizes its energy to fulfil two vital functions in the circuit. Initially, this energy is directed towards charging the capacitors $C1$ and $C2$, thereby adding to the energy pool accumulated from V_{in} and the discharged inductor $L1$. Furthermore, this released energy from $L2$ and $L3$ takes up the role of powering the load, thus ensuring a consistent energy supply during the non-conductive phase of the switch. A notable shift in the diodes D3 and D4 status is observed at this point. These components assume a reversed-biased position, hindering current flow through their respective pathways. This configuration effectively isolates certain segments of the circuit, directing the current flow along the desired pathways to facilitate the charging of capacitors and supply the load.

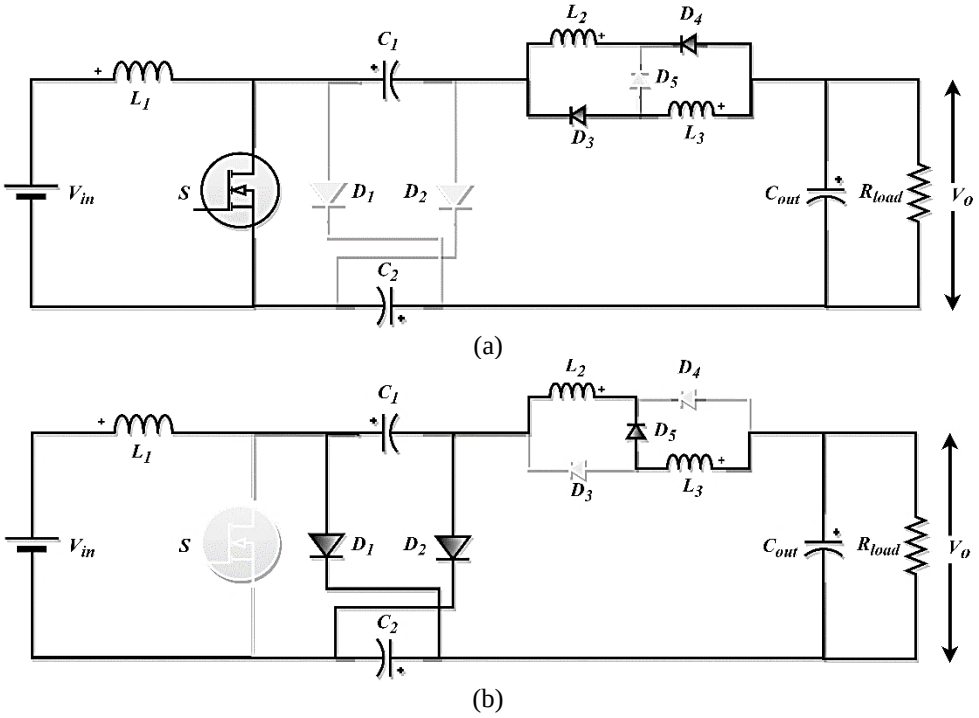


Figure 3. Modes of operation (a) mode 1 and (b) mode 2

A comprehensive understanding of the circuit's behavior in this phase is further enriched by referring to Figure 4, which depicts the CCM of the entire process. This figure showcases the main steady-state waveforms, representing the complicated variations during one cycle period in greater detail. It serves as a vital tool in understanding and analyzing the circuit's behavior in-depth, allowing for an enhanced perception of the functional intricacies involved in the non-conductive phase of the switch.

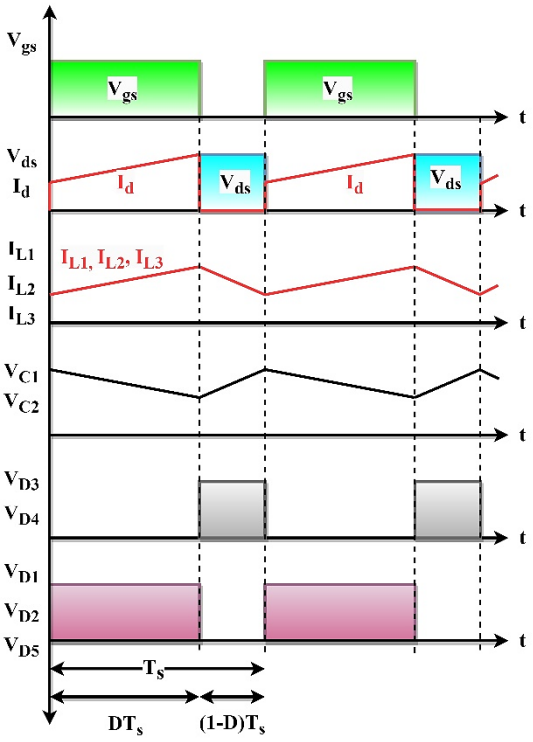


Figure 4. Theoretical waveforms of the proposed converter under CCM

3. CIRCUIT ANALYSIS AND COMPARISON

3.1. Steady-state analysis

To facilitate a streamlined evaluation of the proposed converter, it must be understood that it operates in a steady-state mode. Here are a few foundational assumptions that reinforce this analysis:

- The system presumes that all components function with flawless efficiency, exhibiting a 100% operational rate.
- The input voltage involved in the process is exclusively DC, without any AC components.
- All capacitors within the system have been meticulously engineered to secure a minimal voltage fluctuation even at the switching frequency.

Considering these key assumptions, we can proceed with a clear and precise evaluation of the converter's performance and efficiency. The voltage level across $L1$, $L2$, and $L3$ can be represented according to (2) and (3) while the switch is in the operational or conducting state. To enhance clarity, it is assumed that the capacitor values of $C1$ and $C2$ are equal, denoted as $C1 = C2 = C$.

$$V_{L_1} = V_{in} \tag{2}$$

$$V_{L_2} = V_{L_3} = 2V_C - V_{out} \tag{3}$$

The voltages across $L1, L2$, and $L3$ can be defined according to (4) and (5) when the MOSFET is in an inactive or turned-off state. To enhance clarity, it is assumed that the capacitor values of $C1$ and $C2$ are equivalent, denoted as $C1 = C2 = C$.

$$V_{L_1} = V_{in} - V_C \tag{4}$$

$$V_{L_2} = V_{L_3} = \frac{V_C - V_{out}}{2} \tag{5}$$

The use of the volt-second balance concept shown as (6) and (7).

$$V_{in} \times D + (1 - D) \times (V_{in} - V_C) = 0 \tag{6}$$

$$D \times (2V_C - V_{out}) + (\frac{V_C - V_{out}}{2}) \times (1 - D) = 0 \tag{7}$$

The voltage across capacitors $C1$ and $C2$ is now determined, as shown in (8).

$$V_{C1} = V_{C2} = V_C = \frac{1}{(1-D)} V_{in} \quad (8)$$

The appropriate voltage gain for the suggested converter is then provided in (9).

$$A = \frac{V_{out}}{V_{in}} = \frac{3D+1}{(1-D)(1+D)} \quad (9)$$

One can develop a formula to calculate the current for the input inductor L1 by using Figures 3(a) and 3(b) as a guide. The equation $I_{L1} = I_{Lin}$ can be derived from (9), as shown in (10).

$$I_{L_{in}} = I_i = \frac{3D+1}{(1-D)(1+D)} I_o = \frac{(3D+1)P_o}{(1-D)(1+D)V_o} \quad (10)$$

Referring to Figures 3 and 4, one can derive an equation that facilitates the computation of the current flowing through the two output inductors. The (12) is derived from (11) by assuming that the inductance values of the two output inductors, I_{L2} and I_{L3}, are equal, resulting in $I_{L2} = I_{L3} = I_{Lout}$.

$$I_o = 2I_{L_{out}} D + I_{L_{out}}(1 - D) \quad (11)$$

$$I_{L_{out}} = \frac{I_o}{(1+D)} = \frac{P_o}{(1+D)V_o} \quad (12)$$

The reverse voltage across $D1$, $D2$, and $D4$ of the SC and SI while they are in the state of blocking (ON-mode) is presented in (13) and (14).

$$V_{D_1} = V_{D_2} = \frac{V_{in}}{(1-D)} \quad (13)$$

$$V_{D_5} = \frac{V_{in}}{(1+D)} \quad (14)$$

The expression for the voltage stress across the power switch and the diodes D3 and D5 in the blocked or OFF mode is given by (15) and (16), respectively.

$$V_S = \frac{V_{in}}{(1-D)} \quad (15)$$

$$V_{D_3} = V_{D_4} = \frac{D}{(1-D)(1+D)} V_{in} \quad (16)$$

The inductor currents at the input are represented as $\triangle i_{L1} = \triangle i_{Lin}$, and at the output, indicated by $\triangle i_{L2} = \triangle i_{L3} = \triangle i_{Lout}$, is presented in (17) and (18).

$$\triangle i_{L_{in}} = \frac{DV_{in}T}{L_{in}} = \frac{V_{in}D}{L_{in}f} \quad (17)$$

$$\triangle i_{L_{out}} = \frac{TD(2V_C - V_{out})}{L_{out}} = \frac{D(2V_C - V_{out})}{L_{out}f} \quad (18)$$

The peak-to-peak change of the voltage across the capacitor, denoted as $\triangle v_{C1} = \triangle v_{C2} = \triangle v_C$ is presented in (19).

$$\triangle v_C = \frac{DTI_o}{C} = \frac{DP_o}{AV_{in}fC} \quad (19)$$

3.2. Performance comparison

In an intricate exploration of different converter configurations, this research compares the newly proposed MCUK converter against its conventional counterparts - namely, the classical Cuk, classical boost, enhanced Cuk 1 (ECUK1) [16], and ECUK2 [17] converters. These comparisons are systematically articulated in Table 1, providing a convenient reference for analysis and scrutiny. Analyzing the specifics, it is evident that the MCUK converter topologies have a superior edge over the conventional versions regarding

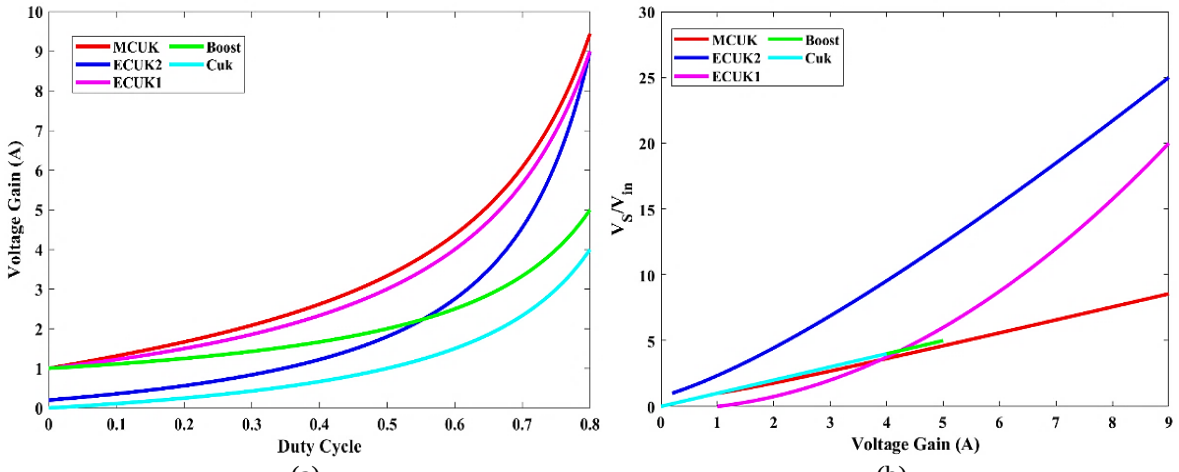
voltage gain, implying they can improve a given input voltage to a substantially higher output voltage. This innovative MCUK topology emerges as the peak of voltage gain improvements. Moving beyond the mere aspect of voltage gain, it is imperative to consider another vital dimension that influences the efficiency and durability of these configurations: the voltage stress imposed on the components. This study zeroes in on the normalized voltage stress, represented as $\frac{V_S}{V_{in}}$, on the main switch. This parameter sheds light on the voltage stress endured by the MOSFET switch. It is crucial to note that higher voltage stress can precipitate early degradation and possible component malfunction, making a reduced value typically more favourable. Consequently, a graphical depiction illustrating this enhanced performance has been encapsulated in Figure 5(a), facilitating a more bright and comprehensible adaptation of the information.

Table 1. Comparison among the peers

Topology	Cuk	MCUK	ECUK1	ECUK2	Boost
MOSFETs	1	1	1	1	1
Diodes	1	5	2	4	1
Capacitors	2	3	2	4	1
Inductors	2	3	2	3	1
Voltage stress	$\frac{D}{1-D}$	$\frac{3D+1}{(1-D)(1+D)}V_{in}$	$\frac{1+D}{1-D}V_{in}$	$\frac{D(1-D)+1}{(1-D)^2}$	$\frac{1}{1-D}$
Voltage gain	$\frac{D}{1-D}$	$\frac{1}{(1-D)}$	$\frac{1}{(1-D)}$	$\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$

To provide a detailed and comprehensive understanding, this study has measured and compared the normalized voltage levels of the newly proposed converter design with those of the classic Cuk converter, as well as its various modified versions and the boost converter. This comparison is an important step to measure the performance and improvement the new design brings. The normalized voltage is an important parameter in assessing the efficiency and reliability of a converter. It gives us a clear indication of the voltage stress that components are subjected to during the operation of the converter. Lower values are preferable as they signify lesser stress on the components, potentially leading to a longer lifespan and reduced risk of failure. Visually represented this data in Figure 5(b) to allow for an easier and more intuitive understanding of the findings. Visual representation aids in quickly grasping the differences and advantages of the new design compared to others.

When looking at Figure 5(b), it is clear that the proposed MCUK maintains lower voltage stress compared to traditional designs and excels remarkably, exerting the minimum voltage stress on its components. This proves its superior design, as it minimizes the potential wear and tear on the components, promising better performance and improved reliability and durability. In essence, the new converter is the best choice, standing as the clear winner in this comparative analysis, demonstrating both innovation and efficiency in its design and operation.



(a) (b)

Figure 5. Performance comparison (a) output voltage gain and (b) voltage stress of the MOSFET

4. RESULTS AND DISCUSSIONS

This study introduces an advanced Cuk DC-DC converter called MCUK to operate with a source voltage of 24 V. This innovative device has a substantial power capacity of 200 W, marking it a robust tool in electrical conversions. Its inner workings are regulated at a switching frequency of 75 kHz, a rate that is adept at ensuring efficiency and stability during the conversion process. Furthermore, the MOSFET switch incorporated within this converter is programmed to operate at a 65% duty cycle, a proportion that balances performance with energy conservation, contributing to its overall efficiency. In order to ascertain the viability and performance metrics of this proposed converter, it underwent a series of rigorous testing procedures using MATLAB/Simulink software. This software facilitates a conducive environment where the converter's characteristics and functionalities can be observed in a controlled, virtual setup before being employed in real-world applications, guaranteeing its reliability and effectiveness. For those seeking a deeper insight into the technical attributes and specifications of the MCUK converter topology, a detailed enumeration has been compiled and presented in Table 2. This table is a repository of vital information, offering readers an in-depth perspective on the converter's electrical specifications, thereby allowing for a more comprehensive understanding and analysis of its performance metrics and potential applications in various fields.

Table 2. Electrical specifications of the recommended Cuk converter

S.No.	Parameters	Ratings
1.	Source voltage V_{in}	24 V
2.	Duty cycle D	0.7
3.	Power output P_{o}	100 W
4.	Output voltage V_o	-145 V
5.	Inductors (L_1, L_2, and L_3)	600 μH
6.	Load resistance R_L	210 Ω
7.	Switching frequency f_s	50 kHz
8.	Capacitors (C_1 and C_2)	22 μF

The MCUK converter has been carefully designed to provide an output voltage of roughly -145 V. A graphical depiction effectively captures the MOSFET's voltage and current stresses. Figure 6 depicts the existing levels of current and voltage strains experienced by the MOSFET. Figure 6(a) depicts the gating signal, Figure 6(b) illustrates the MOSFET voltage stress, and Figure 6(c) illustrates the MOSFET current stress. The stresses experienced by a MOSFET are crucial factors that significantly influence its efficiency and lifespan. The voltage stress experienced by this MOSFET reaches a maximum value of approximately 80 V peak. Simultaneously, the maximum magnitude of the current stress is approximately 6 A peak.

In Figures 7(a) and 7(b), we can observe the voltage stress on the two diodes, D1 and D2, that are connected to the SC. Both diodes are under a voltage stress of about -80 V. Diodes D3 and D4 principally determine the inductor's charging and discharging phases. In order to prevent back-feeding into the source, the diode D4 frequently serves as a channel for circulating currents or as a protective diode. When the MOSFET is inactive (or in its off-state), both the D1 and D2 diodes are conducting; however, when the MOSFET is operational (or in its on-state), these diodes stop conducting, as shown in Figures 7(a) and 7(b). According to the configuration and state of the switching devices, the SI cell frequently employs three diodes (D3, D4, and D5) and two inductors. The MOSFET charges the inductor when it is ON. Depending on the situation, the inductor discharges while the switching device is OFF, sending energy to the load or back to the source. D5 is reverse-biased as the inductor charges up during the MOSFET active state. As shown in Figure 7(c), the voltage across D5 is negative (the magnitude depends on the voltage source and the level of inductor charging). The inductor might discharge when the MOSFET switch is off because D5 conducts when it is forward-biased. The voltage across D5 decreases to zero or a very low value. D3 is in reverse bias when the switch is turned on. As shown in Figure 7(d), a strong negative voltage results from adding the inductor and output voltage to the voltage across D3. If the inductor voltage exceeds the output voltage when the MOSFET switch is OFF, D3 becomes forward-biased and conducts. Throughout this time, the voltage across D3 is almost nil. Depending on the load and source conditions, D4 may be forward-biased while the MOSFET switch is ON. The voltage across this diode may occasionally be zero or very close to zero, as seen in Figure 7(e), because it prevents any back-feed to the source. D4 is reverse-biased while the MOSFET switch is OFF, carrying the voltage differential between the source and the inductor. The dynamics of the inductor and the states of the switching devices affect the voltage waveforms across the diodes.

The current waveforms for the L1, L2, and L3 inductors are shown graphically in Figure 8. Figure 8(a) represents the current through the inductor L1, Figure 8(b) represents the current through the inductor L2, and Figure 8(c) represents the current through the inductor L3. When the MOSFET is operational (ON), these inductors operate in a charging process. This is how they operate in relation to MOSFETs. These

inductors start to discharge as soon as the MOSFET transitions to its off-state. The source supplies energy to charge L1 when MOSFET is ON (refer to Figure 8(a)). The source's voltage causes a linear increase in the current. Through the capacitors of the SC circuit, the input source and the load, the inductor L2 gets charged, and the current slowly rises (refer to Figure 8(b)). The arrangement suggests that while MOSFET is ON, L3 also has a way to charge (refer to Figure 8(c)). Both inductors L2 and L3 experience an increase in current as the discharge energy of the capacitors charges them during the ON period of the MOSFET. L2 and L3 need a way to release their accumulated energy when MOSFET is turned OFF through the diodes D1, D2, and D5 and charges the capacitors. The inductor L1 and the input source also charge capacitors C1 and C2.

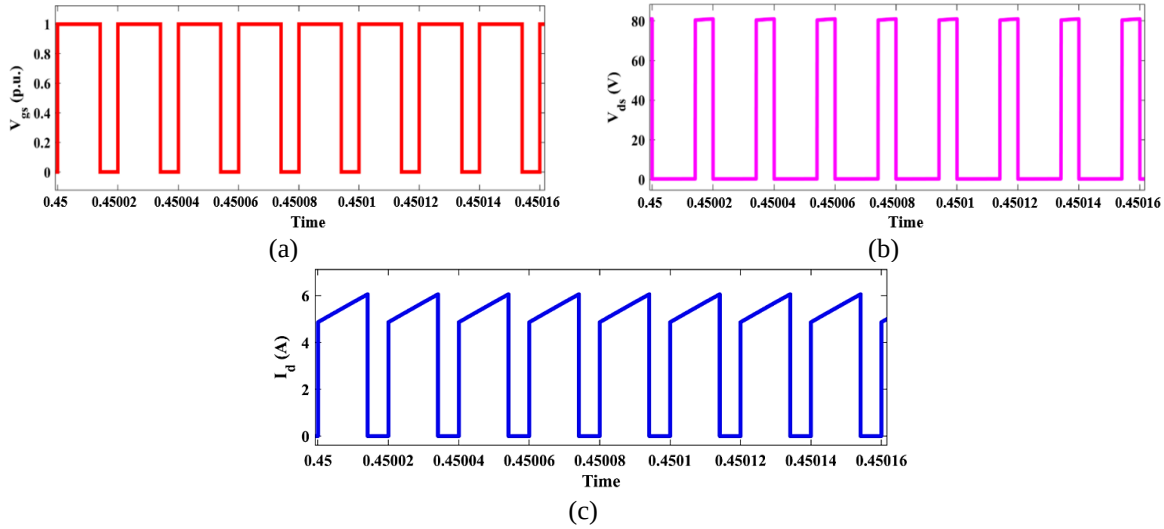


Figure 6. Current and voltage waveforms of the MOSFET (a) gating signal, (b) voltage stress, and (c) current stress

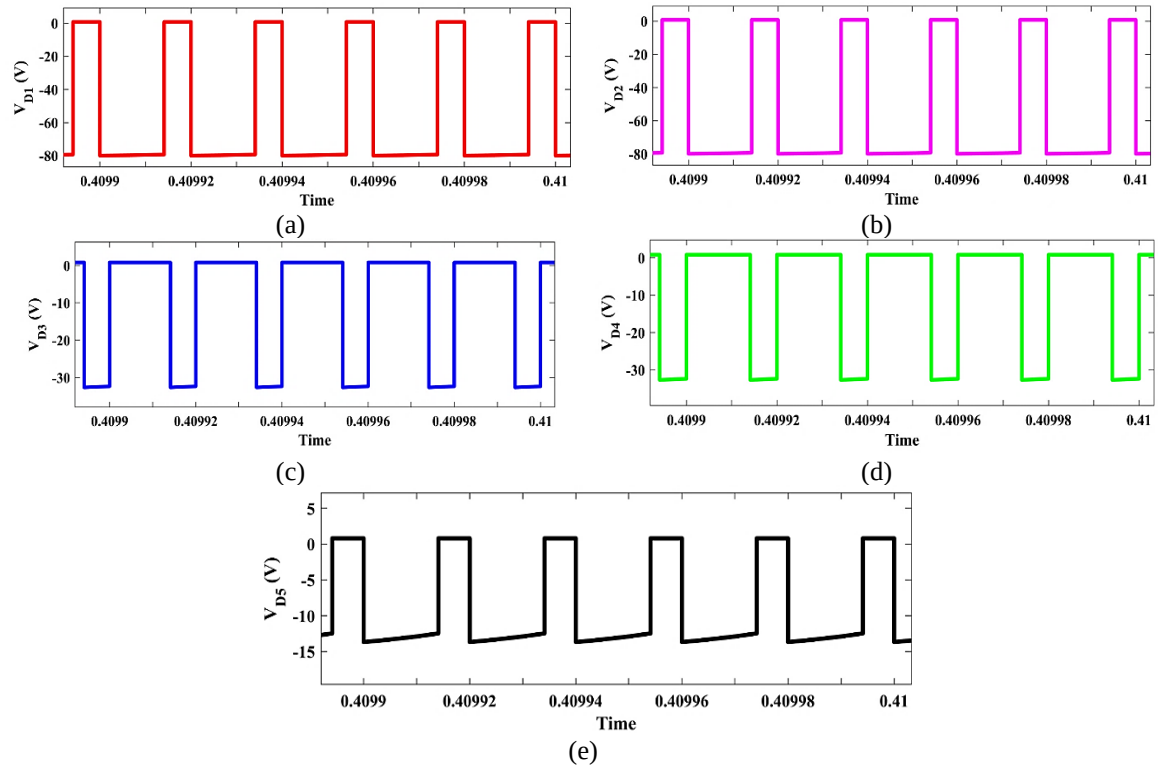


Figure 7. Voltage waveforms of SI and SC diodes (a) V_{D1}, (b) V_{D2}, (c) V_{D3}, (d) V_{D4}, and (e) V_{D5}

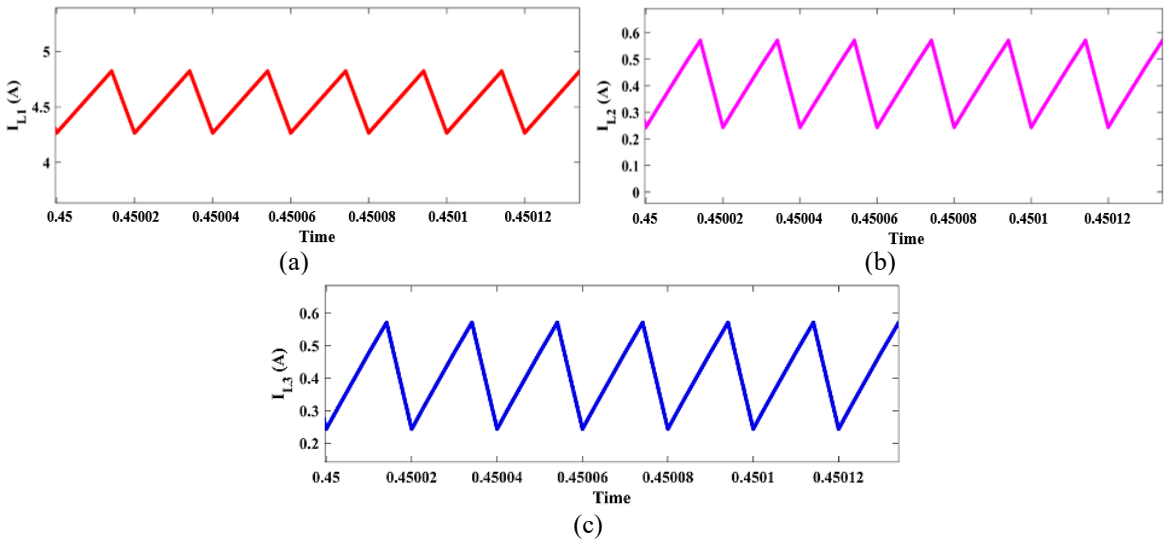


Figure 8. Current waveforms of the inductors (a) I_{L1}, (b) I_{L2}, and (c) I_{L3}

Figure 9 displays the voltage waveforms corresponding to capacitors C1 and C2. Figure 9(a) shows the voltage across the capacitor C1, and Figure 9(b) illustrates the voltage across the capacitor C2. It is worth noting that the capacitors experience a charging process when the MOSFET is in a deactivated condition. In contrast, the discharge of these capacitors occurs when the MOSFET transitions into its activated state. When C1 is originally at 0V or a voltage level lower than that during the charging process, its voltage rises. The charging rate is contingent upon the on-state resistance of the MOSFET, which encompasses the source resistance and the influence of diodes. The voltage across capacitor C1 gradually rises until it reaches its maximum charge level or until the MOSFET undergoes a state transition (refer to Figure 9(a)). Likewise, the charging process of C2 is affected by the presence of charge carriers, and the behavior of diodes further impacts its charging rate (refer to Figure 9(b)). The voltage across capacitors C1 and C2 diminishes until they are fully emptied or the MOSFET reverts to the OFF state. Additionally, it is important to acknowledge that various components, such as parasitic capacitances, MOSFET gate charges, diode forward voltages, and other similar elements, can also impact the waveform in real circuits. The behavior of capacitors in terms of charging and discharging can be considerably influenced by including diodes within an SC cell.

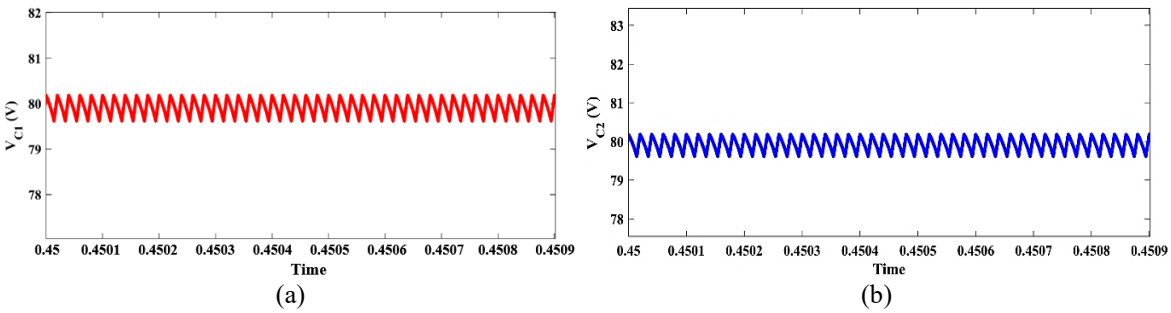


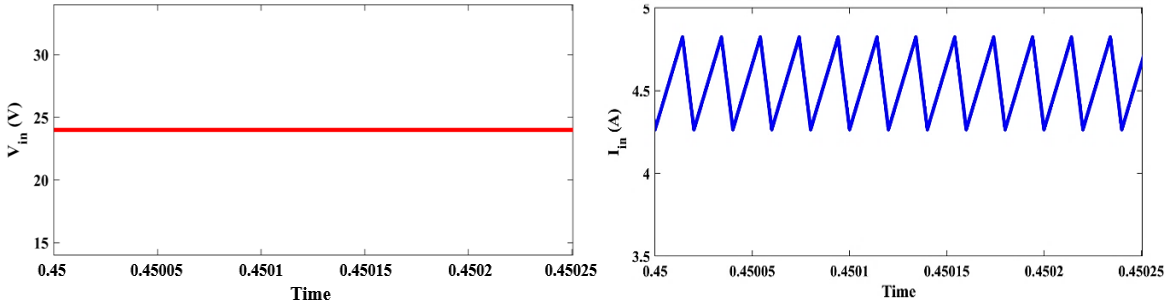
Figure 9. Voltage waveforms of the capacitors (a) V_{C1} and (b) V_{C2}

In the ON state, the MOSFET facilitates the discharge of a capacitor at a higher voltage into another capacitor at a lower voltage. Implementing a diode can effectively inhibit this undesirable current flow, preventing the inadvertent discharge of capacitors into other components within the circuit or adjacent capacitors. Diodes safeguard capacitors against voltage spikes or transient phenomena, particularly in MOSFET switching operations. Diodes serve the purpose of averting the occurrence of current spikes in unwanted directions by effectively impeding the reverse flow of current, hence safeguarding against abrupt voltage fluctuations. The rate of charging or discharging of a capacitor can be influenced by the forward resistance of the diode and the capacitance of the junction. Hence, the diodes employed in an SC cell are crucial in facilitating current flow in a single direction and effectively mitigating any potential adverse interactions between capacitors and other components during the switching stages. Nonetheless, using these

technologies also presents certain obstacles, such as voltage dips and significant thermal concerns, that necessitate careful consideration by designers. Given the converter's ability to function in both boost and buck modes, the input voltage can be more than, less than, or equal to the required output voltage.

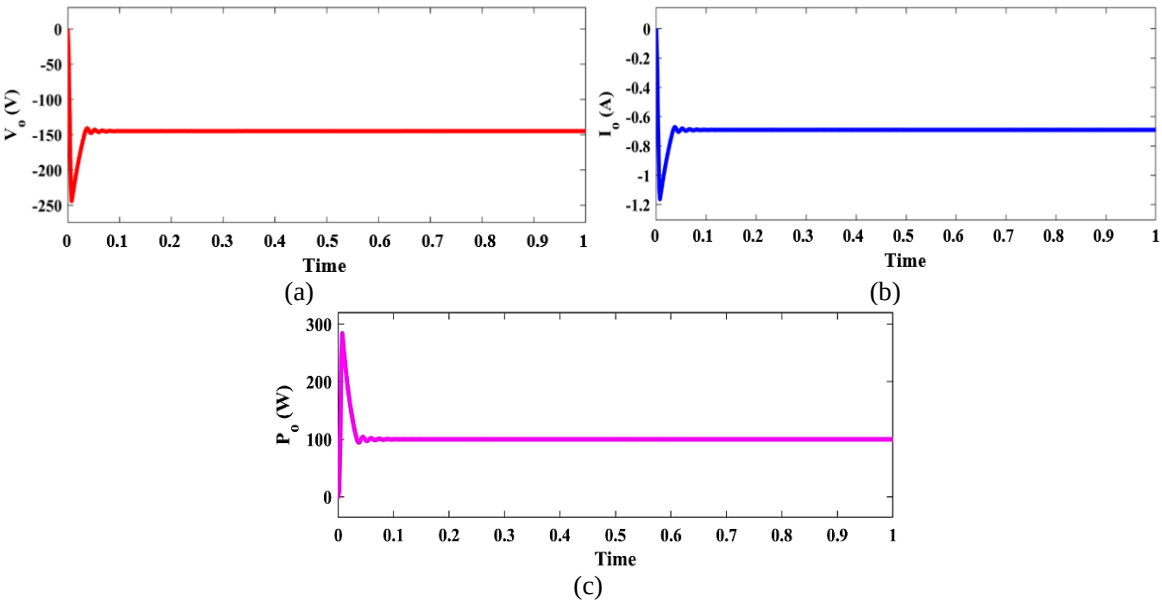
Figure 10 displays the input voltage and current waveforms, providing a comprehensive overview. Figure 10(a) shows the input voltage, and Figure 10(b) illustrates the input current waveform. The input current waveform of the proposed converter exhibits continuity (refer to Figure 10(b)), wherein it remains non-zero during the whole switching cycle, resembling the conventional Cuk converter. Including this characteristic in numerous applications is highly sought after because it can mitigate strain on source components and minimize electromagnetic interference by utilizing a constant input current. The inductor located on the input side serves the purpose of maintaining a continuous current waveform. Nonetheless, the fluctuation in the input current is also affected by the magnitude of the inductor and the operational frequency.

Figure 11 is a one-stop reference, capturing the output voltage, current, and power waveforms. Figure 11(a) shows the output voltage, Figure 11(b) illustrates the output current, and Figure 11(c) shows the output power. It is evidence of the converter's overall efficiency and dynamic operation. The proposed MCUK converter showcases a delicate balance of design, efficiency, and performance, which can be comprehended deeply by examining its components and their dynamic interactions.



(a) (b)

Figure 10. Source current and voltage waveforms (a) V_{in} and (b) I_{in}



(a) (b)

(c)

Figure 11. Output waveforms (a) V_o, (b) I_o, and (c) P_o

The efficiency of the proposed converter is determined by taking into account different losses, each of which contributes in a particular manner to the overall performance of the converter. The losses can be classified into three primary components: conduction, switching, and control losses. Conduction losses arise due to the inherent resistance shown by semiconductor devices while in a conducting condition, i.e., the

power losses occur due to energy dissipation due to the intrinsic resistance when an electric current passes through the device. This effect is commonly noticed in diodes and MOSFETs when they are active. Energy is dissipated during the transition of semiconductors between their active and inactive states. The control refers to the mitigating of losses that are linked to the circuits responsible for regulating the functioning of the semiconductor devices. The energy consumption encompasses the power utilized by gate drivers, control logic circuits, and additional auxiliary circuits responsible for ensuring the proper operation of the semiconductor devices. Although these losses may be relatively minor, they still substantially impact the converter's overall efficiency. It is imperative to underscore those losses intrinsic to the functioning of semiconductor devices. Hence, any optimization or enhancement in converter design must prioritize minimizing these losses to improve the overall efficiency. Table 3 provides a thorough analysis and mathematical depiction of the various losses, facilitating a more comprehensive comprehension. Each loss component is meticulously delineated in the table, accompanied by its corresponding equation. Table 3 is a helpful resource for individuals seeking to explore further the complexities associated with converter inefficiencies.

The efficacy of the proposed MCUK converter is being assessed in relation to the conventional Cuk converter and two altered Cuk converters described in existing literature, as seen in Figure 12. The performance calculation includes evaluating several types of losses, including control, switching, and conduction losses. The effectiveness is further assessed by computing load current fluctuations spanning from 10% to 125% of the designated capacity.

Based on the data depicted in Figure 12, it is evident that the efficiency of the proposed converter exceeds that of the Cuk converter and its various modified versions as the load is increased. The proposed topology demonstrates an efficacy of roughly 92.45% when operating at full load. In comparison, the Cuk converter obtains an efficiency of 86% under similar-rated circumstances. The efficiency of a system tends to improve when the input voltage increases due to a drop in input current. Consequently, this reduction in input current leads to decreased conduction losses of power switches. Upon analyzing the results presented and discussed previously, it is concluded that the suggested MCUK converter exhibits several favorable attributes compared to the traditional Cuk converter. These include a decrease in the voltage of the coupling capacitor, enhanced effectiveness, and a quicker transient response.

Table 3. Different power losses associated with the MCUK converter

Losses	Equation	Remarks
Control loss	$P_{gates} = Q_g V_{gs} f_s$	Q_g signifies the MOSFET's gate charge
Conduction loss	$P_S = i_d^2 R_{ds-ON} D$ $P_D = (V_f i_d + I_d^2 R_f)(1-D)$	R_f and R_{ds-ON} denote the diode's on-state and MOSFET resistance, and V_f signifies the forward voltage drop
Switching loss	$P_S = 5 f_s C_{oss} (0.5V_{in} + V_o)^2$ $P_D = 5 f_s C_d (0.5V_{in} + V_o)^2$	C_d and C_{oss} represent the parasitic capacitance of the diodes and MOSFET, respectively.
Passive devices	$R_{L1} = R_{1dc}\left(\frac{DT_s V_{in}}{L_1}\right)^2$ $R_{L2} = R_{2dc}\left(\frac{DT_s V_o}{L_2}\right)^2$ $R_{L3} = R_{3dc}\left(\frac{DT_s V_o}{L_3}\right)^2$	The direct current resistance determines the losses incurred in each inductor. The losses in the SC capacitors are disregarded due to their extremely small functional resistances.

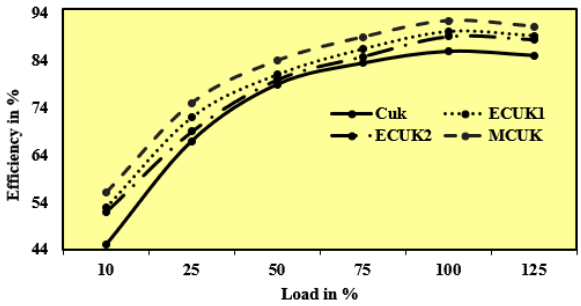


Figure 12. Efficiency curve comparison

5. CONCLUSION

The current study has made significant progress in creating an improved Cuk converter architecture that boasts a significant high voltage gain while reducing stress on the main switch. The ability to achieve this high voltage gain without using conventional methods like transformers, linked inductors, or high-duty

cycles is a noteworthy aspect of this development. It was discovered that the proposed converter primarily operates in the continuous conduction mode after looking more closely at the operational modalities. This mode ensures that energy flows continuously, preventing unpredictable energy pulses that can occasionally reduce power converter efficiency. Despite fluctuating input conditions, the output is consistent since it runs at a steady frequency. The investigation compared the suggested converter to the traditional Cuk converter and a few of its other versions to more clearly define the advantages of this new topology. This comparison highlighted several advantages of the recently introduced converter. The increased voltage gain, a critical parameter in power electronics, is foremost among the benefits. The innovative architecture also guarantees an astonishingly low voltage stress. This decrease in voltage stress is not only a theoretical accomplishment but has real-world implications. This chooses a semiconductor switch with a lower voltage capacity and a lower $R_{ds\text{-}ON}$ value possible. In turn, this improves the converter's dependability and efficiency. Other noteworthy characteristics include the continuous nature of the input and output current, which improves the stability of the energy flow. The usage of a single switch is another feature of the topology. This reduces costs and streamlines the entire design, making it more suitable for real-world use. The design exceeds many of its competitors in terms of efficiency, and its straightforwardness makes implementation simple. The research examined the steady-state analysis of voltage gain in great detail from an analytical perspective, illuminating the complexities inherent in the procedure. The MATLAB/Simulink results are in excellent alignment with the defined modes of operation and mathematical formulas developed during the experiment. This agreement between theory and simulated practice makes the suggested topology even more confident.

Although the research has laid a solid groundwork for creating a new Cuk converter architecture, there is still room for exploration and improvement. Future research could:

- Examine the converter's performance under various load settings, assessing its adaptability and resilience.
- Examine the design's scalability for larger industrial applications to ensure it applies in various situations.
- Look into possible design changes to increase the product's efficiency or lower the manufacturing costs.
- Include cutting-edge control techniques to increase the system's stability and response time.
- Create modular converter architectures that are easily scalable in response to the varying power needs of various applications.
- Looking into more sophisticated insulation and filtering methods in order to further minimize electromagnetic interference, particularly at larger switching frequencies.

The journey seemed encouraging, and with more research, this Cuk converter topology can completely alter the field of power electronics.

REFERENCES

[1] G. S. Reddy, M. Premkumar, S. Ravi, and L. Abualigah, "An intelligent converter and controller for electric vehicle drives utilizing grid and stand-alone solar photovoltaic power generation systems," *International Journal of Applied Power Engineering (IJAPE)*, vol. 12, no. 3, pp. 255–276, Jul. 2023, doi: 10.11591/ijape.v12.i3.pp255-276.

[2] S. Jaisiva, C. Kumar, K. Viji, M. Premkumar, M. Lakshmanan, and V. Jayakumar, "Enhancement of voltage conversion ratio using DC-DC boost converter with coat circuit," in *2022 3rd International Conference on Communication, Computing and Industry 4.0 (C2I4)*, Dec. 2022, pp. 1–5, doi: 10.1109/C2I456876.2022.10051308.

[3] M. Dhananjaya, D. Potnuru, M. Premkumar, and H. H. Alhelou, "Design and Implementation of Single-Input-Multi-Output DC-DC Converter Topology for Auxiliary Power Modules of Electric Vehicle," *IEEE Access*, vol. 10, pp. 76975–76989, 2022, doi: 10.1109/ACCESS.2022.3192738.

[4] Vinod, R. Kumar, and S. K. Singh, "Solar photovoltaic modeling and simulation: As a renewable energy solution," *Energy Reports*, vol. 4, pp. 701–712, Nov. 2018, doi: 10.1016/j.egyr.2018.09.008.

[5] M. Premkumar, P. Jangir, R. Sowmya, R. M. Elavarasan, and B. S. Kumar, "Enhanced chaotic JAYA algorithm for parameter estimation of photovoltaic cell/modules," *ISA Transactions*, vol. 116, pp. 139–166, Oct. 2021, doi: 10.1016/j.isatra.2021.01.045.

[6] Y. Lee, G. Vakil, R. Feldman, A. J. Watson, and P. W. Wheeler, "A high-power DC-DC converter based dual active bridge for MVDC grids on offshore wind farms," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10, doi: 10.1109/EPE.2016.7695573.

[7] H. M. Maheri, E. Babaei, M. Sabahi, and S. H. Hosseini, "High step-up DC–DC converter with minimum output voltage ripple," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3568–3575, May 2017, doi: 10.1109/TIE.2017.2652395.

[8] M. Premkumar, C. Kumar, A. Anbarasan, and R. Sowmya, "A novel non-isolated high step-up DC–DC boost converter using single switch for renewable energy systems," *Electrical Engineering*, vol. 102, no. 2, pp. 811–829, Jun. 2020, doi: 10.1007/s00202-019-00904-8.

[9] M. Premkumar, R. Sowmya, C. Kumar, P. Vijayarajan, and P. Jangir, "A new and effective high gain DC-DC converter topology with hybrid configuration for solar photovoltaic-based power generation systems," in *2023 IEEE 3rd International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Aug. 2023, pp. 1–6, doi: 10.1109/SeFeT57834.2023.10245545.

[10] M. Premkumar, U. Subramaniam, H. H. Alhelou, and P. Siano, "Design and development of non-isolated modified SEPIC DC-DC converter topology for high-step-up applications: Investigation and hardware implementation," *Energies*, vol. 13, no. 15, p. 3960, Aug. 2020, doi: 10.3390/en13153960.

[11] F. L. Tofoli, D. de C. Pereira, W. Josias de Paula, and D. de S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up DC–DC topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, Oct. 2015, doi: 10.1049/iet-pel.2014.0605.

[12] R. Hasan and S. Mekhilef, "Highly efficient flyback microinverter for grid-connected rooftop PV system," *Solar Energy*, vol. 146, pp. 511–522, Apr. 2017, doi: 10.1016/j.solener.2017.03.015.

[13] S. Zengin, F. Deveci, and M. Boztepe, "Decoupling capacitor selection in DCM flyback PV microinverters considering harmonic distortion," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 816–825, Feb. 2013, doi: 10.1109/TPEL.2012.2203150.
[14] R. Redl and L. Balogh, "Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage," in *Proceedings of 1995 IEEE Applied Power Electronics Conference and Exposition - APEC'95*, 1995, pp. 454–458, doi: 10.1109/APEC.1995.468987.
[15] M. Premkumar and T. R. Sumithira, "Design and implementation of new topology for nonisolated DC–DC microconverter with effective clamping circuit," *Journal of Circuits, Systems and Computers*, vol. 28, no. 05, p. 1950082, May 2019, doi: 10.1142/S0218126619500828.
[16] K. A. Mahafzah, A. Q. Al-Shetwi, M. A. Hannan, T. S. Babu, and N. Nwulu, "A new Cuk-based DC-DC converter with improved efficiency and lower rated voltage of coupling capacitor," *Sustainability*, vol. 15, no. 11, p. 8515, May 2023, doi: 10.3390/su15118515.
[17] Y. Almalaq and M. Matin, "Three topologies of a non-isolated high gain switched-inductor switched-capacitor step-up Cuk converter for renewable energy applications," *Electronics*, vol. 7, no. 6, p. 94, Jun. 2018, doi: 10.3390/electronics7060094.
[18] A. J. Sabzali, E. H. Ismail, and H. M. Behbehani, "High voltage step-up integrated double Boost–Sepic DC–DC converter for fuel-cell and photovoltaic applications," *Renewable Energy*, vol. 82, pp. 44–53, Oct. 2015, doi: 10.1016/j.renene.2014.08.034.
[19] J. Baek *et al.*, "11.7 A voltage-tolerant three-level buck-boost DC-DC converter with continuous transfer current and flying capacitor soft charger achieving 96.8% power efficiency and 0.87μs/V DVS rate," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 202–204, doi: 10.1109/ISSCC19947.2020.9063105.
[20] P. Upadhyay and R. Kumar, "A high gain cascaded boost converter with reduced voltage stress for PV application," *Solar Energy*, vol. 183, pp. 829–841, May 2019, doi: 10.1016/j.solener.2019.03.075.
[21] N. Salehi, H. Martínez-García, and G. Velasco-Quesada, "Modified cascaded Z-source high Step-Up boost converter," *Electronics*, vol. 9, no. 11, p. 1932, Nov. 2020, doi: 10.3390/electronics9111932.
[22] X. Wu, J. Wang, Y. Zhang, and Z. Liu, "Switched-capacitor-based high-gain DC–DC converter for fuel cell vehicle powertrain," *Journal of Power Electronics*, vol. 22, pp. 557–568, Apr. 2022, doi: 10.1007/s43236-022-00388-z.
[23] J. K. M. Kumar, H. A. Rauf, and R. Umamaheswari, "Switched capacitor-coupled inductor DC–DC converter for grid-connected PV system using LFCSO-based adaptive neuro-fuzzy inference system," *Journal of Circuits, Systems and Computers*, vol. 29, no. 12, p. 2050201, Sep. 2020, doi: 10.1142/S0218126620502011.
[24] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multicell switched-inductor and switched-capacitor Z-source inverters," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 837–848, Feb. 2013, doi: 10.1109/TPEL.2012.2204776.
[25] M. Shaabani, A. Mirzaei, M. Rezvanyvardom, F. Khosravi, and S. A. Gorji, "A hybrid switched-inductor/switched-capacitor DC-DC converter with high voltage gain using a single switch for photovoltaic application," *Energies*, vol. 16, no. 14, p. 5524, Jul. 2023, doi: 10.3390/en16145524.
[26] M. Premkumar, C. Ramakrishnan, C. Kumar, R. Sowmya, T. R. Sumithira, and P. Jangir, "An Improved Quasi-Z-Source Boost DC-DC Converter Using Single-Stage Switched-Inductor Boosting Technique," *Machines*, vol. 10, no. 8, p. 669, Aug. 2022, doi: 10.3390/machines10080669.
[27] B. R. Ananthapadmanabha, R. Maurya, and S. R. Arya, "Improved power quality switched inductor Cuk converter for battery charging applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9412–9423, Nov. 2018, doi: 10.1109/TPEL.2018.2797005.
[28] S.-W. Lee and H.-L. Do, "High step-up coupled-inductor cascade boost DC–DC converter with lossless passive snubber," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7753–7761, Oct. 2018, doi: 10.1109/TIE.2018.2803731.
[29] M. Premkumar, C. Kumar, and R. Sowmya, "Analysis and implementation of high-performance DC-DC step-up converter for multilevel boost structure," *Frontiers in Energy Research*, vol. 7, Dec. 2019, doi: 10.3389/fenrg.2019.00149.
[30] M. Premkumar, K. Karthick, and R. Sowmya, "A comparative study and analysis on conventional solar PV based DC-DC converters and MPPT techniques," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 11, no. 3, pp. 831–838, Sep. 2018, doi: 10.11591/ijeecs.v11.i3.pp831-838.
[31] X. Fan, H. Sun, Z. Yuan, Z. Li, R. Shi, and N. Ghadimi, "High voltage gain DC/DC converter using coupled inductor and VM techniques," *IEEE Access*, vol. 8, pp. 131975–131987, 2020, doi: 10.1109/ACCESS.2020.3002902.
[32] C. P. Leung and K. W. E. Cheng, "Design, analysis and implementation of the tapped-inductor boost current converter on current based system," *Energies*, vol. 14, no. 4, p. 888, Feb. 2021, doi: 10.3390/en14040888.
[33] S. Pourjafar, F. Sedaghati, H. Shayeghi, and M. Maalandish, "High step-up DC–DC converter with coupled inductor suitable for renewable applications," *IET Power Electronics*, vol. 12, no. 1, pp. 92–101, Jan. 2019, doi: 10.1049/iet-pel.2018.5414.
[34] Y. Zhao, W. Li, Y. Deng, X. He, S. Lambert, and V. Pickert, "High step-up boost converter with coupled inductor and switched capacitor," in *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, 2010, pp. 1–6, doi: 10.1049/cp.2010.0009.
[35] A. Mizani, S. A. Ansari, A. Shoulaie, J. N. Davidson, and M. P. Foster, "Single-active switch high-voltage gain DC–DC converter using a non-coupled inductor," *IET Power Electronics*, vol. 14, no. 3, pp. 492–502, Feb. 2021, doi: 10.1049/pel2.12007.
[36] H. Nouhi, V. Talavat, and M. Farhadi-Kangarlu, "A nonisolated single-switch coupled inductor-based DC-DC converter with high voltage gain for renewable power generation systems," *International Transactions on Electrical Energy Systems*, vol. 2023, pp. 1–15, May 2023, doi: 10.1155/2023/2600232.
[37] A. L. Eshkevari, A. Mosallanejad, and M. S. Sepasian, "Design, analysis, and implementation of a new high-gain P-type step-up dc/dc converter with continuous input current and common ground," *IET Power Electronics*, vol. 14, no. 1, pp. 225–238, Jan. 2021, doi: 10.1049/pel2.12027.
[38] J. Ahmad *et al.*, "A new high-gain DC-DC converter with continuous input current for DC microgrid applications," *Energies*, vol. 14, no. 9, p. 2629, May 2021, doi: 10.3390/en14092629.
[39] A. S. Mansour, A.-H. H. Amer, E. E. El-Kholy, and M. S. Zaky, "High gain DC/DC converter with continuous input current for renewable energy applications," *Scientific Reports*, vol. 12, no. 1, p. 12138, Jul. 2022, doi: 10.1038/s41598-022-16246-8.
[40] X. Liu, S. S. Yu, G. Zhang, W. Lin, T. Liu, and W. Le, "Design and experimental verification of a general single-switch N-stage Z-network high gain boost converter," *Mathematics*, vol. 10, no. 24, p. 4758, Dec. 2022, doi: 10.3390/math10244758.
[41] G. Zhang, B. Zhang, Z. Li, D. Qiu, L. Yang, and W. A. Halang, "A 3-Z-network boost converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 278–288, Jan. 2015, doi: 10.1109/TIE.2014.2326990.
[42] X. Wu, J. Wang, Y. Zhang, J. Du, Z. Liu, and Y. Chen, "Review of DC-DC converter topologies based on impedance network with wide input voltage range and high gain for fuel cell vehicles," *Automotive Innovation*, vol. 4, no. 4, pp. 351–372, Nov. 2021, doi: 10.1007/s42154-021-00163-z.
[43] S. Gopinathan, V. Seshagiri Rao, K. Sundaramoorthy, and B. Mathew Jos, "Family of high-gain quadratic symmetrical active impedance network-based DC-DC converters with fault ride-through feature," *Electric Power Components and Systems*, pp. 1–17, Jul. 2023, doi: 10.1080/15325008.2023.2238711.

[44] T.-D. Duong, M.-K. Nguyen, T.-T. Tran, Y.-C. Lim, and J.-H. Choi, "Transformerless high step-up DC-DC converters with switched-capacitor network," *Electronics*, vol. 8, no. 12, p. 1420, Nov. 2019, doi: 10.3390/electronics8121420.
[45] F. M. Shahir, M. Gheisarnejad, and M.-H. Khooban, "A new transformer-less structure for a boost DC-DC converter with suitable voltage stress," *Automation*, vol. 2, no. 4, pp. 220–237, Oct. 2021, doi: 10.3390/automation2040014.
[46] J. D. Navamani, K. Vijayakumar, and R. Jegatheesan, "Non-isolated high gain DC-DC converter by quadratic boost converter and voltage multiplier cell," *Ain Shams Engineering Journal*, vol. 9, no. 4, pp. 1397–1406, Dec. 2018, doi: 10.1016/j.asej.2016.09.007.
[47] A. Alkhaldi, A. Elkhateb, and D. Laverty, "Voltage lifting techniques for non-isolated DC/DC converters," *Electronics*, vol. 12, no. 3, p. 718, Feb. 2023, doi: 10.3390/electronics12030718.
[48] T. Sutikno, H. S. Purnama, N. S. Widodo, S. Padmanaban, and M. R. Sahid, "A review on non-isolated low-power DC–DC converter topologies with high output gain for solar photovoltaic system applications," *Clean Energy*, vol. 6, no. 4, pp. 557–572, Aug. 2022, doi: 10.1093/ce/zkac037.
[49] J. Zhao, D. Chen, and J. Jiang, "A novel transformerless high step-Up DC-DC converter with active switched-inductor and quasi-Z-source network," *IET Power Electronics*, vol. 14, no. 9, pp. 1592–1605, Jul. 2021, doi: 10.1049/pel2.12128.
[50] P. Luo *et al.*, "A high step-up DC-DC converter based on three-winding coupled inductor and voltage multiplier for renewable energy applications," *IET Power Electronics*, vol. 16, no. 6, pp. 961–974, May 2023, doi: 10.1049/pel2.12443.
[51] A. Farakhor, M. Abapour, M. Sabahi, S. G. Farkoush, S.-R. Oh, and S.-B. Rhee, "A study on an improved three-winding coupled inductor-based DC/DC boost converter with continuous input current," *Energies*, vol. 13, no. 7, p. 1780, Apr. 2020, doi: 10.3390/en13071780.
[52] S.-J. Chen, S.-P. Yang, C.-M. Huang, and P.-S. Huang, "Analysis and design of a new high voltage gain interleaved DC–DC converter with three-winding coupled inductors for renewable energy systems," *Energies*, vol. 16, no. 9, p. 3958, May 2023, doi: 10.3390/en16093958.
[53] F. Wang, "A novel quadratic Boost converter with low current and voltage stress on power switch for fuel-cell system applications," *Renewable Energy*, vol. 115, pp. 836–845, Jan. 2018, doi: 10.1016/j.renene.2017.08.032.
[54] S.-W. Lee and H.-L. Do, "Single-switch high step-up DC-DC converter with a resonant voltage doubler and low duty ratio," *International Review of Electrical Engineering (IREE)*, vol. 15, no. 1, Feb. 2020, doi: 10.15866/iree.v14i6.16945.
[55] R. Ling, G. Zhao, and Q. Huang, "High step-up interleaved boost converter with low switch voltage stress," *Electric Power Systems Research*, vol. 128, pp. 11–18, Nov. 2015, doi: 10.1016/j.epsr.2015.06.016.
[56] M. Zhu and F. L. Luo, "Enhanced self-lift Cûk converter for negative-to-positive voltage conversion," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2227–2233, Sep. 2010, doi: 10.1109/TPEL.2010.2047269.
[57] H. Gholizadeh, S. A. Gorji, E. Afjei, and D. Sera, "Design and implementation of a new Cuk-based step-up DC–DC converter," *Energies*, vol. 14, no. 21, p. 6975, Oct. 2021, doi: 10.3390/en14216975.
[58] D. Zhou, A. Pietkiewicz, and S. Cuk, "A three-switch high-voltage converter," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 177–183, Jan. 1999, doi: 10.1109/63.737606.
[59] F. Khan, M. Zaid, A. Tariq, and M. M. A. Khan, "A new non-isolated high-gain DC-DC converter for the PV application," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 5, p. 100198, Sep. 2023, doi: 10.1016/j.prime.2023.100198.
[60] S. Chakraborty and A. Kumar, "A multilevel based high gain switched inductor quadratic DC-DC boost converter," *IFAC-PapersOnLine*, vol. 55, no. 1, pp. 448–453, 2022, doi: 10.1016/j.ifacol.2022.04.074.
[61] Y. P. Siwakoti, F. Blaabjerg, P. C. Loh, and G. E. Town, "High-voltage boost quasi-Z-source isolated DC/DC converter," *IET Power Electronics*, vol. 7, no. 9, pp. 2387–2395, Sep. 2014, doi: 10.1049/iet-pel.2013.0845.

BIOGRAPHIES OF AUTHORS

A. Clement Raj received his B.E. (Electrical and Electronics Engineering) from Anna University and M.E. (Power Electronics and Drives) from Anna University. He is currently pursuing his Ph.D. in Annamalai University as a part-time (external) in the domain of DC-to-DC converters for PV applications. He has teaching experience of more than 14 years, out of which, he is having 7.5 years in Bule Hora University, Ethiopia. He has guided more than 20 UG projects and published several research papers in reputed journals. He is having lifetime membership in ISTE. His research interest includes power converters, HVDC, renewable energy, and power system analysis. He can be contacted at email: clementlecturer@gmail.com.

Ramaiyan Bensraj was born in 1973 in Marthandam. He obtained a B.E. (Electrical Electronics and Power) and M.E. (Power Systems) from Dr. Babasaheb Ambedkar Marathwada University, Maharashtra and Annamalai University, respectively, and then a Ph.D. in Power Electronics from Annamalai University, Chidambaram, in 2011. He is currently working as an associate professor in the Department of Electrical and Electronics Engineering, at Annamalai University, where he has put in nineteen years of service. He has produced four Ph.D.'s, guided three Ph.D. scholars, and guided twelve M.E. students so far. He has eighty publications in national, and international journals and conferences. His fields of interest include multilevel inverters, power quality and power electronics in power systems, and image processing. He can be contacted at email: bensraj_au@rediffmail.com.