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Analysis and simulation of 7-level and 9-level cascaded H-bridge multi-level inverters

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ABSTRACT

Multi-level inverters (MLIs) have created a new revolution in high-power and medium-voltage applications in industry and research. In recent years, cascaded multi-level inverters have gained significant interest due to their ability to generate high-quality output waveforms with reduced total harmonic distortion (THD). This paper discusses the analysis and simulation of 7-level and 9-level cascaded H-bridge multi-level inverters using mathematical models and simulation tools. The proposed research puts emphasis on evaluating the performance and control strategies of these inverters. The control strategies, including pulse width modulation (PWM) techniques, are discussed in depth, with a focus on their effect on output waveform quality and reduction of THD. The simulation results are compared to showcase the advantages offered by the cascaded multi-level inverters in terms of waveform quality. The findings demonstrate the superior performance and power quality advantages offered by these multi-level inverters compared to traditional two-level inverters. Additionally, a passive LC filter is designed and implemented along with a multi-level inverter configuration that helps to keep the THD within the limits specified by IEEE standards.

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1. INTRODUCTION

The increasing adoption of cascaded H-bridge multi-level inverters in recent decades is largely driven by their capacity to generate high-quality voltage waveforms with lower harmonic content. These advanced power electronics are used in electric vehicles, industrial drives, and renewable energy systems [1]. The rising demand for efficient and reliable power conversion systems has led to a growing interest in the advancement of sophisticated inverter topologies. The fundamental principle behind the cascaded H-bridge multilevel inverter (CHBMLI) lies in its capability to produce a stepped waveform by integrating the outputs of numerous series-connected H-bridge switches. The voltage levels in each H-bridge switch are typically established using a mix of DC sources, including batteries or capacitors, combined with the switching function of semiconductor devices like IGBTs and MOSFETs [2]. Modularity and scalability of the CHBMLI make it suitable for various applications where high-quality power conversion is required. The multi-level nature of these inverters allows for the production of near-sinusoidal voltage waveforms with fewer harmonics than traditional inverters. This paper contains simulation and analysis of 7-level and 9-level configurations of cascaded H-bridge inverters. In cases of switch failure or faults, the system's remaining

switches can continue to operate, thereby minimizing downtime and improving overall system reliability. As research and development in this field advance, these inverters are projected to be crucial in the future of sustainable energy systems and electrification [3]-[5]. Figure 1 shows the schematic diagram of the proposed model. The inverter's output voltage waveforms exhibit significant total harmonic distortion (THD). To mitigate voltage harmonics in the waveform, it is crucial to use an LC filter for suppression.

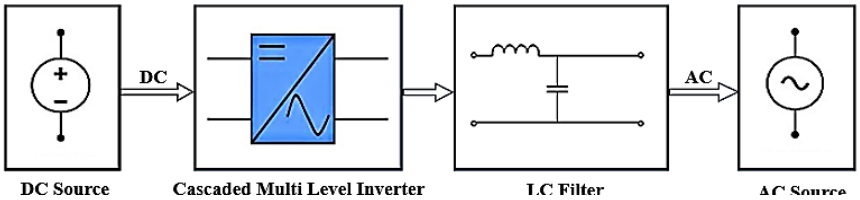

Figure 1. Block diagram of the proposed model

2. COMPREHENSIVE THEORETICAL BASIS

2.1. Conventional inverters

The role of a power inverter is critical in converting direct current (DC) to alternating current (AC), allowing it to power a variety of devices and appliances. Static inverters that use only electronic circuitry are available, depending on application needs and technology. This breakthrough has made inverters more reliable and efficient, making them essential to many power systems and electrical equipment [6].

2.1.1. Two-level inverters

A two-level inverter generates two voltage levels for a load, producing $+V_{DC}$ and $-V_{DC}$ output voltages. The pulse width modulation (PWM) technique is used to switch between these voltage levels, generating AC voltage. However, this method has drawbacks, such as harmonic distortions and high voltage change rate (dv/dt) compared to multi-level inverters [7]. Despite the limitations, the two-level inverter is widely used in applications where output voltage distortion and dv/dt are not critical factors [8].

2.2. Multi-level inverters

High-performance, medium-voltage industrial applications favor multi-level inverters. They convert DC electricity from batteries, supercapacitors, or solar panels into AC power at different voltages. Multi-level inverters convert and use medium-voltage power efficiently by producing high-output power [9], [10]. There are three types of multi-level inverters as given: diode clamped multi-level inverter, flying capacitors multi-level inverter, and cascaded type multi-level inverter.

2.3. Cascaded H-bridge multi-level inverter

Initially, the CHBMLI topology was introduced for motor drive applications. Due to electronic switch power ratings, conventional converters lost power and were inefficient in high-voltage situations. CHBMLI offers lower costs and reduced electromagnetic interference compared to conventional converters [11]. Higher performance with low THD and increased efficiency are obtained. The requirement of separate, equal-value DC sources for each H-bridge in the symmetrical CHBMLI framework reduces the complexity of integrating various renewable energy sources [12]. The relationship between the number of H-bridges (n) and the leveled output per phase (m) is given by the equation $m = 2n + 1$. System requirements, applications, switch limits, and system losses should be considered while choosing the optimum number of levels [13].

2.4. Pulse width modulation (PWM) techniques

PWM transmits information through pulses, with data encoded in the pulse widths. To produce the desired result, PWM techniques are essential. There have been several modulation techniques proposed and discussed in the literature to accomplish this, including space vector PWM (SVPWM), selective harmonic elimination PWM (SHE-PWM), and multi-carrier PWM (MCPWM) [14].

2.4.1. Multi-carrier PWM scheme

Among the various modulation techniques, MCPWM is commonly used for controlling MLIs due to its simplicity. Techniques such as SPWM and SVPWM generate pulses that control the switches in MLIs, with the goal of producing a near-sinusoidal output voltage while minimizing harmonic distortion [15]. MCPWM, the most commonly used, simplifies pulse generation by comparing reference signals with triangular signals to control individual power switches. MCPWM requires (n-1) carrier waves for an n-level inverter [16]. It can be categorized into two types: level-shifted pulse width modulation (LSPWM) and

phase-shifted pulse width modulation (PSPWM). LSPWM encompasses various variants, including phase disposition-pulse width modulation (PD-PWM), phase opposition disposition-pulse width modulation (POD-PWM), alternate phase opposition disposition-pulse width modulation (APOD-PWM), and carrier-overlapping pulse width modulation (CO-PWM) [17]-[20].

2.4.2. Sinusoidal PWM

In SPWM, the comparison is performed between a sinusoidal modulating waveform and a triangular carrier waveform to determine the ON/OFF states of the switches. If the modulating wave is greater than the carrier wave, the switch is ON and the state is high. Lower amplitudes indicate low states and turn OFF the switch [21]. The THD in the output voltage can be reduced by controlling the inverter's switching pattern with SPWM. It can easily eliminate lower harmonics. In the case of the multi-carrier SPWM technique, (m-1) carrier waves are needed for an m-level CHBMLI. Maintaining uniform amplitude and frequency for all carrier waves or triangular waves is crucial.

2.4.3. Level shift PWM

This approach uses triangular waveforms for all carrier signals over the converter's voltage range. These signals have the same frequency and amplitude [22]. They are categorized based on the organization of carrier signals. Producing n levels requires (n-1) carrier signals. It is employed for inverter control without incorporating power balancing.

3. METHOD

3.1. Simulation of cascaded H-bridge 7-level MLI

The circuit topology of the 7-level CHBMLI and the associated output voltage waveform are presented in Figures 2 and 3. It consists of three H-bridges, with each individual bridge consisting of four switches powered by a DC source. Each H-bridge is capable of generating a positive, negative, and zero voltage. In this topology, all three bridges are interconnected in series with each other [23], [24]. The voltage produced by each bridge is added together to get the required voltage. The voltage levels produced in this MLI are +3 V_{DC}, +2 V_{DC}, +V_{DC}, 0, -V_{DC}, -2 V_{DC}, and -3 V_{DC}. The characteristics of 7-level CHBMLI make it suitable for high applications that require low harmonic, distortion, and better voltage control [25].

Switching operations that are used to generate the different voltages are given in Figure 4. In MLIs, corresponding voltages are generated when switches are toggled ON and OFF according to a set pattern, where 1 indicates the switch is ON and 0 indicates it is OFF [26]. Figures 5(a)-5(h) represent various working modes of the 7-level multi-level inverter through which various levels of voltages are produced. Figure 6 illustrates the output voltage waveform of a 7-level CHBMLI.

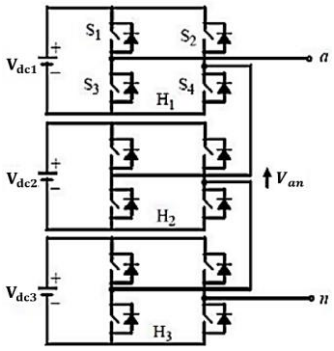

Figure 2. 7-level CHBMLI circuit topology

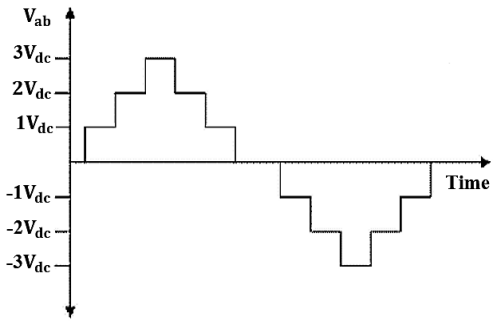

Figure 3. 7-level CHBMLI output voltage waveform

V_{DC}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
+3	1	1	0	0	1	1	0	0	1	1	0	0
+2	1	1	0	0	1	1	0	0	0	1	0	1
+1	1	1	0	0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0	1	0	1
	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	1	0	1	0	1	0	1	0
-2	0	0	1	1	0	0	1	1	1	0	1	0
-3	0	0	1	1	0	0	1	1	0	0	1	1

Figure 4. Switching frequency of 7-level CHBMLI

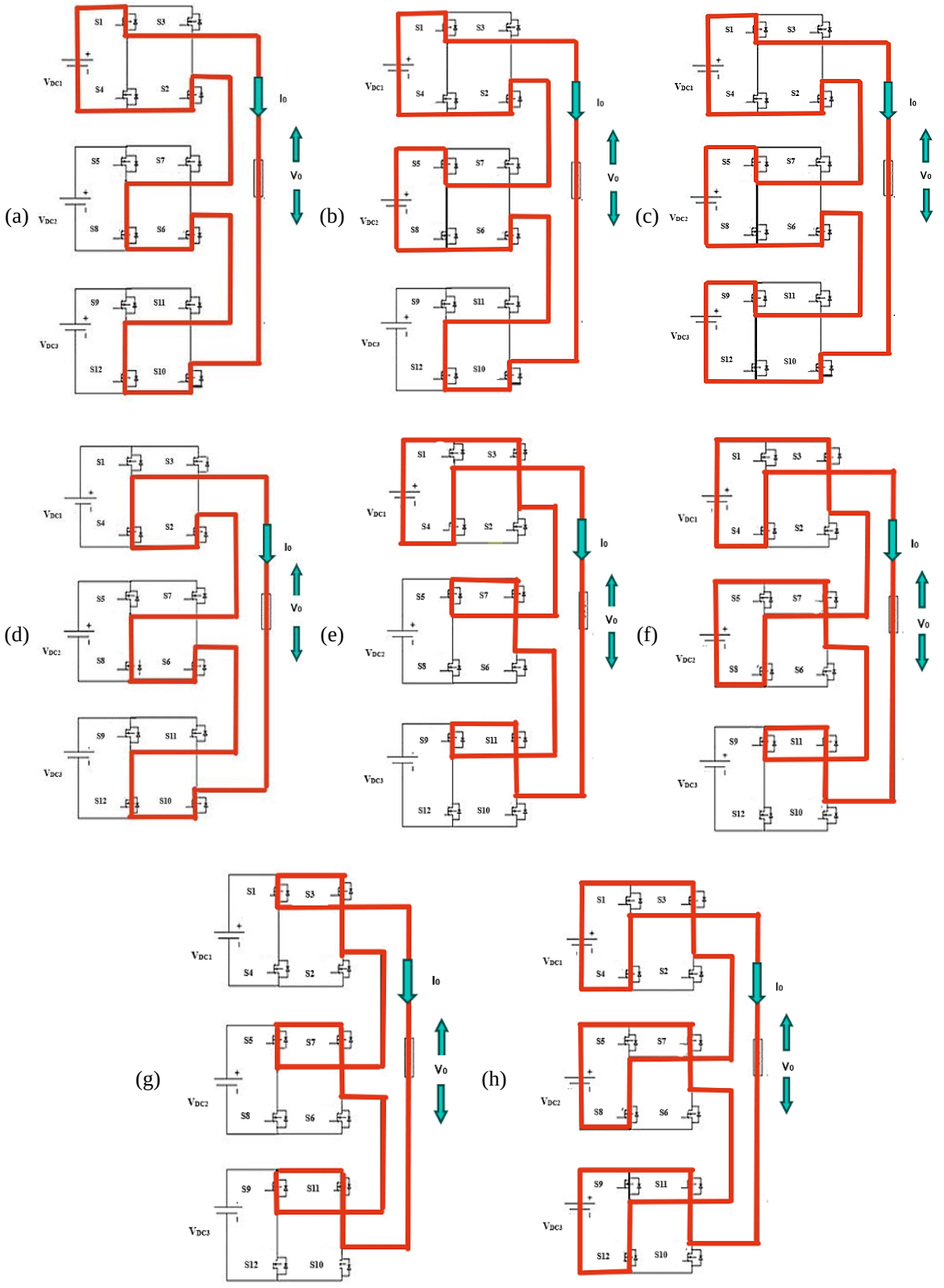

Figure 5. Working modes of the 7-level multi-level inverter: (a) V_{dc}, (b) 2 V_{dc}, (c) 3 V_{dc}, (d) 0 V_{dc}, (e) -V_{dc}, (f) -2 V_{dc}, (g) -3 V_{dc}, and (h) 0 V_{dc}

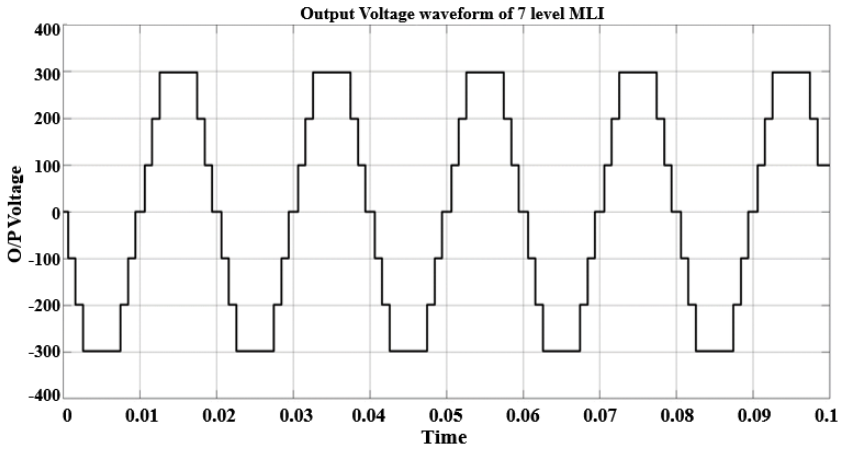

Figure 6. 7-level CHBMLI output voltage waveform

3.2. Simulation of cascaded H-bridge 9-level MLI

The 9-level CHBMLI is a specific configuration that offers advantages in power conversion applications. It consists of four H-bridges, each composed of four switches, generating multiple voltage levels, including positive, negative, and zero voltages. By combining these voltage levels, it achieves higher resolution and flexibility in generating the output voltage waveform [27]. This configuration enhances the quality of the output waveform by decreasing harmonic content, hence minimizing noise and distortion. It also provides reduced switching losses and improved efficiency. The 9-level CHBMLI's high voltage resolution is advantageous for applications that demand precise voltage control, enabling more exact adjustments in output voltage and enhancing control and accuracy in different industrial processes [28].

The general structure of the 9-level CHBMLI and its corresponding waveform are shown in Figures 7 and 8. It produces an output waveform of four positive levels, four negative levels, and a zero level. There are 9 switching modes and it generates the required levels of output of voltages which are +4 V_{DC}, +3 V_{DC}, +2 V_{DC}, +V_{DC}, 0, -V_{DC}, -2 V_{DC}, -3 V_{DC}, and -4 V_{DC}. Figure 9 indicates the corresponding voltages according to the switching pattern. Figures 10(a)-10(i) represent various working modes of the 9-level CHBMLI through which various levels of voltages are produced [29]. Figure 11 represents the output voltage waveform of a 9-level CHBMLI.

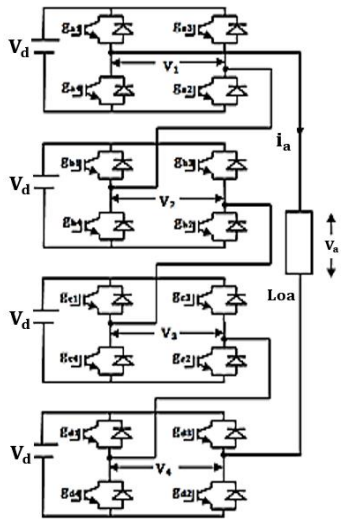

Figure 7. 9-level CHBMLI circuit topology

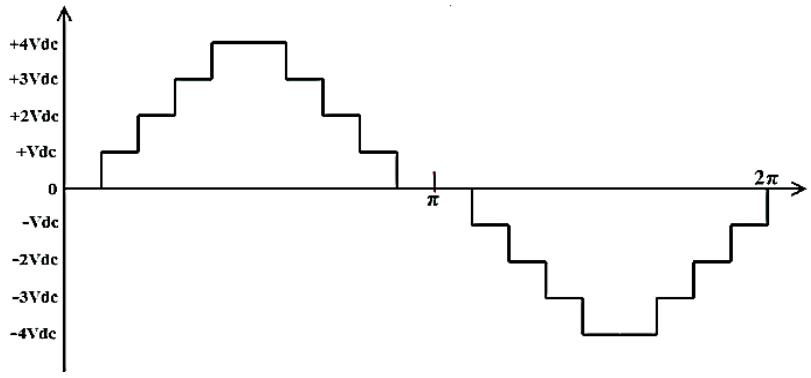

Figure 8. 9-level CHBMLI output voltage waveform

V_{DC}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
4	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
3	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1
2	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1
1	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
-1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
-2	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1
-3	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1
-4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Figure 9. Switching frequency of 9-level CHBMLI

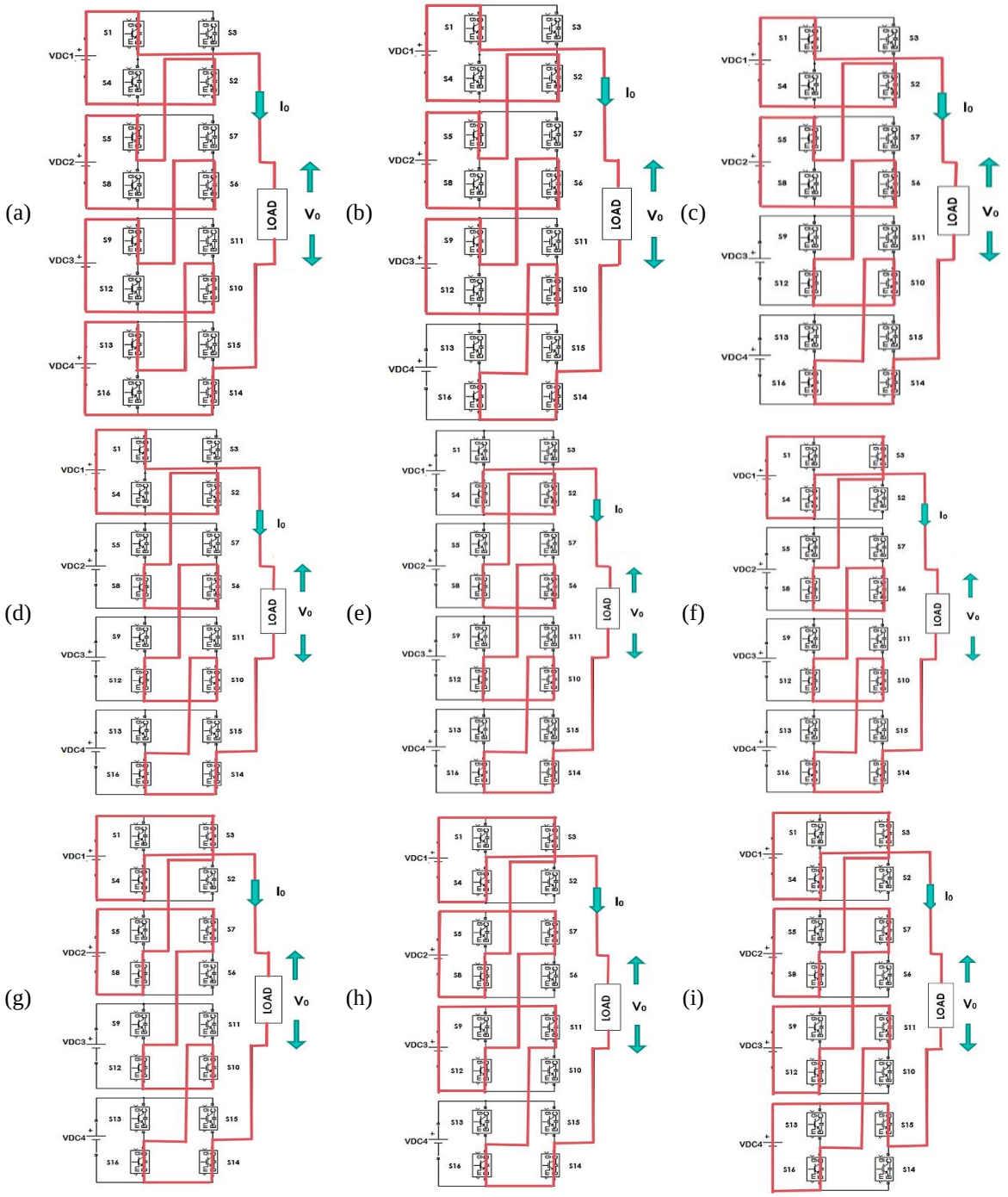

Figure 10. Working modes of the 9-level CHBMLI: (a) 4 V_{dc}, (b) 3 V_{dc}, (c) 2 V_{dc}, (d) V_{dc}, (e) 0 V_{dc}, (f) -V_{dc}, (g) -2 V_{dc}, (h) -3 V_{dc}, and (i) -4 V_{dc}

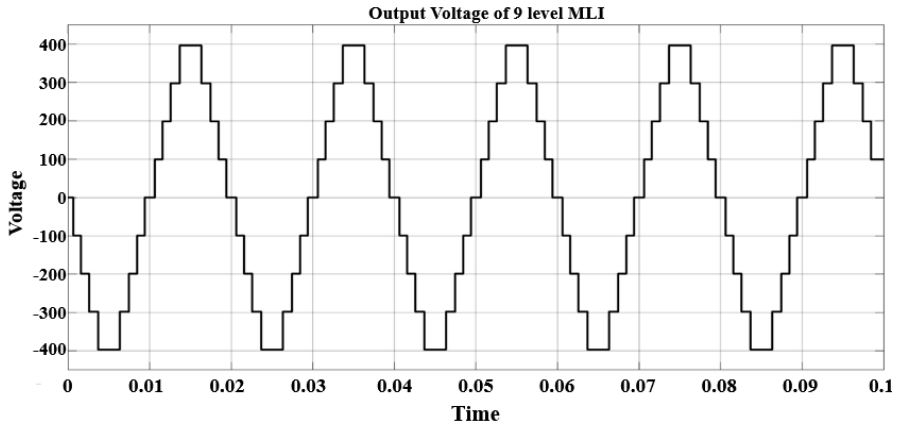

Figure 11. 9-level CHBMLI output voltage waveform

3.3. THD analysis

The quality of a waveform is measured by total harmonic distortion (THD), which is defined by the harmonic number (n). Harmonics in the system can cause equipment degradation and it is crucial to minimize them. In the context of the MLI, controlled switching pulses in the output voltage (V_{out}) are used to reduce the THD. Lowering THD helps eliminate the presence of harmonics and improves the quality of power delivered [30]. Harmonic distortions primarily stem from the usage of non-linear loads, particularly those incorporating power electronics, as these loads do not draw current in a sinusoidal manner. IEEE Standards typically define limit values for voltage harmonics, with a THD limit of 5% and a limit of 3% for each individual harmonic. DC voltages and inverter commutation angles affect output voltage THD. In an ideal scenario with cascaded symmetrical inverters, all DC sources remain constant and equal, as in (1). The THD analysis of the 7-level and 9-level CHBMLI model is shown in Figures 12 and 13, respectively.

$$the\ THD_V = \frac{\sqrt{\sum_{n=2}^{\infty}\left(V_{n,RMS}\right)^2}}{V_{1,RMS}} = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{RMS})^2-\left(V_{1,RMS}\right)^2}}{V_{1,RMS}} \quad (1)$$

3.4. Design and implementation of a passive filter

Due to the switching nature of MLIs, it introduces undesired harmonics and distorts the AC output waveform. Filters are utilized to mitigate the harmonics and enhance fundamental components of the output voltage. Filters allow for a smoother and more sinusoidal waveform, thus reducing harmonic distortion. There are three main types of filters commonly used, they are inductor filter (L), inductor-capacitor filter (LC), and inductor-capacitor-inductor filter (LCL). The LC filter, also known as a passive LC filter or second-order filter, is an electronic circuit that utilizes inductors (L) and capacitors (C) to shape or filter the frequency response of a signal. It is designed to meet IEEE standards by achieving less than a 5% deviation. The LC filter incorporates both an inductor and a capacitor, making it a second-order filter. In the LC filter, a capacitor is connected to the grid in parallel. Applied with a switching method, the LC filter is capable of removing lower-order odd harmonics from the output. For single-phase full bridge inverters, $V_{out}(rms) = V_{DC}$, $V = 100\sqrt{2}$ sin wt, ΔI_L = 20% of the rated current, and $\Delta I_{L\,max} = \frac{V_{dc}}{4\times L\times F_{sw}}$.

$$L = \frac{V_{dc}}{4\times \Delta I_{L\,max}\times F_{sw}} \quad (2)$$

$$C = \left(\frac{10}{2\times \Pi\times F_{sw}}\right)^2 \times \frac{1}{L} \quad (3)$$

Where L is inductance in mH, F_{sw} is switching frequency in Hz, and C is the capacitance in mF. Figures 14 and 15 represent the output voltage waveforms of a 7-level and 9-level CHBMLI with a passive LC filter. Figures 16 and 17 represent the THD analysis of a 7-level, 9-level CHBMLI with a filter. The observations from the above models are tabulated in Table 1.

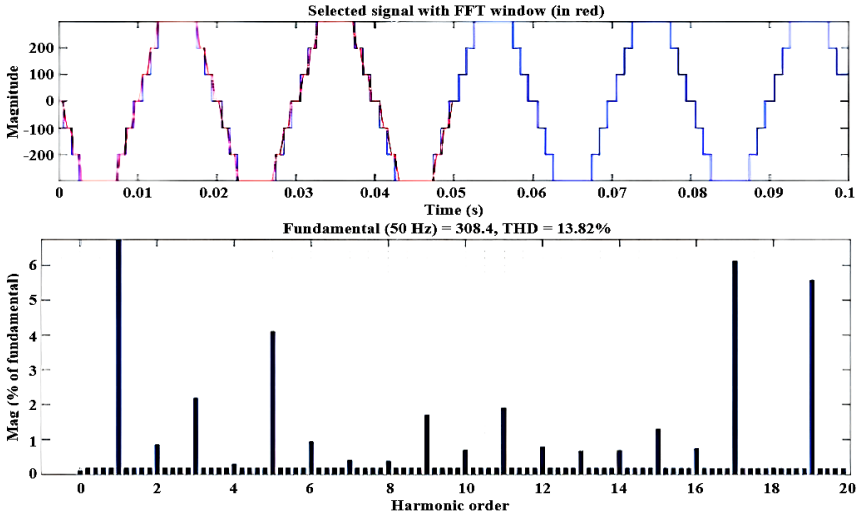

Figure 12. THD analysis of 7-level CHBMLI

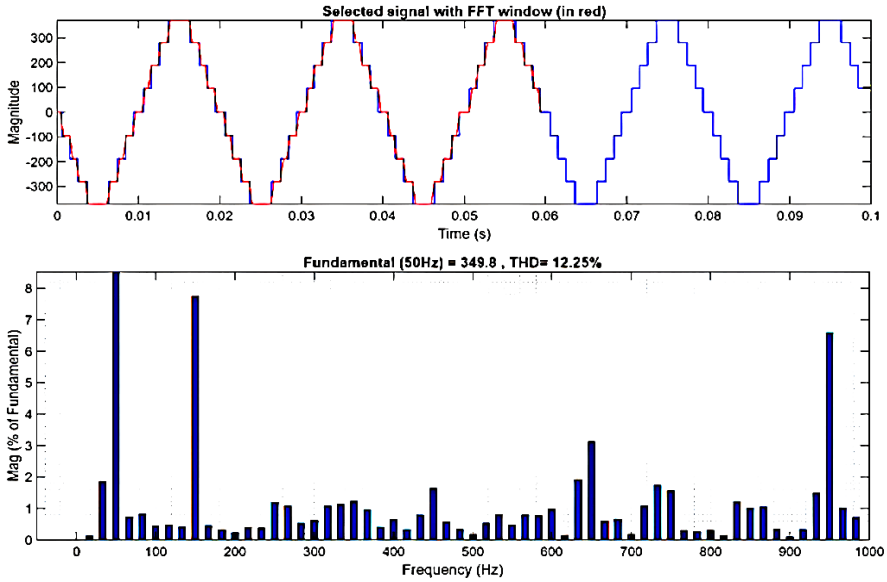

Figure 13. THD analysis of 9-level CHBMLI

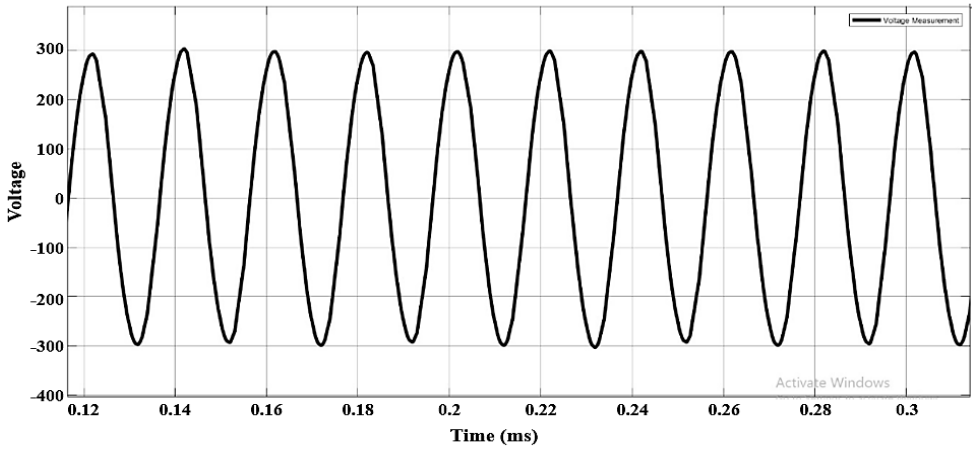

Figure 14. Output voltage waveform of 7-level CHBMLI with an LC filter

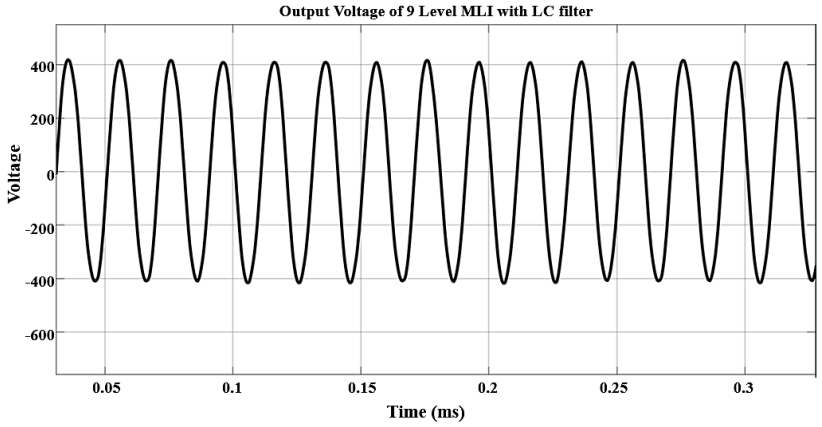

Figure 15. Output voltage waveform of 9-level CHBMLI with an LC filter

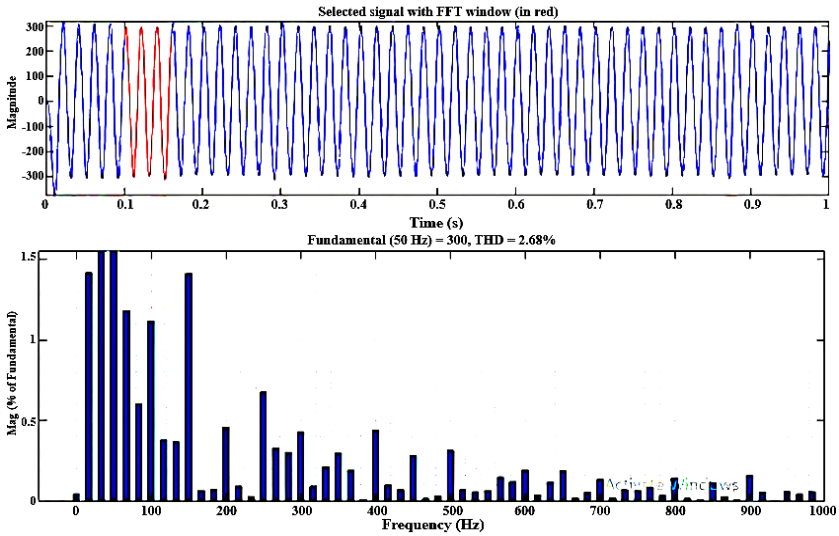

Figure 16. THD analysis of 7-level CHBMLI with passive LC filter

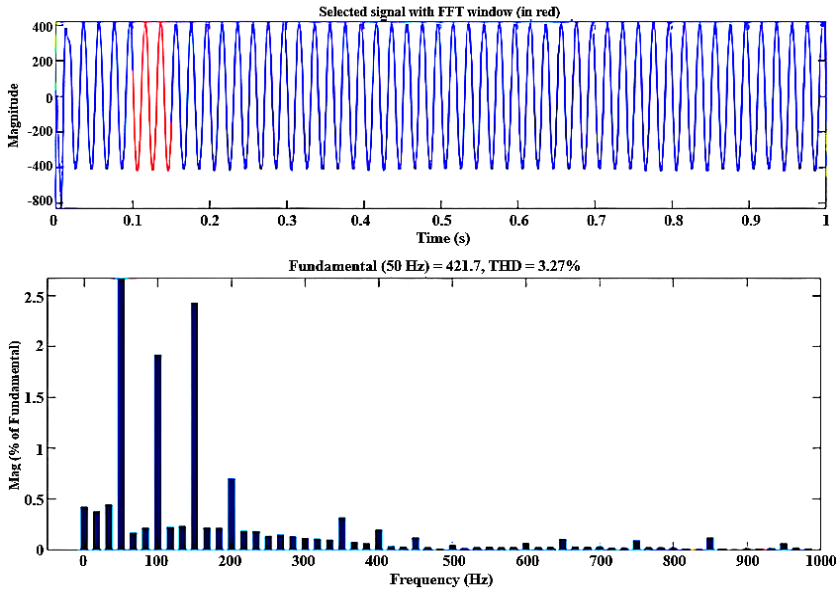

Figure 17. THD analysis of 9-level CHBMLI with passive LC filter

Table 1. THD comparison of 7-level and 9-level MLI

Level of MLI	Parameters	THD value	Fundamental component of output voltage (V)
7-level MLI	Fixed DC without LC filter	13.82%	308.4
	Fixed DC with LC filter	2.68%	300
9-level MLI	Fixed DC without LC filter	12.25%	349.8
	Fixed DC with LC filter	3.27%	421.7

4. CONCLUSION

The CHBMLI is capable of producing superior quality output waveforms compared to traditional two-level inverters, which has contributed to its rising popularity in applications requiring medium to high power. When it comes to MLI, PWM techniques are necessary to achieve the desired output. It was decided to use the level shift pulse width modulation (PWM) technique for this project, with a sine wave serving as the modulating signal. The total harmonic distortion (THD) was measured to be 13.82% for the 7-level inverter and 12.25% for the 9-level inverter, respectively. It is evident that increasing the number of levels in the MLI lowers the THD percentage and enhances the fundamental voltage, which signifies improved inverter performance. The efficiency of passive filters in lowering THD is another key takeaway from this effort. Through the execution of the required computations, an LC filter was designed. The THD values for 7-level and 9-level CHBMLIs are reported to be 2.68% and 3.27%, respectively, once the passive filter that was constructed is incorporated with the proper DC input voltage. Precise adjustment of filters is necessary to generate pure sinusoidal waveforms of voltage and current, which will decrease THD and enhance efficiency.

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