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Minimization of the circuit components with modified cascaded multilevel inverter topology

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ABSTRACT

This article examines a modified multilevel inverter circuit that uses basic units connected in cascade. The suggested circuit can be used with an inverter that is symmetrical or asymmetric. The magnitude of the DC voltage source is determined using a variety of methods in order to generate a large number of voltage levels. For both symmetrical and asymmetrical configurations, the magnitude of two DC sources in basic units can be used. The DC voltage source's magnitude is the same for each unit in the symmetrical configuration. However, in an asymmetrical configuration, the value of the DC source for the fundamental units is inequitable, and their magnitudes are obtained using various techniques. Comparison study demonstrates that the suggested circuit requires minimum components, reduces power loss, and boosts inverter efficiency. Additionally, in comparison to modern topologies, the standing voltage across the switches is acceptable. To verify the effectiveness of the investigated topology, simulation results for 15, 17, 23, and 31-level inverters are analysed.

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1. INTRODUCTION

Multilevel inverters (MLI) have drawn significant attention over the past two decades for the following benefits: i) lower dv/dt stress; ii) less total harmonic distortion (THD) with decreased electromagnetic interference (EMI) issues [1]-[5]. This makes it appropriate for high voltage applications like dynamic voltage restorers (DVR), AC drives, flexible AC transmission systems (FACTS), and renewable energy sources [3]-[5]. There are generally three common topologies: Baker proposed the cascaded H-bridge (CHB) inverter in 1975 [6]. Neutral point clamp (NPC) inverters were created by Nabae *et al.* [7], Yuan and Barbi [8]. Flying capacitors are an alternative to NPCs [9], [10]. The number of components in NPC and flying capacitor (FC) rises as the number of voltage levels does as well. Both also experience issues with voltage balancing. The CHB inverter is a good option than other classical circuit for producing a maximum number of levels [6]-[10]. In CHB, there are two configurations: one that is symmetric and the other that is asymmetric. In a symmetrical inverter, the DC source's magnitude is the same. However, in the asymmetrical configuration, the magnitude of the DC source is not equal. The size of the DC sources has been determined using a number of algorithms [11]-[13], and it has been determined that the CHB inverter needs a significant amount of DC sources.

To rectify the above discussed circuits, various topologies have been published in [14]-[19] to address the drawbacks of the aforementioned MLI topologies. These MLIs are only suitable for high voltage applications due to the high voltage stress on devices caused by the H-bridge at the output terminals.

Numerous studies have been focused on developing new MLI configurations that are appropriate for medium voltage applications and that require fewer devices, DC voltage source, and reduced voltage stress on devices [20]-[30]. In contrast to the suggested configurations in [18]-[30], a novel MLI circuit was developed in this study that overcomes all shortcomings and uses the fewest switches possible. The suggested circuit can be used with an inverter that is symmetrical or asymmetric. Comparison analyses show that the proposed circuit uses fewer components, results in less power loss, and boosts the inverter's effectiveness. Additionally, when compared to modern topologies, the total standing voltage (TSV) across the switches is acceptable. To validate the effectiveness of the suggested circuit, simulation results for fifteen-level, seventeen-level, twenty-three-level, and thirty-one-level inverters are discussed.

The rest of the paper is structured as follows: i) section 2 presents the proposed circuit and its performance analysis in both symmetric and asymmetric configurations; ii) Section 3, comparison analyses of the suggested and other modern topologies are also discussed; iii) The simulation results using the modified switching scheme are discussed in section 4; and iv) Followed by conclusion in section 5, and the references are listed after that.

2. PROPOSED CIRCUIT

The topology consists of series connection basic cells, 6 devices and n- DC voltage (as shown in Figure 1(a). The basic cell consists of 2 DC supplies and 2 devices (S_1 and S_1') as shown in Figure 1(b). The devices S_1 and S_1' are worked in a opposite manner to avoid a fault. The magnitude of DC supplies for a basic cell is same; it is synthesis zero and $2V_{dc}$ given in Table 1. Renewable energy sources, including solar cells, fuel cells with energy storage devices like batteries, and bridge rectifiers with isolation transformers, can provide the DC voltage sources.

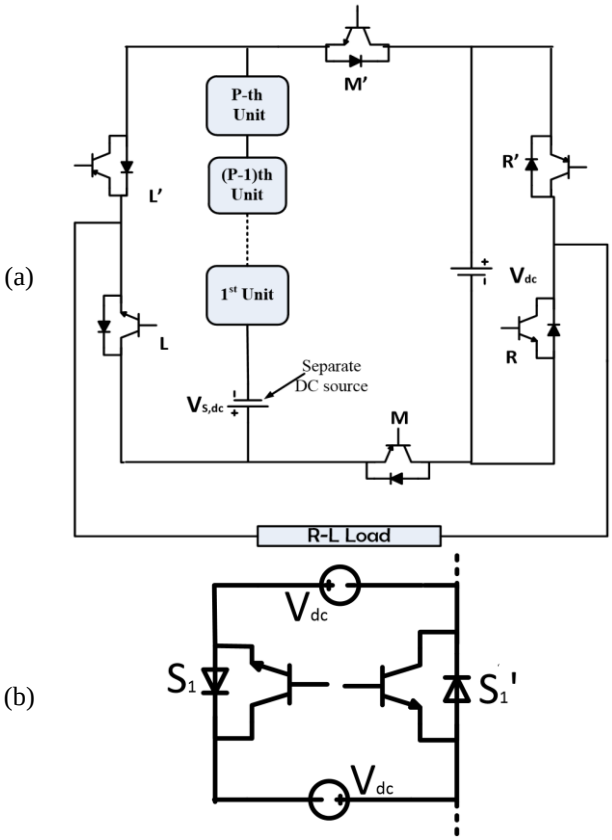

Figure 1. Suggested circuit: (a) main circuit and (b) basic unit

Table 1. Switching states of basic cell

State	S_1	Output voltage
First	ON	Zero
Second	OFF	$2V_{dc}$

2.1. Symmetric MLI

All the DC voltage sources (V_{dc}) having same values, called symmetric source MLI. The necessary count of DC sources (n), number of levels (N_{level}), and the maximum obtained output voltage ($V_{0,max}$) is written as (1)-(3).

$$V_{o,max} = V_{dc} \sum_{j=1}^{n} = nV_{dc} \quad (1)$$

$$n = (N_{level} - 1)/2 \quad (2)$$

$$N_{level} = 2n + 1 \quad (3)$$

Separate DC supplies are shown in Figure 1(a) with arrow marks according to the output voltage levels. The suggested inverter configuration can be disregarded. To generate a fifteen-level output, for instance, the circuit requires 7 input supplies, so the separated DC source is omitted. Another scenario for a seventeen-level MLI calls for 8 separate DC sources, each of which is set to be (V_{dc}).

Higher voltage levels are synthesized using the fundamental units. According to (4), which describes the correlation between p and n, the number of basic units should be an integer. With the value of p, the value of n will be updated. (5) is used to determine the quantity of power switches.

$$n = \begin{cases} 2p + 2 & with\ separate\ DC\ source \\ 2p + 1 & without\ separate\ DC\ source \end{cases} ; p = 1,2,.., \quad (4)$$

$$Nswitch = \begin{cases} (n + 4) & with\ separate\ DC\ source \\ (n + 5) & without\ separate\ DC\ source \end{cases} \quad (5)$$

For instance, each power semiconductor device generates an unnecessary voltage drop that causes the switch to lose power both when it conducts and when it changes from the ON to the OFF state. Conduction and switching losses are therefore predominately dominant. In the suggested circuit, half of the devices must be in a conducting state for any voltage to be present at the output terminal. The magnitude of the voltage drops (Vdp), which occurs while switches are operating, is used in (6). When losses are taken into account, the peak output voltage is calculated using (6).

$$V_{o,max} = V_{dc} \sum_{j=1}^{n} V_j - \left\{\frac{V_{sw}}{2} V_{dp}\right\} \quad (6)$$

2.2. Asymmetric configuration

The value of isolated DC sources from different basic units is not equal in asymmetrical MLI. For instance, the performance of MLI is improved by varying the values of the DC voltage sources for basic units. As a result, selecting DC voltage sources is crucial. To calculate the value of DC voltage, four different methods (M1, M2, M3, and M4) are suggested. The specifications for each method are listed in Table 2.

Table 2. Various constraints of the suggested asymmetrical MLI

Constraints	Method (M1)	Method (M2)	Method (M3)	Method (M4)
Separate DC source ($V_{S,dc}$)	0	1	1	2
Basic unit (p)	(n-1)/2	(n-2)/2	(n-2)/2	(n-2)/2
N_{switch}	n + 5	n + 4	n + 6	n + 5
N_{level}	$2^{(n+3/2)} - 1$	$2^{(n+2/2)} - 1$	$3 \times 2^{(n/2)} - 1$	$2 \times 2^{(n+3/2)} - 1$
Magnitude of DC source	$V_{1,1} = V_{2,1} = V_{dc}$ $V_{1,j} = V_{2,j} = 2^{j-1}V_{dc}$ j = 2, 3, …p	$V_{1,1} = V_{2,1} = V_{dc}$ $V_{1,j} = V_{2,j} = 2^{j-1}V_{dc}$ j = 2, 3, …p	$V_{1,1} = V_{2,1} = 1.5V_{dc}$ $V_{1,j} = V_{2,j} = 2^{j-1}V_{dc}$ j = 2, 3, …p	$V_{1,1} = V_{2,1} = 2V_{dc}$ $V_{1,j} = V_{2,j} = 2^{j-1}V_{dc}$ j = 2, 3, …p

It is important to note that each unit's input DC supply values are different for each of the suggested methods. By adding two additional switches to divide the DC voltage source, the proposed inverter can increase voltage levels in some solutions for asymmetric structures. This switch's new configuration with a separate DC source is depicted in Figure 2. The M3 and M4 methods require this rearrangement. Circuit reconfiguration is not required in such a case.

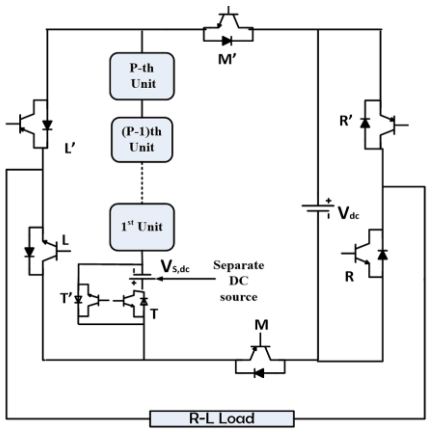

Figure 2. Generalized topologies for asymmetrical MLI

3. COMPARATIVE ANALYSIS

To verify the effectiveness of suggested MLI based on both symmetrical and asymmetrical circuits, we propose four algorithms to determine the value of input DC sources, which are compared with several asymmetrical source MLIs in [24]-[30] including classical cascade H-bridge trinary circuit. Also, relate the topologies presented in the literature [12], [18]-[23] with suggested symmetrical configurations (with and without separate DC source) depicted in Figure 3(a). As complete from figure suggested circuit with (P4) method offers fewer switches as compared to other mentioned MLIs [12], [18]-[30].

The on-state devices in MLI lead to unwanted drops that reason the occurrence of power loss. The conducting switches count is fewer in the suggested circuit as compared to contemporary topologies as shown in Figure 3(b). Therefore, the total power losses are minimized, and hence the efficiency of the inverter is improved. the number of DC supplies in different configurations is shown in Figure 3(c) as seen from comparative analysis the suggested asymmetrical configuration-based forth method requires lower DC source counts than [12], [18]-[30]. However, the second and third methods of proposed configurations require almost the same number of DC sources as [27], [30].

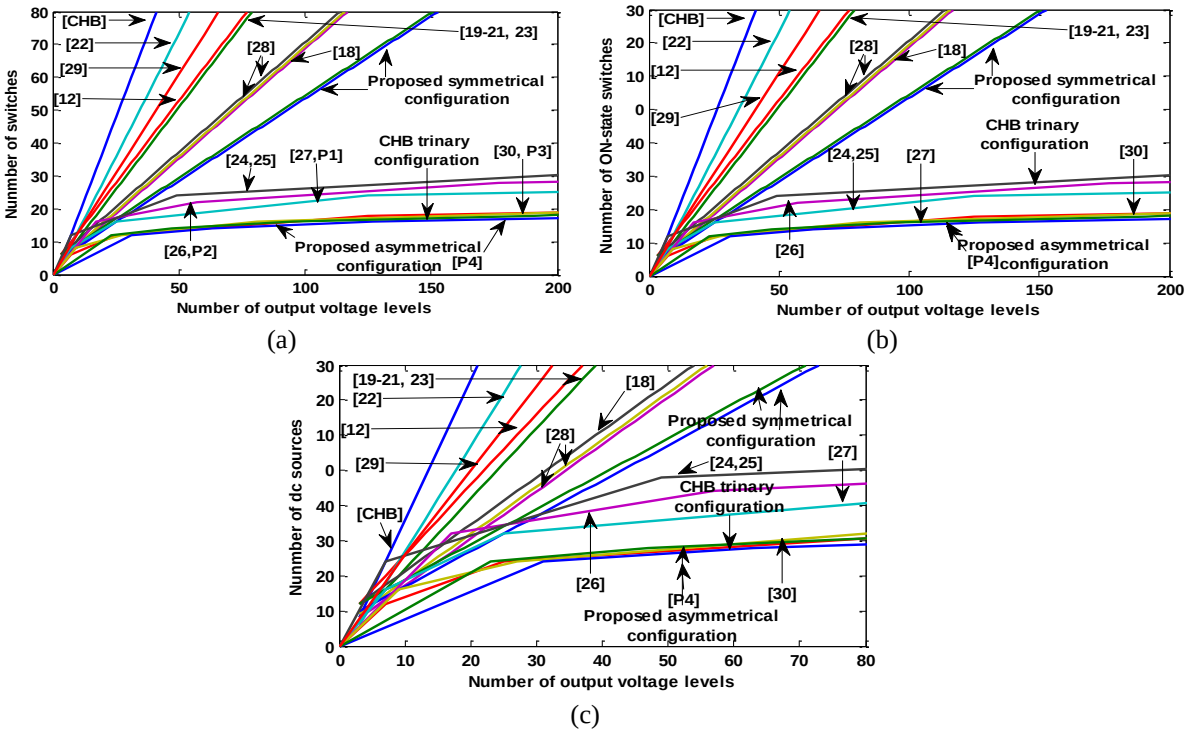

Figure 3. Comparative graphs: (a) no. of switches against no. of levels, (b) no. of on-state switchers against no. of levels, and (c) number of DC sources against number of voltage levels

4. RESULTS AND DISCUSSION

4.1. Modulation techniques for switches

The suggested circuit switches can operate both, at the fundamental and higher switching frequency. Their different modulation techniques have been proposed for inverters like nearest level control, carrier-based sinusoidal pulse width modulation (SPWM) [31], [32], and selective harmonic elimination (SHE) modulation technique [33]-[35], the intricacy of space vector modulation technique for higher levels. Likewise, SHE for the large voltage levels in the suggested circuit is not easy as it requires determining many switching angles. Therefore, a multicarrier-based scheme with a carrier frequency of 1 kHz is taken. A sinewave of 50 Hz frequency is chosen as a reference signal. In a multicarrier-based scheme (N_{level}-1) carriers are compared with reference waveform and switching signal obtained using logic operations. The corresponding signals for the 23-level inverter are illustrated in Figure 4.

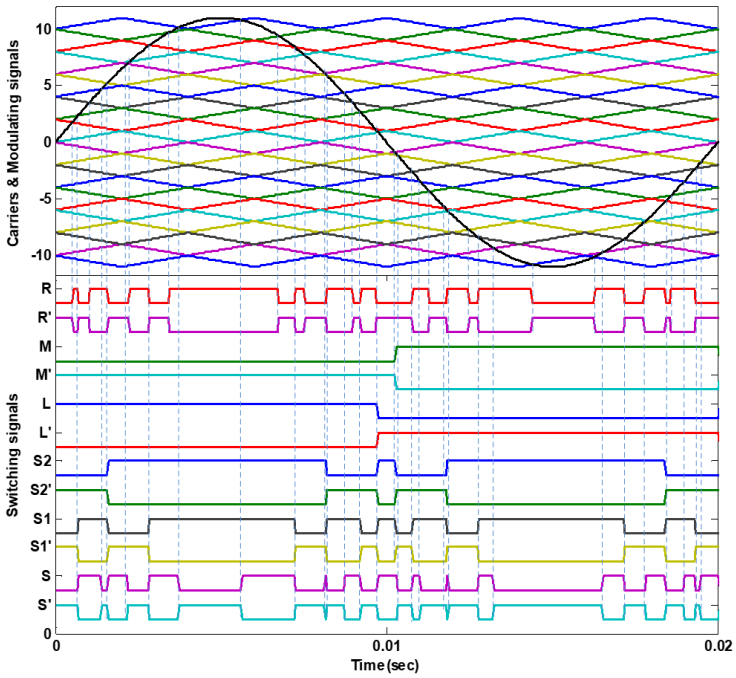

Figure 4. Corresponding signal for 23-level inverter

4.2. Simulation results

The MATLAB/Simulink software has been used to analyze simulation studies to assess the viability of the proposed concept of MLI. The 15-level and 17-level inverters that were suggested as symmetrical structures are used. The seven identically sized DC supplies make up the 15-level inverter circuit. Twelve power switches, three basic cells excluding a separate DC supply, and ten voltages of 10V each. A series RL branch (R = 18 Ω and 25 mH) is taken for output terminals. In contrast, a second independent DC source is added to the 17-level inverter, as shown in Figure 5(a).

The MLI circuit with 23 and 31 levels are used in the proposed asymmetrical source configurations as shown in Figure 5(b), the equivalent circuits of the 31-level and 23-level inverters are simulated using methods P1 and P2, respectively, based on the parameters listed in Table 2. Table 3 shows the switching sequences for the 23-level and 31-level, respectively. Different level inverters with 15, 17, 23, and 31 levels are depicted in Figures 6(a)-6(d) respectively. Voltage THD spectrum for levels 15, 17, 23, and 31 are also shown along with the voltage waveform in Figures 6(b)-6(d). The voltage waveform's total harmonic distortion (THD) was recorded as 4.25, 3.45, 2.59, and 2.15 percent for the 15, 17, 23, and 31-level voltage levels, respectively. This study demonstrates that more voltage levels produce and better THD performance.

In order to verify the robustness of the proposed inverter for operating at different modulation indices at input side variations in load at output terminals for the 15-level inverter are considered. The dynamic behavior is depicted in Figure 7 for dynamic loading. As seen from Figure 7 the variation in load, the output voltage is not affected by load current. The modulation index is changed for less time (2 ms) in 1 cycle and is verified as shown in Figure 8(a). It causes the output voltage levels get decrease from fifteen-level to five-level and load current varies during different in modulation index as shown in Figure 8(b).

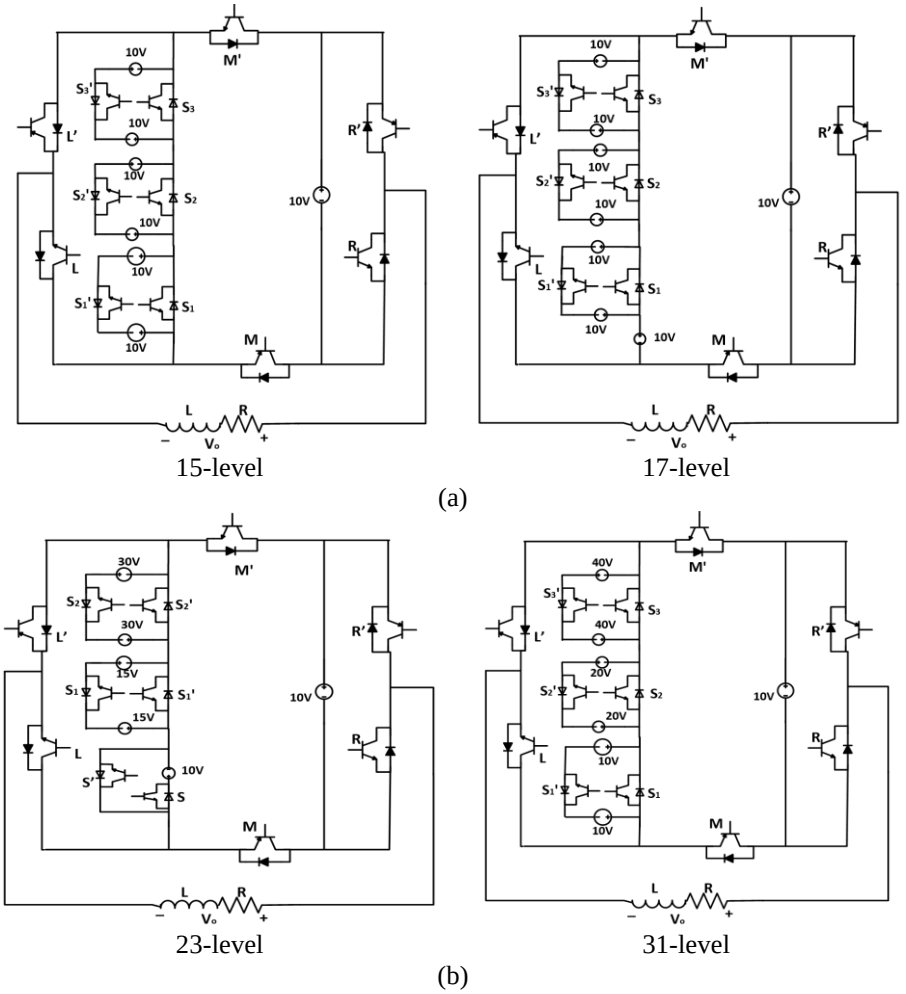

Figure 5. Circuit diagram of suggested MLI: (a) symmetrical source circuit and (b) asymmetrical source circuit

Table 3 Switching sequences for twenty-three-level inverter

States	ON state switches						Output voltage
	L	M	R	S	S_1	S_2	
I	ON	OFF	ON	ON	OFF	OFF	110 V
II	ON	OFF	ON	OFF	OFF	OFF	100 V
III	ON	OFF	OFF	OFF	OFF	OFF	90 V
IV	ON	OFF	ON	ON	ON	OFF	80 V
V	ON	OFF	OFF	ON	ON	OFF	70 V
VI	ON	OFF	OFF	OFF	ON	OFF	60 V
VII	ON	OFF	ON	ON	OFF	ON	50 V
VIII	ON	OFF	ON	OFF	OFF	ON	40 V
IX	ON	OFF	OFF	OFF	OFF	ON	30 V
X	ON	OFF	ON	ON	ON	ON	20 V
XI	ON	OFF	OFF	ON	ON	ON	10 V
XII	OFF	OFF	OFF	OFF	OFF	OFF	0
XIII	OFF	ON	OFF	OFF	ON	ON	-10 V
XIV	OFF	ON	OFF	ON	ON	ON	-20 V
XV	OFF	ON	ON	OFF	OFF	ON	-30 V
XVI	OFF	ON	ON	ON	OFF	ON	-40 V
XVII	OFF	ON	OFF	ON	OFF	ON	-50 V
XVIII	OFF	ON	ON	OFF	ON	OFF	-60 V
XIX	OFF	ON	ON	ON	ON	OFF	-70 V
XX	OFF	ON	OFF	ON	ON	OFF	-80 V
XXI	OFF	ON	ON	OFF	OFF	OFF	-90 V
XXII	OFF	ON	ON	ON	OFF	OFF	-100 V
XXIII	OFF	ON	OFF	ON	OFF	OFF	-110 V

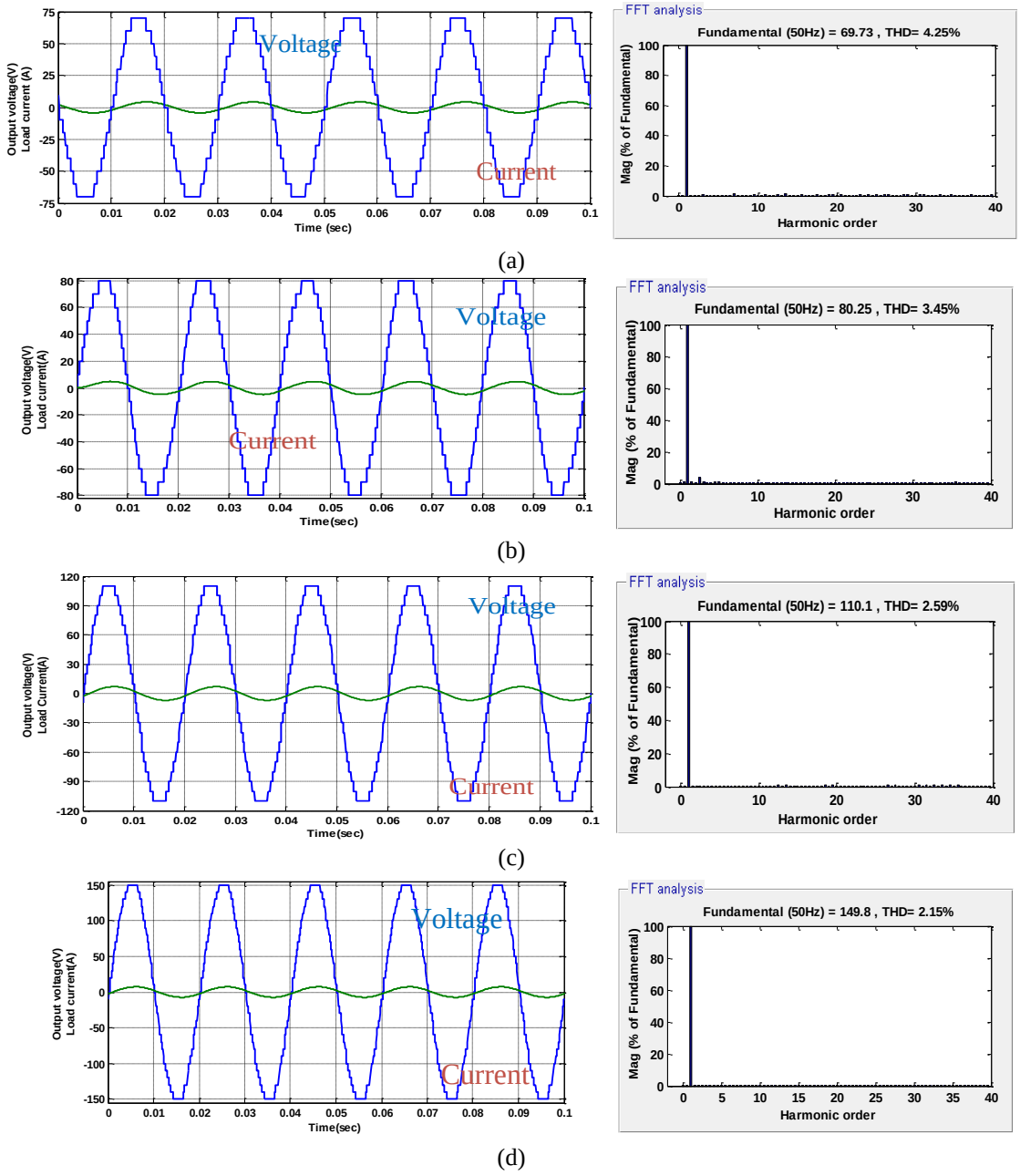

Figure 6. Simulation results for output voltage and current waveforms with voltage THD: (a) fifteen-level, (b) seventeen-level, (c) twenty three-level, and (d) thirty one-level

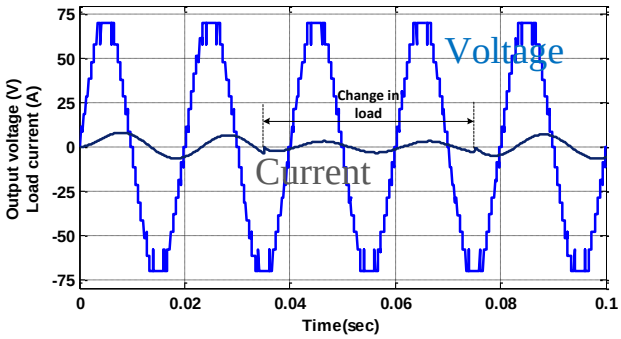

Figure 7. Simulated output waveforms during load variation

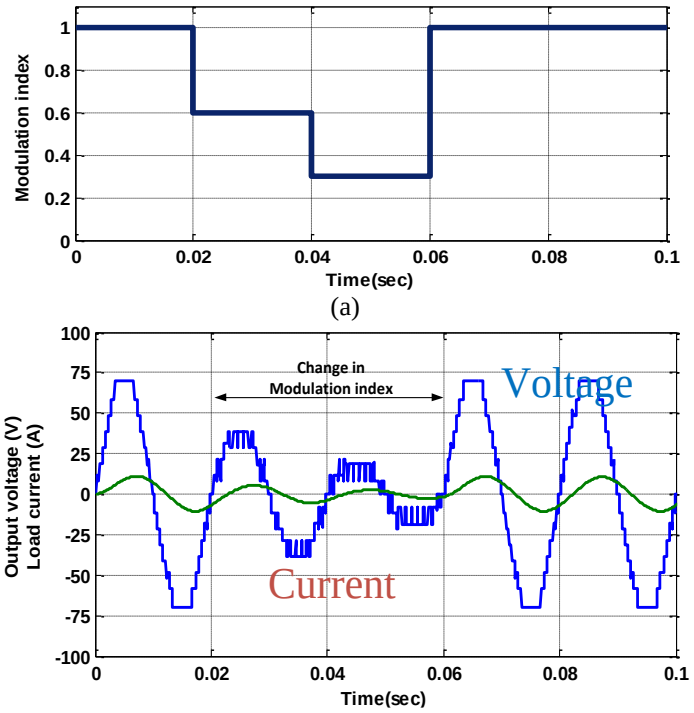

Figure 8. Simulated output waveforms for varying modulation index (a) variation in modulation index and (b) simulated waveforms

5. CONCLUSIONS

In this paper, a modified circuit for multilevel inverter has been proposed and analyzed. Generating high number of levels with minimum devices, methods for obtaining the DC supplies count are the ultimate aim of the proposed study. Also, various MLI compared with suggested circuit in terms of number of devices, voltage stress on devices and DC supplies. The obtained total harmonic distortion (THD) for voltage waveform is lowest 2.59, and 2.15 percentage for the twenty level, and thirty-one level inverter, respectively. The provided theoretical in constant load and change in load verify the efficacy of suggested circuit to generate maximum number of voltage levels with remarkably reduced devices count.

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