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Phase-locked loop based synchronization schemes for three-phase unbalanced and distorted grid: a review

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ABSTRACT

The rapidly growing dispersion of distributed generation systems into the utility grid needs appropriate control techniques to stay interconnected even under abnormal and distorted grid conditions to ensure the overall grid stability. To avoid the loss of renewable energy sources (RES) based power generation, the disintegration of RES with respect to synchronization issues must be prohibited for efficient operation. RES control highly relies on the synchronization technique as it is faster and accurate enough to detect the utility grid variables in terms of amplitude, phase, and frequency. Mostly, the phase-locked loop (PLL) synchronization schemes are utilized for control of RES and monitoring of grid voltage. The dynamics of the grid side converter (GSC) is directly influenced by the performance and design criteria of the PLLs. This paper proposes an overall review of the performances of three phase PLL based grid synchronization methods under diverse weak grid conditions.

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1. INTRODUCTION

Recently, phase-locked loops (PLLs) are mostly used for the distributed electrical energy power generations connected with grid for synchronization purpose. PLLs are required for extracting the grid's voltage profile information like amplitude, phase, and frequency to coordinate and control the power flow between renewable energy sources (RES) power generation connected to main utility grid and local load though power converters as an interface [1]-[5].

The challenge for all the power electronics-based electrical system with synchronization methods is to have a stable operation under various grid disturbances such as voltage unbalances, voltage sags or swells, harmonics and direct current (DC) offsets present in the utility voltage. These kinds of disturbances are majorly caused due to the increasing dispersion of distributed generations or renewable energy systems along with power electronics devices or nonlinear power electronic loads. So, the control of the power converters for synchronization between RES converter and the utility grid is highly essential to ensure safe and effective operation.

The synchronization methods in power converters are classified as closed loop-based and open loop-based strategies [6], [7]. The closed loop-based synchronization needs a feedback loop for one or more signals in its structure and is of two groups (PLLs [8]-[14] and frequency-locked loops (FLLs) [15]-[18]). This paper emphasizes the overview of prominent closed-loop PLLs with their designs and applications for solving power quality problems by improving their performance under different grid circumstances [19]-[24].

2. DESIGN AND CONTROL OF A FUNDAMENTAL PHASE LOCKED LOOP SYSTEM

The representation of the basic PLL system is defined by three numbers of basic elements as presented in Figure 1, where the phase detector (PD) detects the phase error by measuring the difference between the phase angle of the input and output signal and passes it to the loop filter (LF) for the elimination of phase error. The loop filter also called as a proportional integral controller sends an output signal that enables the voltage-controlled oscillator (VCO) to produce the estimated phase as output that follows the input for tracking the main grid phase. PD is accountable for generating phase error information as output whereas the LF drives phase error signal to become zero. Then, VCO generates an estimated synchronized signal in terms of phase as an output. The dq PLL/synchronous reference frame PLL (SRF PLL) and αβPLL/fixed reference frame PLL (FRF PLL) are the traditional PLLs with simplest implementation. PLLs are categorized into three phase and single-phase type on the basis of applications. An efficient PLL is characterized by lower computational burden, robustness to grid instabilities (i.e., imbalanced voltages, harmonics, DC offsets, inter harmonics, and frequency variations), and faster dynamic response with improved stability.

In recent years, designing of more advanced three-phase PLLs with enhanced disturbance rejection ability compared to classical SRF PLL and more modified versions of classical SRF PLL are encouraged to tackle the growing power quality problems in electrical power systems [25]-[27]. The fundamental SRF PLL [28] is a standardized PLL which is the foundation for all the extended PLLs in three-phase applications. The upcoming section presents some of the advanced versions of three-phase PLL based grid synchronization techniques which are the advanced versions of SRF PLLs with certain modifications for better performance under various grid disturbances.

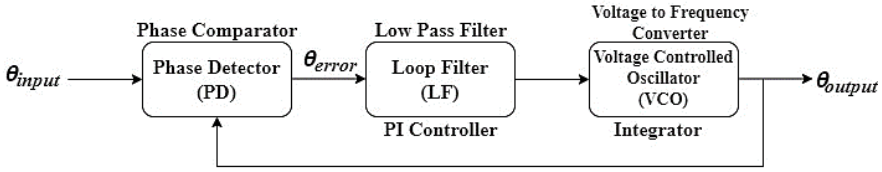

Figure 1. Basic PLL structure

3. REVIEW OF ADVANCED THREE-PHASE PLLS WITH ENHANCED FILTERING ABILITY

The increasing renewable energy resources injection into the electrical grid with the growing interconnection of the nonlinear loads have led to severe power quality problems making the synchronization process more challenging. To tackle this issue, advanced PLLs with enhanced disturbance cancellation ability have been proposed. All these PLLs are nothing but basic SRF PLL with additional filters implemented inside its control loop structure or prior to its input [29], [30]. The typical three-phase PLLs with their overall classification are summarized in Figure 2. This section presents a comprehensive review of these advanced three-phase PLL algorithms.

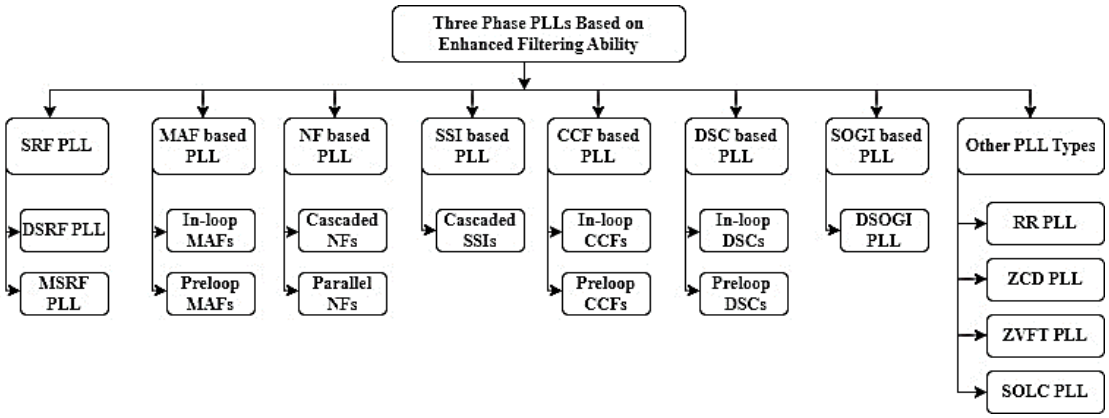

Figure 2. General classifications of three-phase phase-locked loops

3.1. Classical synchronous reference frame PLL

The conventional synchronous reference frame PLL (SRF PLL) is the basic PLL from which various modified PLLs are developed using Clarke and Park transformation modules for conversion of dq/synchronous reference frame from natural/abc reference frame. Then, proportional-integral (PI) controller is used to regulate the q variable with grid frequency as an output. After that, the utility grid phase angle is generated as an output by integrating the grid frequency as an input to VCO/integrator/phase angle generator. The obtained output phase angle is fed again back into the PD (αβ-dq transformation block) for closed-loop control. The SRF PLL is mainly utilized in three-phase grid integrated power converters due to its simplest operation with exact and fast phase or frequency assessment in mostly ideal grid conditions. The classical SRF PLL is represented in Figure 3. The SRF rotation with respect to its positive angular speed allows the classical SRF PLL in faster and precise determination of the grid frequency and phase angle in normal grid conditions that is under balanced fault circumstances. Whereas, it fails in tracking the phase angle in case of unbalanced fault condition as a result of the double grid frequency (2ω) oscillations introduced by the fundamental negative sequence components which leads to mismatch of V_d/direct axis voltage component from the positive sequence magnitude [31] of dq-components. The SRF-PLL is also unable to work properly under harmonically polluted grid voltages.

The multiple SRF filter-based PLL (MSRF PLL) is one of the famous extended versions of SRF-PLLs. The dual synchronous reference frame phase-locked loop (DSRF PLL) [2] consists of two SRF modules rotating with same angular speed though in reverse directions with a cross-feedback system intended to extricate and segregate the fundamental frequency negative and positive sequence components from the utility input voltage. The imbalanced grid input voltage has no negative consequence on the performance of the DSRF PLL but the harmonics mixed voltage as input of DSRF PLL might originate fluctuating errors in the assessed quantities. To overcome this difficulty, some SRF blocks which rotate on the basis of targeted harmonic frequencies with respect to the fundamental SRF PLL called as MSRF PLL is used [32] but more SRFs lead to increased PLL computational burden. The DSRF PLL is the mathematical equivalence of the decoupled double SRF PLL (DDSRF PLL) when the PI controller's input voltage signal is adjusted to $V_{q,1}^{+}$.

3.2. Moving average filter based PLL

Figure 4 illustrates the moving average filter based PLL (MAF PLL) [33] which is a conventional SRF PLL with a moving average filter (MAF) that is a filter of linear phase type which is defined in the Laplace domain shown as (1). Where, T_w represents the window length of MAF.

$$G_{MAF\ PLL}(s) = \frac{1-e^{-T_w s}}{T_w s} \tag{1}$$

It is noted that inclusion of MAF blocks inside the SRF PLL's control loop /in loop MAF SRF PLL remarkably improves its filtering ability but with a considerable reduction of its dynamic response due to the MAF's in-loop phase delay when MAF's window length (T_w) is same as the MAF PLL input signal's nominal period (T) that is $T_w = T$. It is recommended to select the MAF window length same as the fundamental time period of input voltage of the grid ($T_w = T$) during unknown idea about the DC offset and grid harmonic present in the PLL's input. Different selections of the MAF's window length such as $T_w = \frac{T}{2}$ and $T_w = \frac{T}{6}$ are appropriate for the applications with possible existence of odd harmonics existing in the PLL's input. The MAF permits the DC component to pass by completely blocking the integral multiple frequency components of $\frac{1}{T_w}$. For further improvement of the MAF PLL dynamics with improved harmonics filtering operation, different approaches have been recommended in the literature studies.

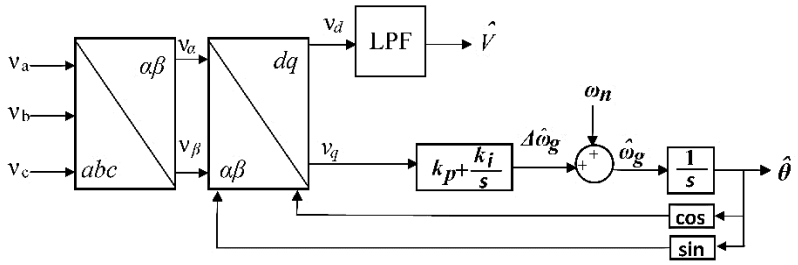

Figure 3. Basic structural diagram of a classical SRF PLL

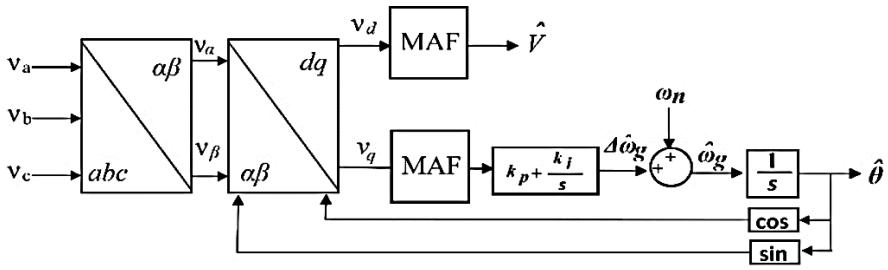

Figure 4. Basic structural diagram of the MAF PLL

The conventional PI in-loop controller replaced by an in-loop proportional integral derivative (PID) controller in the MAF PLL's LF provides additional degree of freedom. The phase delay produced by the MAF can also be efficiently canceled out by a pole-zero cancellation arrangement in the MAF PLL strategy [19]. Additionally, placing a special lead compensator prior to the MAF PLL's PI controller [34], where the compensator's transfer function that is reverse of the transfer function of MAF enables in the reduction of the phase delay in the MAF based PLL's control loop. The MAF PLL having a window length same as the fundamental time period of grid input can eliminate completely the harmonics with frequency errors and fundamental frequency distorted components.

Preview study [35], removal of in loop MAFs and by inserting them before the input of a separate SRF PLL is proposed. This MAFs based SRF behaves like a preprocessing filter that can efficiently eliminate the disturbing components there by enhancing the PLL's dynamic behavior. The proposed prefiltering phase comprises of an extra frequency detector. The removal of the added frequency detector is also possible by the amplitude scaling and phase shift correction performed by the frequency non adaptive MAF prefiltering phase inside the SRF PLL [36].

3.3. Notch filter based PLL

Generally, a band rejection filter called as notch filter (NF) is knowingly capable of attenuating frequency of specific range and passing all other frequency signals totally unaltered. This characteristic of NF enables it to cancel out the selective range of harmonic components present in the PLL input signal [19]. The NFs are classified as adaptive and non-adaptive type filters. The adaptive NF is highly chosen over the other due to easier selection of narrow bandwidth for NF thereby minimizing the PLL control loop's phase delay but increases the computational burden. The NF PLL's construction is same as the typical MAF PLL with the MAF block replaced by the NFs as illustrated in Figure 5. Inclusion of multiple NFs inside the PLL control loop topology is also considered as cascaded NF PLL and parallel NF PLL differentiated on the basis of its frequency estimation method [37], [38]. All the NFs in parallel configuration utilize the same frequency estimator whereas, each NF has its own individual frequency estimator in cascaded configuration thereby setting a trade-off between their filtering capacity and computational problem. For satisfactory performance with a robust PLL, usually three numbers of NFs with notch frequencies at $2w_g$, $6w_g$, and $12w_g$ are recommended [19].

3.4. Sinusoidal signal integrator based PLL

The representation of the sinusoidal signal integrator PLL (SSI PLL) is shown in Figure 6 where the grid's voltage is extracted by the fundamental frequency positive sequence component (FFPSC) with the SRF PLL design for an enhanced operation under unbalanced and harmonically polluted grid situations. The SSI PLL loop response speed and loop bandwidth are controlled by the parameter 'K'. An equivalent structure using a single SSI is presented in [39] that extracts positive sequence component through the single SSI filter for input grid voltage that is calculated through a 90 degree delay in the signal. The major merit of SSI-PLL is its ability to operate in unbalanced grid situations with resistance to the grid voltage distortion. Furthermore, its simplified version with certain modifications can be applied to single-phase grid application.

3.5. Complex coefficient filter-based PLL

The complex coefficient filter PLL (CCF PLL) features asymmetrical frequency response of the CCFs around zero frequency implying their ability to distinguish between the negative and positive sequence components at different frequency [40]. This trait makes the CCFs suitable for the precise extraction and nullification of harmonics/disturbance components from polluted grid input voltage before sending as input to the SRF PLL. The diagram of a popularized CCF PLL using two numbers of complex coefficient-based band pass filters (CCBFs) as prefilters inside SRF PLL loop is shown in Figure 7 which is referred as dual

complex coefficient filter PLL (DCCF PLL). The CCFs in the SRF PLL input work collaboratively to extract a specific component from the PLL input. The DCCF PLL is the mathematical alike of the DSRF PLL when the DSRF PLL has first-order LPFs with cut-off frequency w_p [41].

Preview study [41], the stability analysis, small-signal modelling and a systematic process for parameters tuning of the DCCF PLL is also mentioned. In case of dominant harmonic components, the DCCF PLL can be modified by the use of additional complex band pass filters (CBFs) centered at the chosen harmonic frequencies. The use of an in-loop PID based LF SRF PLL with a pole-zero cancellation arrangement minimizes the interconnection between the SRF PLL and CCFs thereby improving the DCCF PLL's dynamic performance and its extended form as [42]. The CCFs are also employed as in-loop filters within the SRF PLL's loop control but this topology has not yet gained much attention.

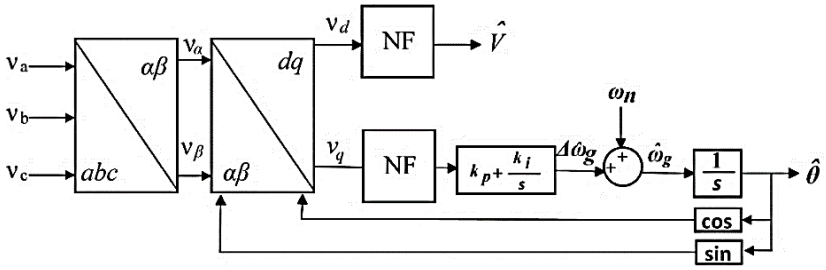

Figure 5. Basic structural diagram of the NF PLL

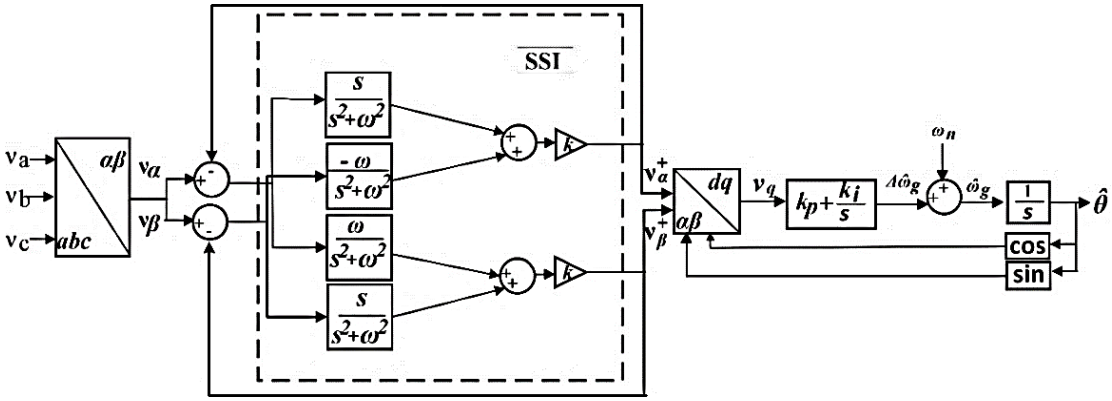

Figure 6. Basic structural diagram of the SSI PLL

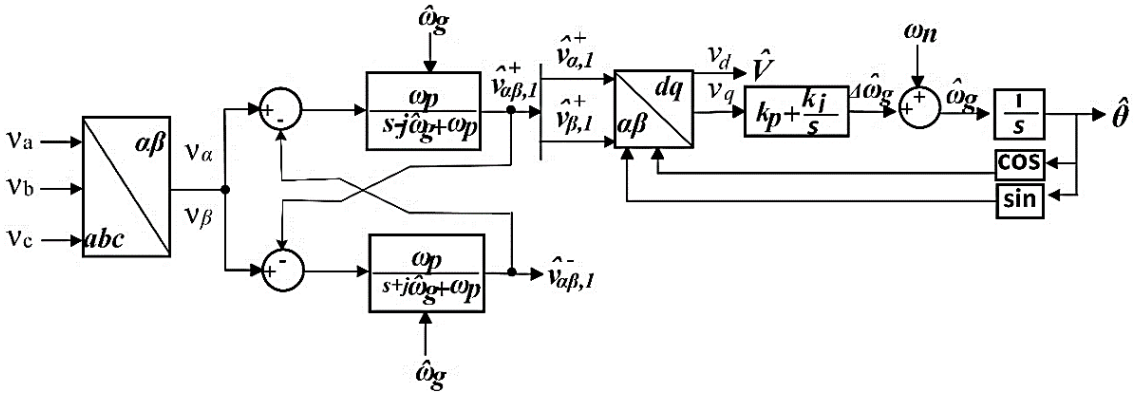

Figure 7. Basic structural diagram of the DCCF PLL

3.6. Delayed signal cancellation-based PLL

The delayed signal cancellation PLL (DSC PLL) is usually intended for enhancing the filtering ability of the standard SRF PLLs because of its simple custom features under various grid voltage conditions [43]. It is an in-loop filter of conventional SRF PLL that works like a preprocessing filter prior to the classical SRF PLL input. As increased phase delay and slower dynamic response might be caused by the DSC operators thereby causing the instability of the PLLs, they are mostly employed as a preprocessing filter for improving the filtering ability of the basic SRF PLL [19]. The expected harmonic elements of polluted three-phase grid voltages determine the DSC blocks number in the PLL's control loop. In contrast, the SRF PLL's estimated frequency is frequently fed back for adaptability to the variations in frequency of the system. Additional DSCs functioning in the SRF PLL's control loop increases the operational difficulty and computational load. The frequency feedback loop leads to an extremely nonlinear and tough-to-perform stability analysis of the PLL system. Though few different methods are presented in [19], they still need further computational efforts. Additionally, the phase and amplitude error correction methods in PLLs are recommended for computational burden reduction due to the fixed DSC delay lengths leading to easier stability analysis [44]. This method's demerit is the inability to enhance disturbance elimination capability of the frequency nonadaptive DSCs during the utility grid frequency deviation from its actual value which limits its additional usage during larger frequency drifts and serious asymmetrical grid faults.

3.7. Second-order generalized integrator-based PLL

A second-order generalized integrator PLL (SOGI PLL) works like an SSI PLL as well as behaves like a quadrature signal generator (QSG) and bandpass filter (BPF), as represented in Figure 8 [45]. Figure 8 shows its usage for the FFPSC extraction prior to the input to SRF PLL. The QSG and BPF of the SOGI also known as QSG-SOGI is an appropriate method for extracting and separating the fundamental frequency positive and negative sequence components of the three-phase grid voltage signal. Two number of QSG-SOGIs are utilized for extraction of the direct (d) and quadrature (q) axis components of V_α and V_β and then instantaneous symmetrical component method is used for the fundamental positive sequence component calculation. It has a mathematical equivalent structure similarity with the dual SOGI-based PLL (DSOGI PLL), DSRF PLL, and DCCF PLL [19]. For enhanced harmonic filtration ability of DSOGI PLL, extra QSG-SOGIs can be combined with the standard structure tuned at the harmonic frequencies [19]. Another method that is a BPF based on a third-order generalized integrator (TOGI) and a QSG (QSG-TOGI) in place of the QSG-SOGI can be used in DSOGI PLL called TOGI PLL is used for improving the dynamic response [3]. One more similar to the DSOG PLL is found in [46] that practice using an adaptive notch filter (ANF) built on the least mean square method (LMS) with two adaptive weights as a replacement for the QSG-SOGI in its structure. The QSG-SOGI and ANF are mathematically equal implying that the ANF-based PLL [46] and DSOGI PLL are mathematically equivalent structures.

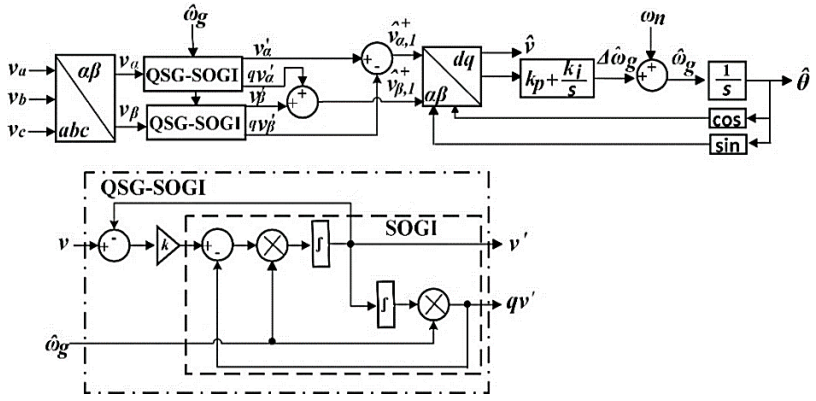

Figure 8. Basic structural diagram of the DSOGI PLL

3.8. Other three-phase PLLs

There are various types of three phase PLLs based on different applications. Preview study [47], SRF PLL's control loop has a repetitive regulator (RR) based controller inside it known as RR PLL is recommended for the efficient selective elimination of harmonic components. The RR PLL controller is built on the concept of discrete transformation whose computational problem does not depend on the numbers of input grid voltage harmonics aimed to be canceled out. So, removal of a single harmonic or a greater number

of grid harmonics needs the same computational efforts by the regulator making RR-PLL more advantageous. The higher dependency of RR PLL regulator with respect to the sampling frequency increases the computational cost during increased sampling frequency making RR PLL unsuitable for applications with higher sampling frequency.

A zero-crossing detection PLL (ZCD PLL) [48] is recommended for removing the fundamental frequency negative sequence component for generating the balanced grid signals from the imbalanced input signals. The ZCD PLL has implementation simplicity with effective operation even when the PLL input has multiple locations of zero crossings. The ZCD PLL accounts exclusively for the grid voltage amplitude imbalances as the PLL input but with inability to work during the grid voltage phase imbalances. Moreover, the ZCD PLL has a very limited harmonic filtering capacity.

The space vector Fourier transforms PLL (SVFT PLL) [49] is a sort of three-phase PLL where the SVFT works like a prefiltering phase in the SRF PLL. The SVFT successfully rejects nearly all the harmonic elements with very little computational struggle. The recursive application of SVFT filters involves possible stability issues in the electrical system which can be prohibited by the non-recursive form of SVFT implementation that might increase the computational cost. A second-order lead compensators PLL (SOLC PLL) [50] is proposed by the implementation of a SOLC scheme inside the SRF PLL where the compensators contain sets of pure imaginary poles and zeroes providing a selective harmonic elimination as the NFs don't produce phase delays in the SRF PLL. Thus, the compensators of SOLC PLLs have improved filtering ability without limiting their bandwidth but with reduced noise immunity.

4. PERFORMANCE COMPARISON OF THREE-PHASE PLLS

A performance comparison of various three-phase PLLs with their typical structures is analyzed and summarized in Table 1. In an ideal grid condition case, the most commonly used PLL is SRF PLL because of its simple structure, lower computational burden, and faster dynamic response. Due to the high sensitivity of the SRF PLL to the grid voltage imbalances and harmonics, some other PLLs like SSI PLL, DCCF PLL, and SOGI PLL are suggested to increase the system reliability towards the grid disturbances and unbalanced grid faults. Whereas, the stability performance and the dynamic response of the PLLs are the major concerns. Nearly all the PLLs in Table 1 exhibit decent dynamic response and robustness but the DSC PLL, ZCD PLL, and MAF PLL generally require PID-based prefilter block or additional phase compensator for improving the system's dynamic response that might raise the computational problem. Additionally, the ZCD PLL is inadvisable for direct application in the grid-integrated power system due to its non-adaptive frequency nature and limited harmonic filtration ability.

All of the three-phase PLLs in Table 1 benefited from different disturbance/harmonic rejection capabilities with a direct relationship between their computational burden and filtering ability. Hence, the harmonics filtering capacity of the PLLs can be modified by the addition of extra filter modules resulting in a higher computational burden. Exceptionally, only RR PLL does not face this. A higher filtering ability with a slower dynamic response has been seen in the in-loop DSC-based PLL case due to the use of multiple DSC operators in its control loop that results in an enhanced filtration ability but a sluggish dynamic response.

Table 1. Performance comparison of three-phase PLLs

Types of three-phase PLLs	Features							
	Design simplicity	Frequency adaptiveness	Harmonic extraction	Robustness to imbalance	Computational complexity	System response dynamics	Disturbance rejection ability	Filtering capacity and noise immunity
SRF-PLL	Better	Medium	No	Weak	Medium	Faster	Low	Low
MSRF-PLL	Medium	Medium	Yes	Weak	More	Faster	High	High
MAF-PLL	Medium	Medium	No	Weak	Less	Medium	Low	High
NF-PLL	Better	Medium	Yes	Medium	More	Faster	High	High
SSI-PLL	Medium	Medium	Yes	Better	More	Faster	High	High
CCF-PLL	Medium	Medium	Yes	Better	More	Faster	High	High
DSC-PLL	Medium	Medium	No	Better	Less	Medium	Average	High
SOGI-PLL	Medium	Medium	Yes	Better	More	Faster	High	High
PR-PLL	High	Medium	No	Medium	More	Medium	High	High
ZCD-PLL	Better	Weak	No	Weak	Less	Faster	Low	Low
SVFT-PLL	Medium	Medium	No	Medium	More	Faster	Low	High
SOLC-PLL	Medium	Medium	No	Medium	Medium	Faster	High	Average

5. CONCLUSION

The purpose of this research article is to deliver a comprehensive summary of the current advanced three-phase PLLs. The operational principle of the three-phase PLLs is illustrated with their merits, demerits, features, and applications. This paper reflects on the improvement of the PLL's filtering capability, and rejection ability against different disturbances by the inclusion of various filters inside the control loop after or prior to the PLL input, simplified control structure, and dynamic response of system performance under various grid situations. Lastly, the performance comparison information provided in this paper could provide immediate and easy guidance for the proper selection of suitable PLL for appropriate application by the engineers and researchers.

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