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Implementing fuzzy control for a DC-DC boost converter using FPGA

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ABSTRACT

This research explores the use of field programmable gate arrays (FPGA) to mitigate static voltage errors and reduce voltage spikes in DC-DC boost converters. Given the dynamic nature of the load impedance in these converters, FPGA is well-suited for designing systems with adaptive behavior. The study implements a fuzzy control algorithm on FPGA in a simulation environment with a small sampling period. The parallel processing capability of FPGA enables the simultaneous execution of fuzzy control algorithms, enhancing the system's responsiveness to rapid changes in load conditions. This approach minimizes voltage overshoot and effectively suppresses voltage spikes. By leveraging FPGA's high-speed parallelism and flexibility, the research demonstrates significant improvements in the dynamic performance of the DC-DC boost converter. The results highlight FPGA's potential as a robust platform for controlling power electronic systems, ensuring improved stability and efficiency under varying load conditions.

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1. INTRODUCTION

DC-DC switching converters (DC-DC SC) play a vital role in a wide array of electronic applications, facilitating the conversion of DC voltage levels efficiently. However, one common challenge encountered is voltage overshooting on the converter's output, particularly triggered by abrupt changes in load impedance. Such spikes can disrupt the performance of electronic devices or, in severe cases, cause malfunctions. To tackle this issue, an experimental model integrating a DC-DC SC and a variable load impedance was developed for practical analysis. Simulations were meticulously conducted alongside real-world experiments to validate the findings.

Recognizing the swift dynamics of DC-DC SC, traditional microprocessors fall short in implementing control algorithms swiftly enough to stabilize output voltage amidst rapid impedance fluctuations. Thus, leveraging field programmable gate arrays (FPGA) emerges as a viable solution. FPGA's parallel computing capabilities enable the execution of control algorithms concurrently with essential tasks like measurement, pulse width modulation (PWM) generation, and filtering. This parallel approach empowers the implementation of discrete-time control algorithms with remarkable responsiveness, operating at intervals below 1 μs [1]. Some of the control techniques available in literature are:

- Digital control techniques: The integration of digital control techniques, such as pulse width modulation (PWM), with FPGAs has been extensively studied. FPGAs can generate precise PWM signals required

for the operation of boost converters, with the ability to modify duty cycles dynamically based on feedback from the system. This allows for better regulation of the output voltage and reduces the impact of input voltage fluctuations and load variations.

- Advanced control algorithms: FPGAs enable the implementation of advanced control algorithms such as proportional-integral-derivative (PID) controllers, sliding mode control, and fuzzy logic controllers. These algorithms can be executed in parallel within the FPGA, leading to faster response times and enhanced performance. For example, sliding mode control implemented on an FPGA has shown significant improvements in converter efficiency and transient response compared to traditional microcontroller-based implementations.
- Real-time monitoring and adaptive control: The reconfigurability of FPGAs allows for real-time monitoring of converter parameters and adaptive control. This is particularly beneficial in applications where operating conditions can vary significantly, such as in renewable energy systems. Adaptive control strategies implemented on FPGAs can adjust control parameters on the fly, ensuring optimal performance under different operating conditions.

FPGA architectures for DC-DC boost converters: Various FPGA architectures have been explored for the control of DC-DC boost converters. These architectures range from simple single-loop controllers to more complex multi-loop systems that incorporate feedback from multiple sensors. The choice of architecture depends on the specific application requirements, such as the need for high precision, fast transient response, or minimal power consumption.

A crucial aspect of this endeavor involves crafting a controller transfer function to meet key objectives such as eradicating static errors and curtailing voltage spikes or drops when load impedance undergoes sudden changes. In essence, this integrated approach amalgamating experimental modeling, advanced control algorithm design, and FPGA utilization offers a promising avenue to mitigate voltage overshooting issues in DC-DC switching converters, thereby enhancing the stability and reliability of electronic systems [2], [3].

The DC-DC boost converter illustrated in Figure 1 serves the purpose of elevating DC input voltage to a higher level of DC voltage. It operates in two distinct phases: during the first phase, switch T is turned on, converting input energy into magnetic energy stored within inductor L. In the subsequent phase, switch T is turned off, allowing inductor L to release energy through the current, thereby replenishing capacitor C. Diode D1 plays a crucial role in preventing current flow from the capacitor to ground when switch T is on. The dynamic behavior of this converter is described by a nonlinear mathematical model, as in (1).

$$\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}u_d - \frac{R_L}{L}\cdot i_L - \frac{1}{L}\cdot u_0 \cdot \big(1-\delta(t)\big)\\ \frac{du_0}{dt} &= \frac{1}{C}\cdot i_L \cdot \big(1-\delta(t)\big) - \frac{1}{RC}\cdot u_O\end{aligned} \quad (1)$$

Where iL is the inductor current, u_0 is the capacitor or output voltage, R_L is the inductor resistance, L is the inductance, C is the capacitance, R is the load resistance, and $\delta(t)$ is the average conduction ratio of switch T.

To facilitate linear controller design, it's essential to derive a linear dynamic model that captures the system's behavior near its operational point, particularly focusing on small signal perturbations [4], [5]. This is achieved using the state space averaging technique, transforming the nonlinear model from (1) into both large-signal and small-signal models, as presented in (2).

$$\begin{aligned}\frac{dI_L}{dt} + \frac{d\tilde{I}_L}{dt} &= \frac{1}{L}\cdot(U_d+\tilde{u}_d) - \frac{R_L}{L}\cdot\big(I_L+\tilde{I}_L\big) - \frac{1}{L}\cdot(U_0+\tilde{u}_0)\cdot\big(1-\Delta_p-\tilde{\delta}\big)\\ \frac{dU_0}{dt} + \frac{d\tilde{u}_0}{dt} &= \frac{1}{C}\cdot(I_L+\tilde{\imath}_L)\cdot\big(1-\Delta_p-\tilde{\delta}\big) - \frac{1}{RC}\cdot(U_0+\tilde{u}_0)\end{aligned} \quad (2)$$

In which the uppercase capital letters stand for average signals and the small letters with "~" for small-signal perturbations.

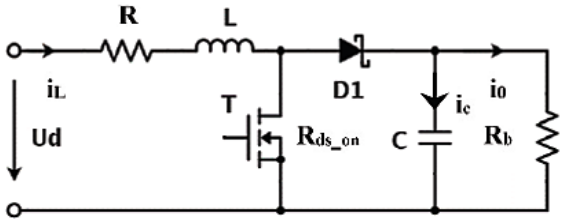

Figure 1. DC-DC boost converter

The static model, as described in (3), is derived by omitting all small-signal components from the system's representation. This involves setting derivatives to zero, effectively capturing the system's behavior under steady-state conditions.

$$\frac{dI_L}{dt} = \frac{1}{L} \cdot U_d - \frac{R_L}{L} \cdot I_L - \frac{1}{L} \cdot U_0 \cdot (1 - \Delta_p) = 0$$
$$\frac{dU_0}{dt} = \frac{1}{C} \cdot I_L \cdot (1 - \Delta_p) - \frac{1}{RC} \cdot U_0 = 0 \quad (3)$$

The (4) can be used to determine the ratio between output and input voltages [5]. This voltage ratio is contingent upon the conduction ratio of the switch, denoted as Δ_p, as well as certain constants governing the operational point of the system. Notably, the voltage U_0, load resistance R, and inductor current I_L, although not fixed constants, represent average values at the operating point. That is the main reason for the voltage error at the output when switching among different loads R.

$$\frac{U_0}{U_d} = \frac{R \cdot (1 - \Delta_p)}{R_L + R \cdot (1 - \Delta_p)^2} \quad (4)$$

2. DYNAMIC MODEL OF DC-DC CONVERTER

The linear dynamic model, as presented in (5), is provided in the context of a small-signal model. This model is derived from nonlinear models by combining large-signal and small-signal components [6]. Notably, all products of small signals are considered negligible, given their inherently small values. Additionally, small variations in the input voltage $\tilde{u}$ can be disregarded, assuming a stable power source for the input voltage.

$$\frac{d\tilde{I}_L}{dt} = \frac{R_L}{L} \cdot \tilde{l}_L - \frac{1}{L} \cdot \tilde{u}_0 \cdot (1 - \Delta_p) + \frac{1}{L} \cdot U_0 \cdot \tilde{\delta}$$
$$\frac{du_0}{dt} = \frac{1}{C} \cdot \tilde{l}_L \cdot (1 - \Delta_p) - \frac{1}{C} \cdot I_L \cdot \tilde{\delta} - \frac{1}{RC} \cdot \tilde{u}_0 \quad (5)$$

Utilizing Laplace transformation on the linear model described in (5), the transfer function of the DC-DC boost converter was obtained. This transfer function succinctly captures how the output voltage dynamically responds to small changes in the conduction ratio.

$$F_{\tilde{\delta}}(s) = \frac{\tilde{u}_0(s)}{\tilde{\delta}(s)}$$
$$= \frac{-s \cdot L \cdot I_L + (U_0 \cdot (1 - \Delta_p) - I_L \cdot R_L}{s^2 \cdot L \cdot C + s\left(\frac{L}{R} + C \cdot R_L\right) + \frac{R_L}{R} + (1 - \Delta_p)^2} \quad (6)$$

To determine the final linear switch function (eight) of the converter, the subsequent operating point parameters as in (7) have been taken into consideration in the general form of the transfer function in (6).

$$U_d = 7.4\ V$$
$$U_0 = 14\ V$$
$$L = 15\ \mu H$$
$$C = 33\ \mu F$$
$$R_b = 33\ \Omega$$
$$R_L = 0.081$$
$$\Delta_p \approx 0.48$$
$$I_L \approx 0.8159\ A$$
$$f = 500\ kHz \quad (7)$$

$$F_{\tilde{\delta}}(s) = \frac{-1.224e^{-5}s + 7.214}{4.95e^{-10}s^2 + 3.128e^{-6}s + 0.2729}$$
$$R(s) = K_r \cdot \frac{s^2 + 6318.2 \cdot s + 551240138}{s^2 + 189546 \cdot s}$$
$$K_r = 0.534 \quad (8)$$

3. LOAD WITH CHANGEABLE IMPEDANCE

For experimental purposes with the DC-DC converter, a specially designed load was created to facilitate rapid changes in impedance, encompassing various traits like inductance (L), capacitance (C), and resistance (R). Leveraging a microprocessor allows for the development of tailored impedance switching

algorithms. The fundamental component arrangement is illustrated in Figure 2. Typically, the components are arranged into three parallel branches, each representing distinct load types such as RLC, RC, RL, and R. The flexibility of this setup lies in the ability to adjust certain element values by configuring parallel elements within each branch. Furthermore, any combination of parallel branches can be established to mimic a wide range of load scenarios [7]. In this context, there's no necessity for a dynamic load model, as the primary objective is to assess the converter's performance under unpredictable impedance changes [8], [9]. The focus remains on creating realistic load conditions to evaluate the converter's resilience and efficiency in handling dynamic impedance alterations.

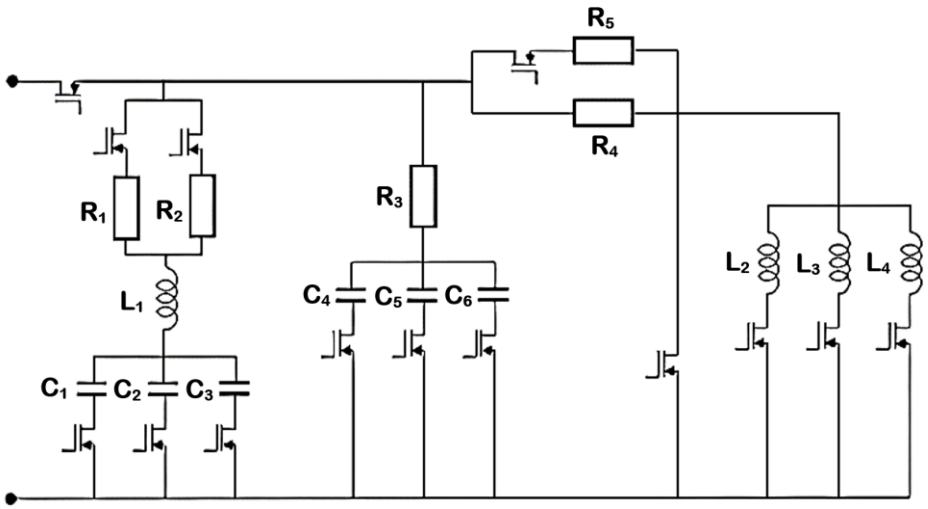

Figure 2. Element arrangement for changing impedance load

4. DESIGN OF FUZZY CONTROL ALGORITHM

A transfer function was carefully selected for the implementation of the fuzzy controller. The placement of poles and zeros was meticulously determined to fulfill the requirements of the closed-loop system [10], [11]. These requirements are primarily aimed at removing static errors in the output voltage and reducing over/undershoots of voltage when impedance changes occur.

In the design process of the fuzzy controller, only a linear dynamic model of the DC-DC converter was utilized at a specific operating point [12]. This enabled the creation of a controller that could effectively address the system's dynamics under typical operating conditions. The developed controller was rigorously tested using both a nonlinear simulation model and a nonlinear prototype, both of which operated at the chosen operating point [13]. This comprehensive testing approach ensured the controller's robustness and effectiveness across different scenarios, validating its performance in real-world applications.

The root-locus plot of the linear system depicted in Figure 3 illustrates the configuration of poles and zeros, indicating a non-minimal phase system. Notably, there's an unstable zero located to the right of the origin, while the complex poles are predominantly clustered near the left side of the origin. To address voltage under/overshoot issues, the approach taken is to enhance the system's relative stability [14]. This involves shifting the complex poles towards the left side and closer to the horizontal axis. By doing so, the system's response becomes more stable, reducing the likelihood of overshooting and enhancing overall performance [15], [16]. This adjustment aims to create a more resilient and dependable control system, better equipped to handle dynamic variations and disturbances.

An integral pole was positioned at the coordinate origin in order to achieve the original goal of removing static voltage inaccuracy. Any static inaccuracy in the output is essentially eliminated by this integral process. All relevant factors were carefully taken into account when creating the fuzzy controller's transfer function. Pole-zero compensation is made possible by the numerator in (9) matching the denominator of the system transfer function as in (8). Two poles were located at the coordinate origin and a considerable distance to the left of the stable half-plane, respectively, with respect to the denominator of the controller's transfer function. This pole was limited to half the sampling frequency in order to comply with the Shannon theorem. The highest frequency of any pole in our instance was just under 200 kHz, using a sampling frequency of 500 kHz.

It was crucial to ascertain the controller gain Kr. In the closed-loop system, this gain aligns the system poles with the root-locus. In order to move the closed-loop system poles more to the left of the compensated poles and closer to the x-axis than the compensated poles, the gain Kr was chosen. Furthermore, a larger gain indicates a faster closed-loop system reaction [17]. The root-locus diagram shown in Figure 4 was used to calculate the value of gain Kr.

The (5) shows the second-order transfer function of the controller after the numerator, denominator, and gain were determined. Every modeling and transfer function analysis was carried out in the frequency and continuous time domains. The transfer function had to be transformed into a discrete form, as shown in (8), in order for the control algorithm to be implemented practically on a digital device. The "Tustin" discretization method was used to accomplish this conversion, and the discrete system was running at a sample frequency of 500 kHz.

$$R(s) = K_r \cdot \frac{s^2+6318.2 \cdot s+551240138}{s^2+189546 \cdot s}$$
$$K_r = 0.534 \quad (9)$$

$$R(Z) = \frac{0.452z^2-0.8973z+0.4463}{z^2-1.681z+0.6813} \quad (10)$$

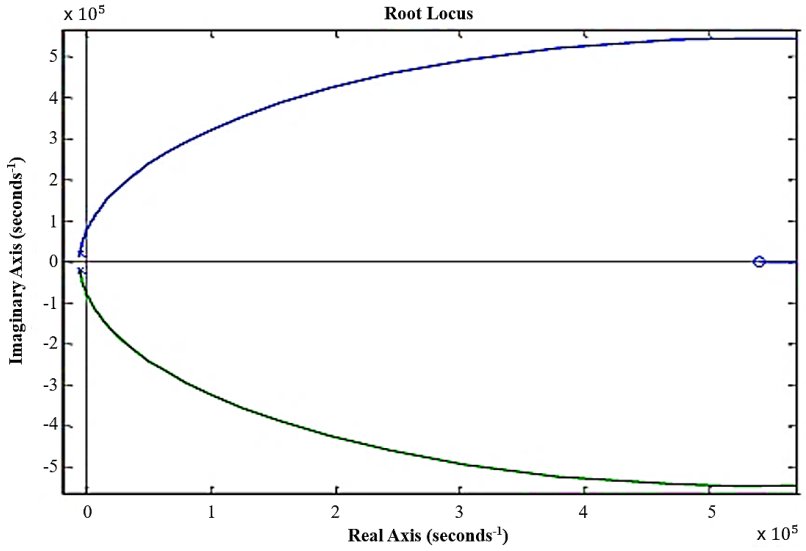

Figure 3. Root locus of a linear transfer function

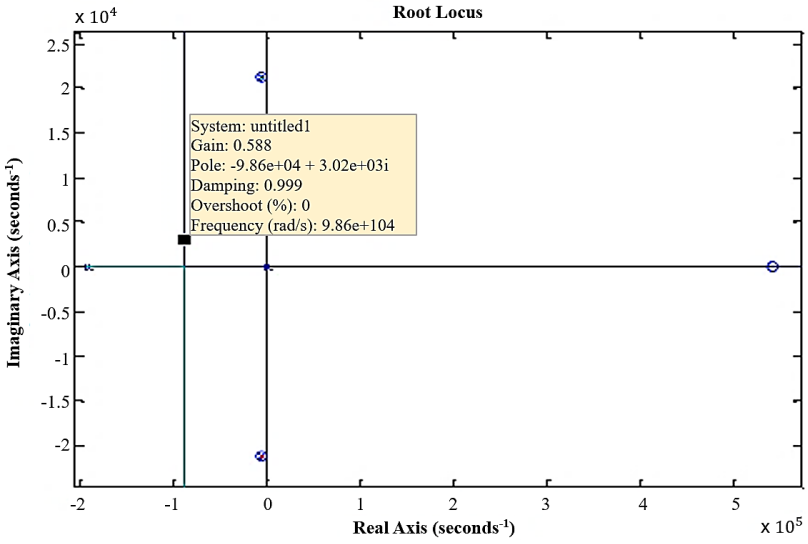

Figure 4. Root locus of open-loop system with fuzzy controller

5. FPGA BASED CONTROL OF DC-DC CONVERTERS

Regarding the frequencies of the system's poles, the control loop frequency must meet a minimum of 400 kHz. Conventional microprocessors frequently struggle to achieve such high frequencies. However, FPGA is another method that makes it possible to design a control algorithm at such frequencies. FPGA technology offers the processing power and flexibility required to satisfy real-time demands. It guarantees that, for a single sample, the time spent on all calculations inside the series does not surpass the sampling time. An FPGA from Xilinx's Spartan-3E family with core 3S500 was used in the research [2]. To make the controller's discrete transfer function given in (8) compatible with the digital device given in (11), it must be converted into a discrete differential equation. This conversion guarantees the smooth integration of the controller with the FPGA-based system and is necessary for practical implementation.

$$Y(k) = 1.681 \cdot Y(k-1) - 0.6813 \cdot Y(k-2) \\ +0.452 \cdot X(k) - 0.8973 \cdot X(k-1) + 0.4463 \cdot X(k-2) \quad (11)$$

The output of the above differential equation is determined by the sum of all products; hence, each product must be calculated before computing the output value [18]. Multipliers for each product can be implemented simultaneously to accomplish this. The period of the sum, or one clock pulse, coincides with the multiplication time. Thus, just two clock pulses are needed to calculate the transfer function in its differential form. In low-level digital circuits, shifting is the process of delaying all inputs and outputs until the second clock pulse, when the sum is calculated.

Maintaining computation accuracy is a problem in integer arithmetic, particularly given the high frequency of the system poles. To solve this and guarantee enough accuracy, all coefficients must be scaled up to a higher factor. An alternative is to make use of a floating-point unit (FPU). However, the FPU needs more clock pulses for processing and uses more digital elements than traditional multiplication. Additionally, delays are introduced by conversions from AD/DA converters between floating-point and integer values, which use more clock pulses. These factors highlight how difficult it is to perform precise computations at high frequencies in digital systems while preserving effectiveness and reducing resource usage.

6. PARALLEL TASKS IMPLEMENTED ON FPGA

The control method is just one of several tasks that the FPGA must perform. Some of these responsibilities include PWM modulation, command execution, high sample rate digital filtering of both channels, high sample rate channel data collection, and serial communication with the computer for voltage and current measurements [10], [11]. Each of the tasks in Figure 5 executes rapidly and simultaneously.

The digital filters were created as transfer functions and are constructed similarly to the controller. The filter transfer functions, however, typically have a higher order. The digital filters' fourth-order transfer functions, which are independent of the order of the transfer function, ensure consistent calculation speed [19]. These filters remove noise associated with high-frequency switching.

Data conversion is an important component of data processing along the entire chain, from capture to control. For this task, the relative digital data from the AD converter needs to be transformed into physical values. Additionally, acquiring measurements and communicating serially with the computer are crucial tasks [20], [21]. Through measurement acquisition, output voltage and inductor current samples can be acquired, sent to a computer, and plotted for further examination and tracking. Collectively, these responsibilities guarantee accurate data gathering, filtering, control, and communication with external devices in addition to the effective operation and performance of the FPGA-based system.

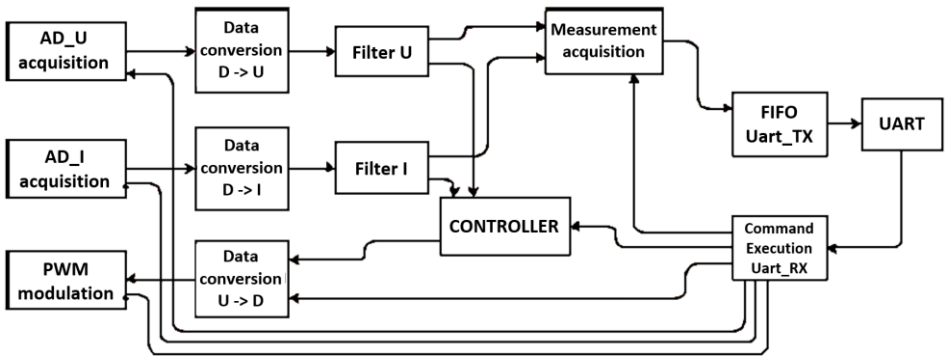

Figure 5. Tasks running in parallel on FPGA

7. EXPERIMENTAL RESULTS

As shown in Figure 6, the converter was tested by turning on and off different branches of load elements. Five milliseconds was the duration of the load change. A graphical user interface (GUI) was created using LabVIEW software to record and visualize the output voltage measurement graph and modify various FPGA settings.

The experiment was carried out with an "unknown" load because the control design did not include the load model. Two distinct loads were dynamically switched between by the fuzzy controller according to their respective properties. The DC-DC converter operated at its best under a variety of operating situations thanks to the controller's ability to adjust to changes in the load impedance [22], [23].

Only the second branch of the load's element—which corresponds to a capacitive load—was altered in the first experiment. Figure 7 shows the voltage and current readings that the FPGA recorded and transmitted to the computer. The voltages of the regulated and non-controlled systems differ noticeably from one another. Given that static error has been totally eradicated and voltage undershoot has been much decreased, it is clear that both requirements have been satisfied [24]. The operational point requirements are in line with the output voltage reference [25]. The second experiment involved turning the full load on and off. The voltage and current data made during the second experiment are shown in Figure 8. Similar gains are noted, including the elimination of static faults and a decrease in voltage undershoot [26].

However, in the regulated system, there are additional oscillations recorded shortly after the load is switched on [3]. The greater dynamics of the regulated system are the main cause of this phenomenon. Furthermore, the PWM generator's low resolution of 1% adds to the controlled system's instability. These results demonstrate how well the fuzzy controller reduces static errors and voltage undershoot while also pointing out areas that need more improvement to handle transient instabilities.

The resulting PWM signal operates at 1000 MHz, which is 100 times smaller than the input frequency of 100 MHz used by the PWM generator. The PWM signal's resolution, which is 1/100th or 1% of the conduction ratio, is likewise impacted by this frequency difference. Changing the conduction ratio by ±1% causes the output voltage to change by about ±250 mV while the converter is functioning at its operational point. Nevertheless, the fuzzy-controlled system's output voltage does not show these notable amplitude steps. This is explained by the way the system behaves as a filter. Higher dynamics are found in the noise in the measured voltage that is sent to the system input through the PWM conduction ratio.

However, this high-frequency noise cannot be efficiently transferred due to the system's slow dynamics. This efficiently filters out the high-frequency noise since the system only "feels" the average value of the conduction ratio in PWM. In the fuzzy-controlled system, this phenomenon contributes to smoother and more stable voltage regulation.

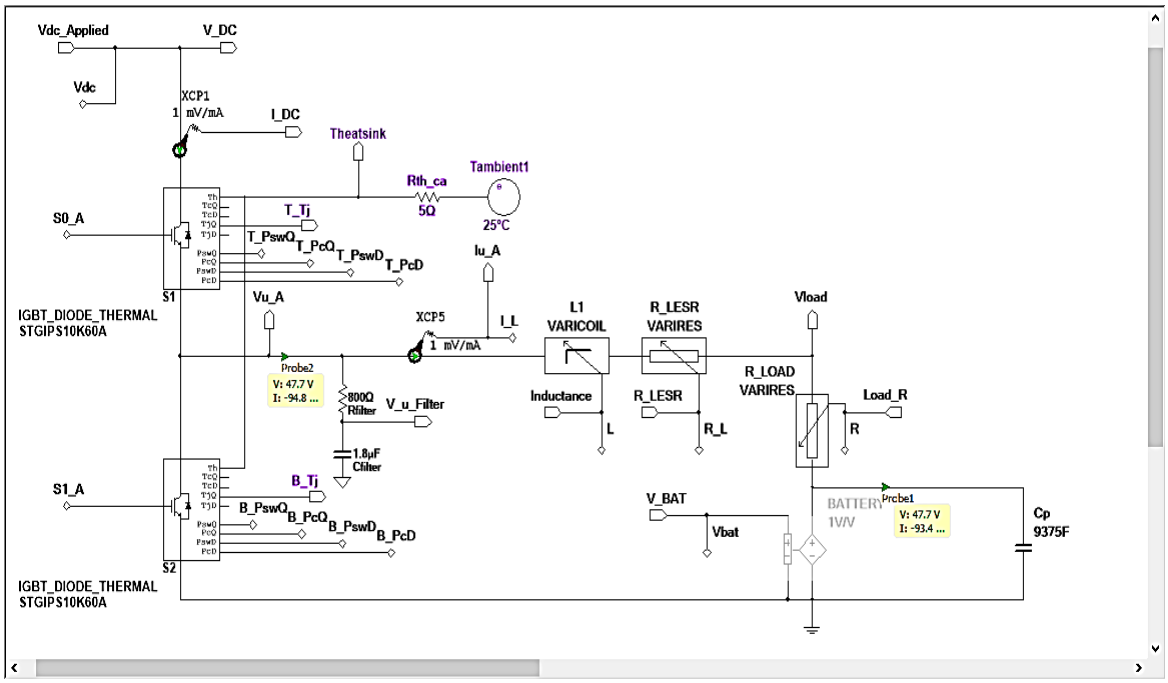

Figure 6. FPGA real-time digital simulator

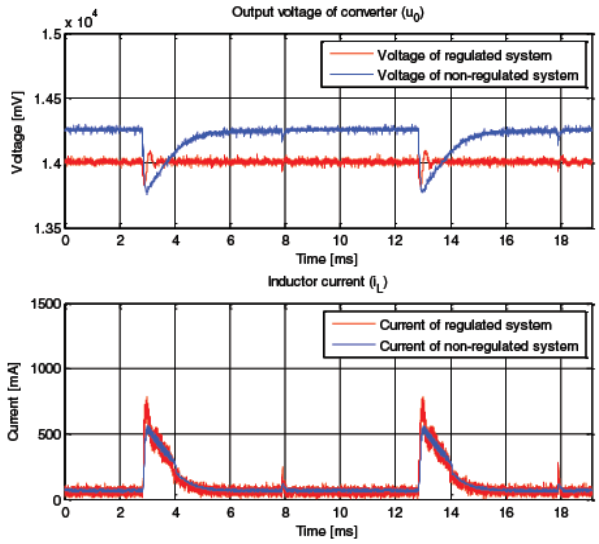

Figure 7. Switching of a second load branch (capacitive load)

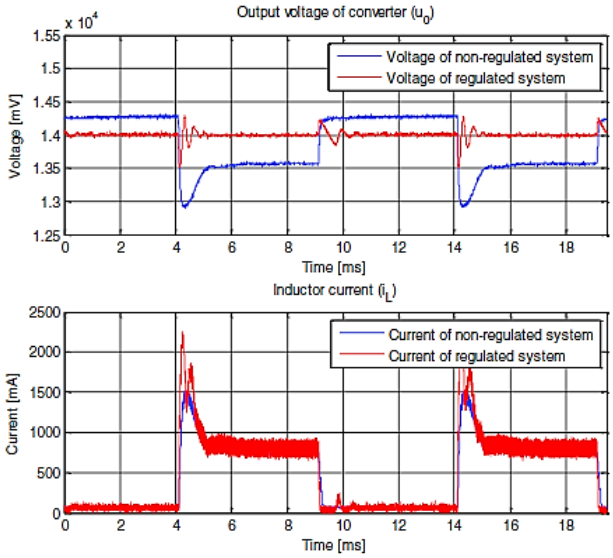

Figure 8. Switching of an entire load at once

8. CONCLUSION

Even though there were issues with the conduction ratio's low resolution, the experiments' results were judged adequate. Designing an external analog PWM modulator with a 16-bit DA converter to precisely set the duty cycle is one possible way to solve the resolution problem. The greatest resolution with this configuration might be 1/16384, which would equal to a step size of roughly 1.5 mV. This kind of PWM resolution improvement could greatly increase the controlled system's stability. Both trials accomplished their initial goals, confirming the effectiveness of the FPGA-based parallel control system. Furthermore, the converter's expected performance and the adjustable load were verified. Further developments in the subject can be facilitated by exploring and experimenting with different kinds and structures of fuzzy control algorithms using such experimental models. Overall, in spite of early difficulties, the trials produced positive outcomes and offer a strong basis for further study and advancement in the field of fuzzy control algorithms and their use in DC-DC converters.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state that there is no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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