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Asymmetrical nine-level hybrid multilevel inverter design and analysis for electric vehicle applications

Gerri Ratnaiah, Ramya Ganesan
Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology,
SRM Institute of Science and Technology, Ramapuram Campus, Chennai, India

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ABSTRACT

A novel type of single-phase hybrid multilevel inverter (HMLI) is proposed in this paper. A hybrid system is made up of a multilevel inverter coupled to an H-bridge unit and which can generate nine-level output. To synthesize an output voltage waveform with nine steps, this setup uses merely seven power switches, two diodes, and two DC supplies. A greater number of steps were achieved in output voltage through suggested circuit with a smaller number of components than other existing multilevel inverter (MLI) topologies. A finer output waveform that is closer to a sinusoidal shape is produced with less total harmonic distortion (THD) because of the greater number of steps in the output voltage. Furthermore, it prolongs the switches' lifetime and lowers the voltage stress across them, increasing reliability. In addition, the system produces fewer switches than necessary, resulting in lower power losses and increased efficiency. This guarantees the suggested system's small size and inexpensive cost. A comparison between the suggested topology and the most current MLI topologies has been conducted to highlight the key components of the proposed topology. The suggested topology has been controlled using three distinct controlling schemes are phase disposition-pulse width modulation (PD-PWM), phase opposition disposition-PWM (POD-PWM), and alternative phase opposition disposition-PWM (APOD-PWM).

Corresponding Author:

Ramya Ganesan
Department of Electrical and Electronics Engineering, Faculty of Engineering and Technology
SRM Institute of Science and Technology, Ramapuram Campus
Ramapuram, Chennai, Tamil Nadu, India
Email: ramyag@srmist.edu.in

1. INTRODUCTION

DC-AC converters are a crucial component of electrical power systems that provide changeable frequency and magnitude in output. Multilevel inverters have become very popular, particularly in the realm of DC/AC converters, academic and industry research. This interest comes from a variety of advantages that multilevel inverters have over traditional inverters, which reduces the output waveform's harmonic content with a lot of steps in the output voltage waveform. Moreover, the physical dimensions of the AC side filter elements are reduced. In addition, the output waveform's large step count extends the lifetime of the switching components and lowers their voltage stress and dv/dt rate, improving system reliability. For the same output power level, the more steps in the waveform of output voltage have the benefit of reducing the switching devices' rating when compared to a conventional converter. This lowers the multilevel inverter (MLI) system's cost and size and makes it more packageable [1]. Three major categories of traditional MLIs: cascaded H-bridge multilevel inverters (CHB-MLIs), flying capacitor multilevel inverters (FC-MLIs), and neutral point diode clamped multilevel inverters (NPC-MLIs).

Hybrid electric vehicle (HEV) and renewable energy integration industries continue to use these topologies extensively. Compared to common flying capacitors and neutral point clamped topologies, losses are lower with a conventional cascaded H-bridge inverter since it simply uses switches. The balance of capacitors is another issue related to flying capacitors. Additionally, neutral point clamped structures only provide half voltages at the output levels. To get around these limitations, a lot of work has gone into creating unique MLI topologies that can yield greater steps in output voltage waveform with limited switches and DC voltage sources. Regarding this, numerous topologies with symmetrical and asymmetrical configurations have been presented [2], [3].

Several innovative topologies with a range of applications have been published in this field since the initial attempt at the MLI was provided in 1981 with three-level NPC. The authors in [4]-[7] presented new MLI topologies with 13 and 17 levels of output and different modulation schemes, and they are suitable for renewable applications. Hybrid multilevel inverter design and analysis for asymmetric input voltages have been presented in [8], [9]. These topologies address the design of a single-phase hybrid multilevel inverter for a standalone system using asymmetrical voltage input sources and three-level T-type, diode clamped legs, and H-bridge MLI. In comparison to traditional topologies, this architecture requires fewer switches to reach the output voltage level. An asymmetric configuration for the 15-level topology is proposed in [10]. This topology naturally produces both positive and negative cycles without the need for an extra H-bridge unit, thus lowering the inverter's overall standing voltage.

A recently designed multilevel inverter with a hexad voltage-boosting capability has been presented in [11]. It uses a single source with just fourteen switches, two diodes, and four capacitors to create a 13-level waveform. By connecting the DC source and capacitors in parallel at multiple points during an operational cycle, during the inverter's switching, proper magnitude of the voltage at the capacitors is maintained. In [12], [13], there is another topology that aims to minimize the number of switching devices. A prototype of a nine-level quadruple boost inverter (NQBI) topology is shown in [14], which runs on a single solar photovoltaic source and uses less switches, capacitors, and diodes. With the help of this topology, the voltages of the two capacitors are effectively balanced, giving the output nine voltage levels. A new multilevel inverter topology presented in [15], for multilevel voltage generation, stacked voltage sources taken from single DC link and series-connected capacitors. A detailed analysis of a pencil-shaped (PS) 9-level inverter with reduced components that was constructed with just two DC sources was provided in [16]. An analysis of the benefits and drawbacks of multilevel inverter topologies in electric vehicle applications was published in [17]. A new topology and survey with less no of switching devices was presented in [18], [19]. Muhammad *et al*. [20] presented an adaptive hybrid control strategy in conjunction with a cascaded reduced switch symmetrical multilevel inverter to efficiently and steadily inject power produced from distributed energy resources into the utility grid.

In this paper, a unique hybrid MLI topology with an enhanced H-bridge unit is presented. This setup generates an output voltage with 9 steps using just 7 switches, 2 diodes, and 2 DC sources. Compared to the traditional approach, the suggested system achieves several output steps with fewer components and facilitates versatile operation. By contrasting the suggested system with the recently developed MLI topologies, the uniqueness of the suggested system has been demonstrated. The suggested topology will also be suitable for other domains such as renewable energy (solar, wind, and tidal), grid-to-vehicle (G2V), and vehicle-to-grid (V2G). This topology outperformed the other designs when the number of distinct components was considered.

This paper is divided structurally as follows: Section 1 presents a literature review and an introduction has been provided; the existing and suggested hybrid system, including its structure and switching scenarios, is described in section 2. To illustrate the major features of the suggested system, section 3 will compare it with a few current topologies. Section 4 has outlined the various control methods for the suggested system. In section 5, the results and the discussion are given. In section 6, the work's conclusion is presented.

2. NEW TOPOLOGICAL HYBRID MULTILEVEL INVERTER (HMLI)

2.1. Design of the system

The suggested novel nine-level hybrid multilevel inverter system is depicted in Figure 1. The suggested design included three diodes, D1, D2, D3, and two DC sources (Vdc1 = 3 V and Vdc2 = V), in addition to seven power switches (S1 to S7). As a result, this topology falls into the group of asymmetrical MLI topologies. These components were all joined together into one unit to create a 9-level voltage waveform as the output. The suggested topology is precisely constructed to prevent any chance of a short circuit occurring along any of the circuit routes.

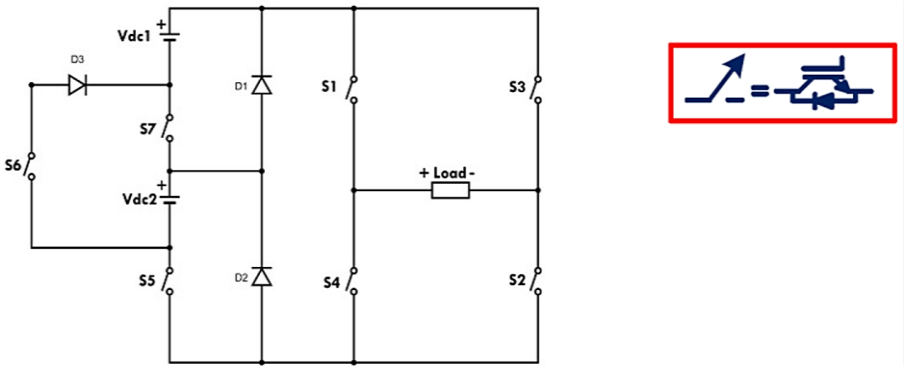


Figure 1. Diagram illustrating the suggested 19L hybrid MLI architecture

2.2. Modes of operation of proposed system

The proposed structure was developed to generate waveform of an output voltage with nine levels restricted quantity of switching devices and dc voltage sources. For this topology, a total of four positive levels, four negative levels, and one zero levels switching state have resulted in the production of nine distinct switching states. Every level includes a different loop with specific switches that must be turned ON to reach the desired level. Figure 2 provides a detailed explanation of each of these switching scenarios separately.

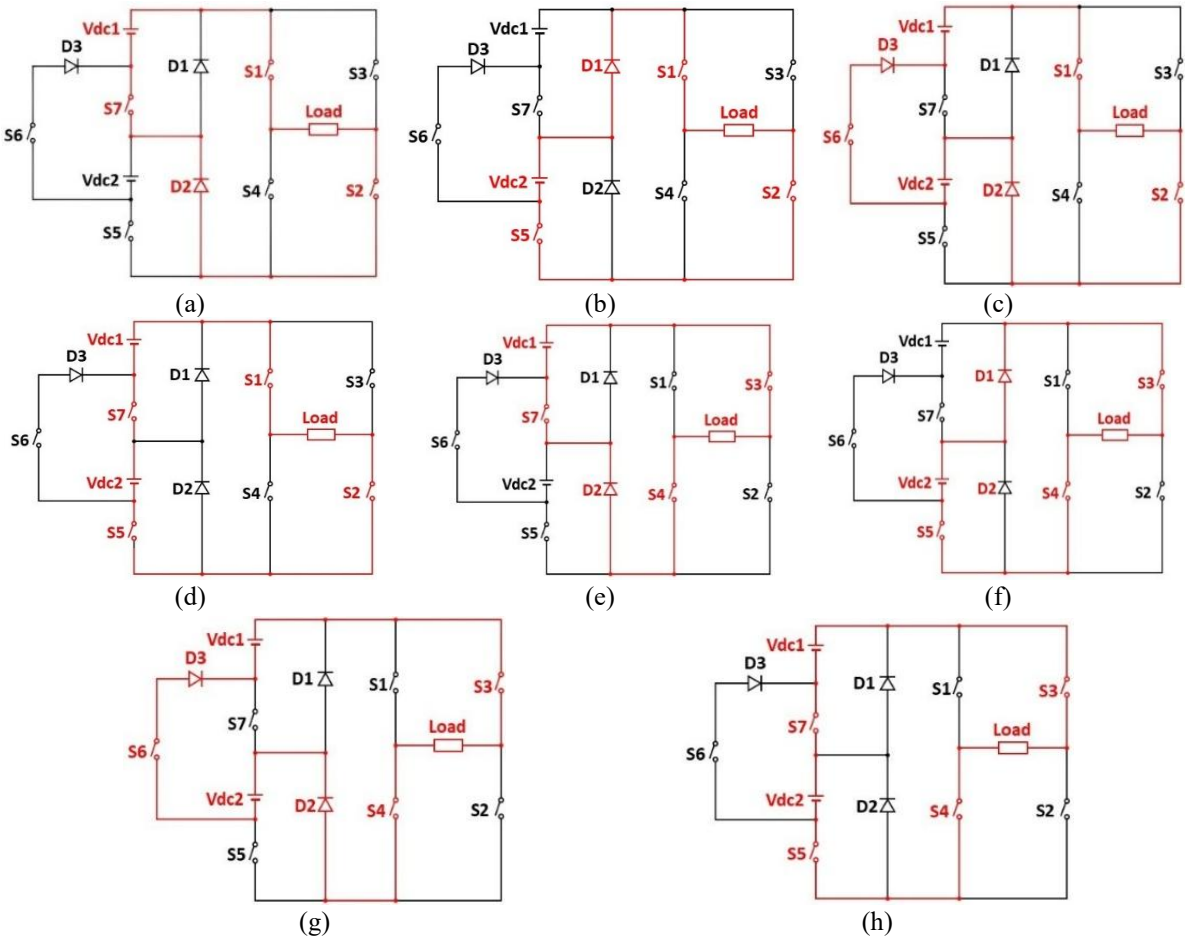


Figure 2. Detailed operation of 9-level hybrid MLI at different levels: (a) Vo=Vdc1, (b) Vo=Vdc2, (c) Vo=Vdc1-Vdc2, (d) Vo=Vdc1+Vdc2, (e) Vo=-Vdc1, (f) Vo=-Vdc2, (g) Vo=-(Vdc1-Vdc2), and (h) Vo=-(Vdc1+Vdc2)

Table 1 shows the elements that can be used in each level generation procedure [1]. From Table 1, the switching operation for different output levels is shown in Figure 3. For positive cycle the switches S1, S2, S5, S6, and S7 are in ON position and remaining switches are in OFF position, whereas for negative cycle switches S3, S4, S5, S6, and S7 are in ON position and remaining switches are in OFF position. Switches S1, S3, or S2, S4 are in ON position and the remaining switches are in OFF position to get zero voltage at the load.

Table 1. Various operating stages for the suggested system

Switching states	Vout	Closed loop Current path
1	$V_{dc1}+V_{dc2}$	S_1, S_2, S_5, and S_7
2	V_{dc1}	S_1, S_2, S_7, and D_2
3	$V_{dc1}-V_{dc2}$	S_1, S_2, S_6, D_2, and D_3
4	V_{dc2}	S_1, S_2, S_5, and D_1
5	0	S_1, S_3 or S_2, S_4
6	$-V_{dc2}$	S_3, S_4, S_5, and D_1
7	$-(V_{dc1}-V_{dc2})$	S_3, S_4, S_6, D_2, and D_3
8	$-V_{dc1}$	S_3, S_4, S_7, and D_2
9	$-(V_{dc1}+V_{dc2})$	S_3, S_4, S_5, and S_7

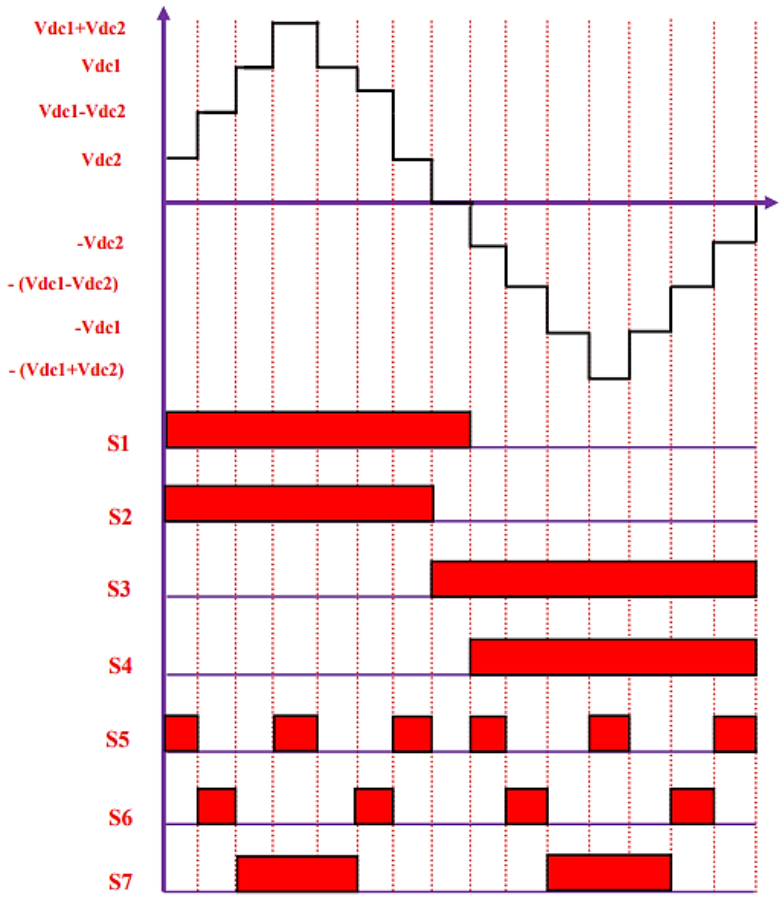


Figure 3. Switching scheme for one cycle

2.3. Computing the total standing voltage (TSV)

The selection of a power device is significantly influenced by the voltage stress across the switches. Generally, total standing voltage (TSV) is the overall voltage stress across all power switching devices, accounting for all voltage steps TSV [1].

$$TSV = \sum_{i=1}^{m} V_{Si} \quad (1)$$

Where m is the number of power switching devices. There are 7 switching devices in the suggested topology, so that (1) can be modified as (2).

$$TSV = \sum_{i=1}^{7} V_{Si} = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} \quad (2)$$

One important component of the topology design is the voltage stress on the switches. The suggested structure is shown in Figure 1 with the magnitude of DC sources as Vdc2 = V, Vdc1 = 3 V, the switches' voltage stress is given by (3) and (4).

$$V_{S1} + V_{S2} + V_{S3} + V_{S4} = Vdc1 + Vdc2 = 3\,V + V = 4\,V \quad (3)$$

$$V_{S5} + V_{S6} + V_{S7} = Vdc2 = V \quad (4)$$

Considering the above equations, the TSV of the proposed topology is 19 V [1]. TSV is a measurement of each switch's per-unit voltage stress. It is the relationship between the switches' peak voltage stresses of all switches and peak output voltage [4]. TSV in p.u calculation is given in (5).

$$TSV_{pu} = \frac{V_{S1}+V_{S2}+V_{S3}+V_{S4}+V_{S5}+V_{S6}+V_{S7}}{Vdc1+Vdc2} = 4.75 \quad (5)$$

3. COMPARATIVE STUDY

The proposed topology mainly consists of two dc voltage sources, five driving circuits, and seven power switches. The comparison with the majority of the most recent topologies is displayed in Table 2. With the exception of the topologies offered in the publications [21]-[33], the suggested topology has less components overall. Fewer switches, driver circuits, and DC sources, as well as three diodes and zero capacitors, all contribute to the suggested topology's reduced circuit footprint and increased topology dependability. Same number of power electronic switches in the topology presented in [30], [32], but [32] has more DC sources than the proposed topology. The TSV and cost factor are also less compared to other topologies.

A multilevel inverter's cost factor (CF) is determined by the product of TSV with a constant σ and the cost of its component parts. σ = 0.5 and σ = 1.5 are the constant values chosen for the comparison that is shown below. The cost component is calculated as (6) [4].

$$Cost\ Factor\ (CF) = N_{SW} + N_{GD} + N_D + N_C + N_S + \sigma \times TSV \quad (6)$$

From Table 2, the comparative study presented in Figure 4. The X-axis is taken as multilevel inverter topologies and Y-axis is taken as number of switches in Figure 4(a), the number of gate drive circuits in Figure 4(b), the number of capacitors in Figure 4(c), the total standing voltage in Figure 4(d), and cost factor per level in Figure 4(e). From the comparative study of different topologies (references), the suggested MLI had minimum in switching devices, gate drive circuits, and capacitors. The cost factor per level is also low for the current MLI.

Table 2. Comparison of various multilevel inverters' outcomes

Top	Levels	N_{SW}	N_{GD}	N_D	N_C	N_S	$TSV_{p.u.}$	CF/L	
								σ =0.5	σ =1.5
[21]	11	12	9	0	0	3	5	2.40	2.86
[22]	13	16	16	4	4	2	5	3.42	3.80
[23]	9	8	8	0	2	2	4.5	2.47	2.97
[24]	7	10	10	0	3	1	5.3	3.80	4.56
[25]	7	9	9	1	3	1	5.3	3.66	4.42
[26]	9	12	12	0	2	1	5.5	3.30	3.91
[27]	9	11	11	0	2	1	5	3.05	3.61
[28]	9	10	10	1	2	1	7.5	3.08	3.91
[29]	9	17	15	0	4	1	7.25	4.51	5.31
[30]	9	12	10	0	3	1	6	3.22	3.88
[31]	9	9	9	0	2	1	6.25	2.68	3.37
[32]	9	12	10	0	1	2	5	3.05	3.61
[33]	9	8	8	3	3	1	6.5	2.91	3.63
[P]	9	7	5	0	0	2	4.75	1.81	2.34

N_{SW} = number of switches, N_{GD} = number of gate drives, N_D = number of diodes, N_C = number of. capacitors, N_S = number of sources

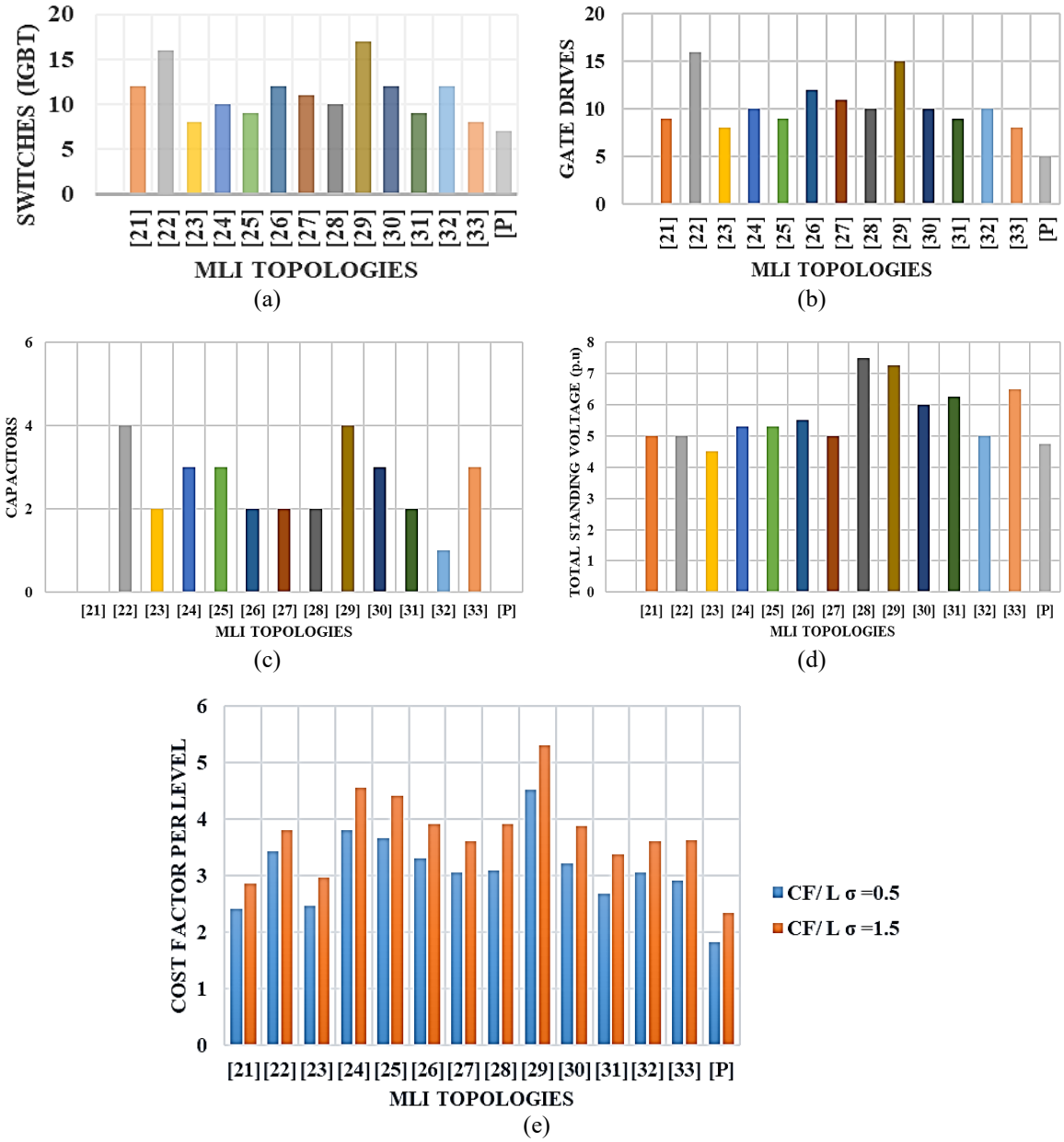


Figure 4. Comparing MLI topologies with (a) number of switches, (b) number of gate drives, (c) number of capacitors, (d) TSV, and (e) cost factor

4. MODULATION TECHNIQUES

In an MLI, the primary goal of pulse width modulation schemes is to generate a train of switching pulses that produce a sinusoidal waveform at the output voltage. THD in the output can be decreased by using these strategies correctly. Reference and carrier signals are compared in modulation techniques. It is necessary to use carrier waves for N-level inverters is (N-1). Multi-carrier based sinusoidal pulse width modulation (MCSPWM) is the most widely utilized modulation technology [18]. The ratio of the peak magnitudes of the carrier waveform and the modulating waveform is called the modulation index (MI).

Different modulation schemes have been implemented (X-axis is taken as time and Y-axis is taken as modulation index value) on the suggested nine-level structure. Figure 5 shows phase disposition pulse width modulation (PDPWM), Figure 6 shows phase opposition disposition pulse width modulation (PODPWM), and Figure 7 shows alternate phase opposition disposition pulse width modulation (APODPWM). Modulation schemes have been implemented in the proposed system, and a comparison is shown [34].

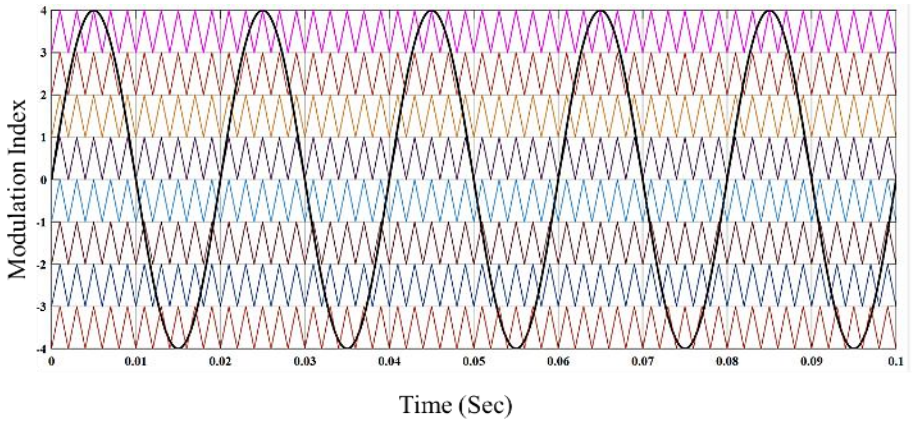


Figure 5. Phase disposition PWM (PDPWM)

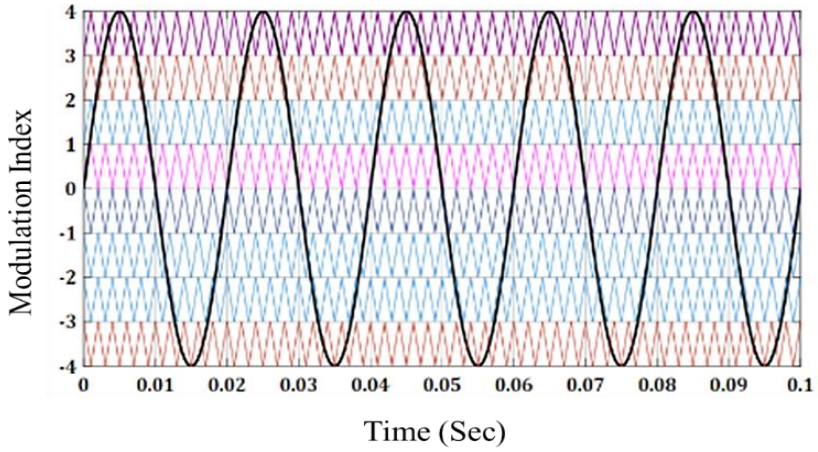


Figure 6. Phase opposition disposition PWM (PODPWM

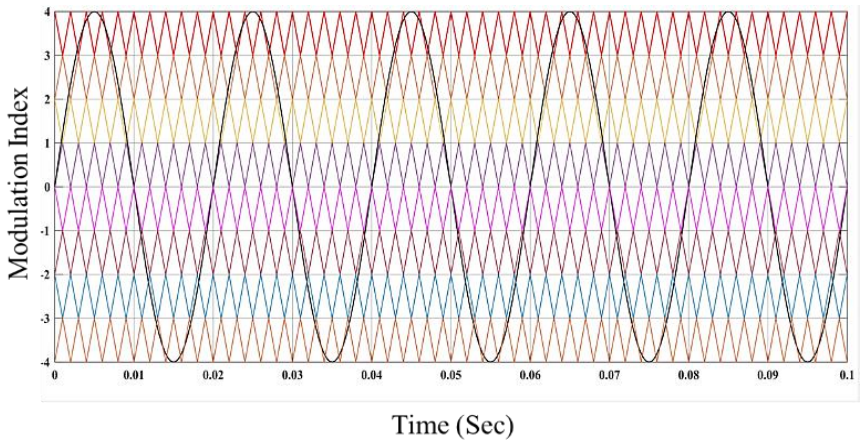
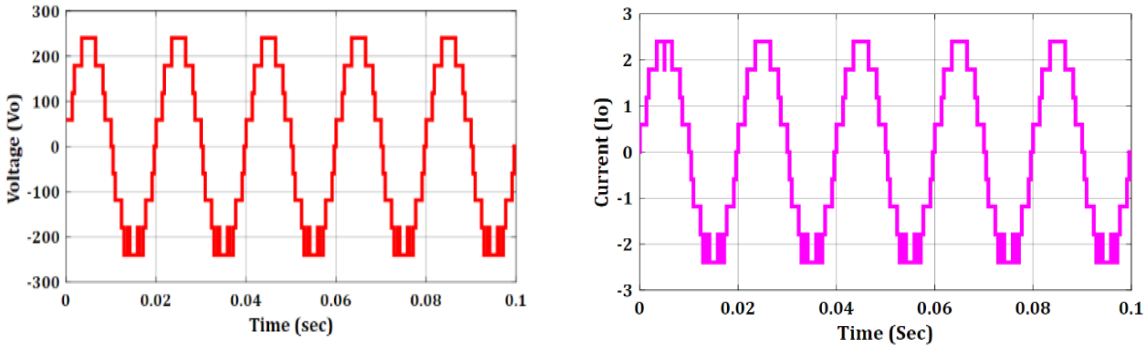


Figure 7. Alternate phase opposition disposition PWM (APODPWM)

5. RESULTS AND DISCUSSION

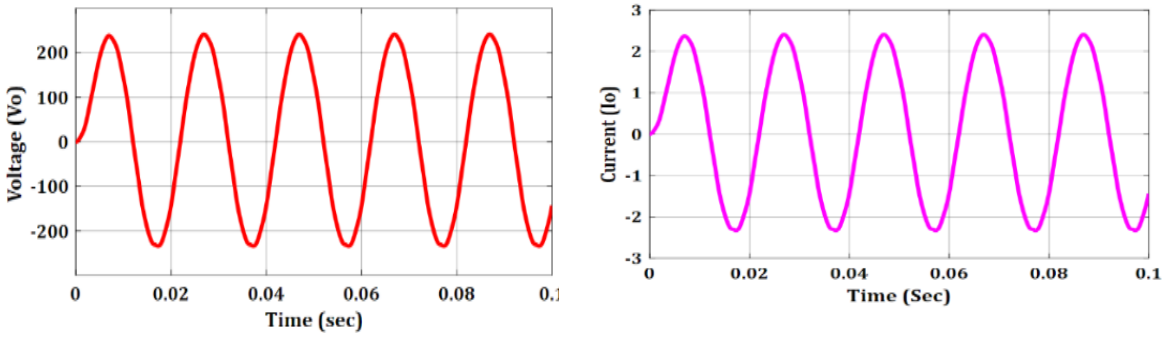
MATLAB software has been used to simulate the suggested nine-level topology. The various simulated waveforms and THD for the suggested structure are displayed in Figures 8-16. The following are the 9-Level MLI simulation parameters. The DC voltage sources are Vdc1=180 V, Vdc2=60 V, resistance is R=10 Ω. When a resistive load (R=10 Ω) is taken, the AC output voltage at its peak of 240 V, the output current reaches a maximum value of 2.4 A. At a carrier signal frequency of 2000 Hz, three different

modulation techniques, PDPWM, PODPWM, and APODPWM, were employed in this research paper. Figure 8 shows output voltage and output current using PDPWM scheme. Figure 9 shows output voltage and output current using PDPWM scheme with a filter. Figure 10 shows output voltage and output current using PODPWM scheme. Figure 11 shows output voltage and output current using PODPWM scheme with filter. Figure 12 shows output voltage and output current using APODPWM scheme, and Figure 13 shows output voltage and output current using APODPWM scheme with filter. Total harmonic distortion (THD) is calculated using FFT analysis in MATLAB/Simulink and comparison results were tabulated in Table 3. Figure 14 shows THD analysis for PDPWM, Figure 15 shows THD analysis for PODPWM, and Figure 16 shows THD analysis for APODPWM. After comparison of three control schemes, PODPWM technique has lower THD.



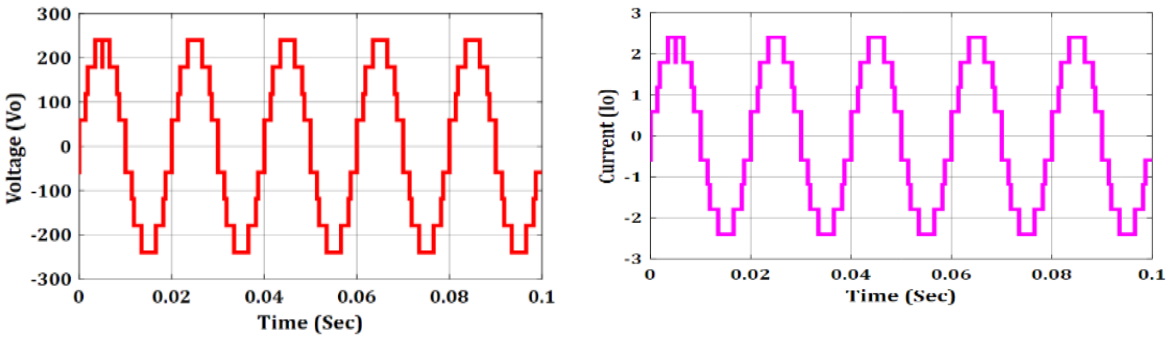
(a) (b)

Figure 8. Suggested HMLI with PDPWM technique: (a) output voltage (V_0) and (b) output current (I_0)



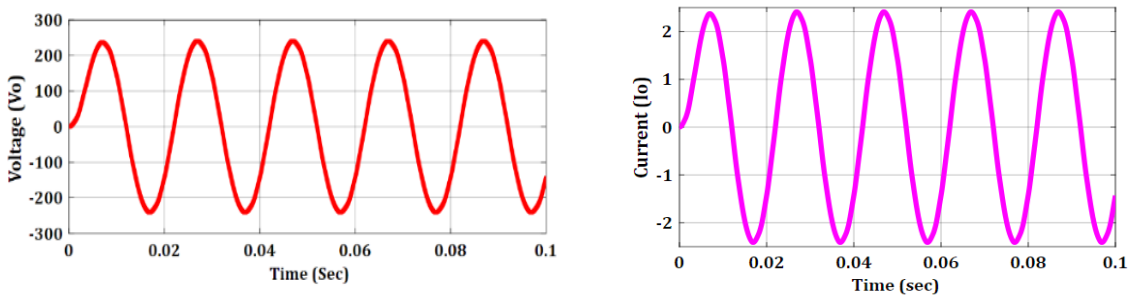
(a) (b)

Figure 9. Suggested HMLI with PDPWM technique using filter: (a) output voltage (V_0) and (b) output current (I_0)



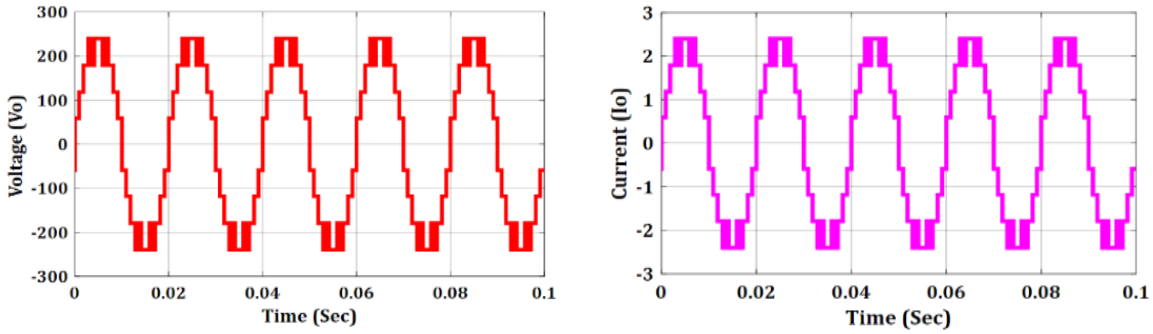
(a) (b)

Figure 10. Suggested HMLI with PODPWM technique: (a) output voltage (V_0) and (b) output current (I_0)



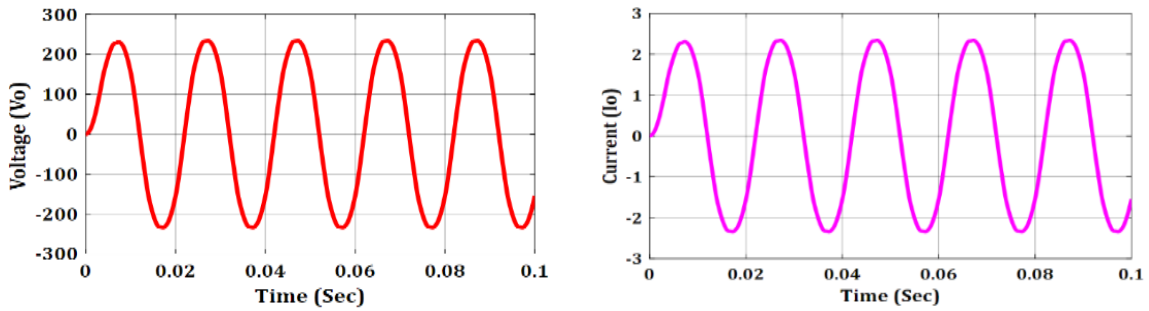
(a) (b)

Figure 11. Suggested HMLI with PODPWM technique using filter: (a) output voltage (V_0) and (b) output current (I_0)



(a) (b)

Figure 12. Suggested HMLI with APODPWM technique: (a) output voltage (V_0) and (b) output current (I_0)



(a) (b)

Figure 13. Suggested HMLI with APODPWM technique using filter: (a) output voltage (V_0) and (b) output current (I_0)

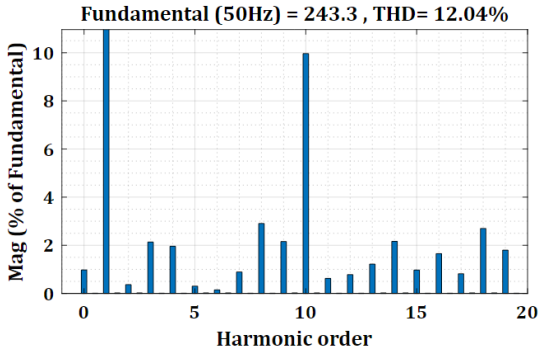


Figure 14. THD analysis of the proposed HMLI with PDPWM

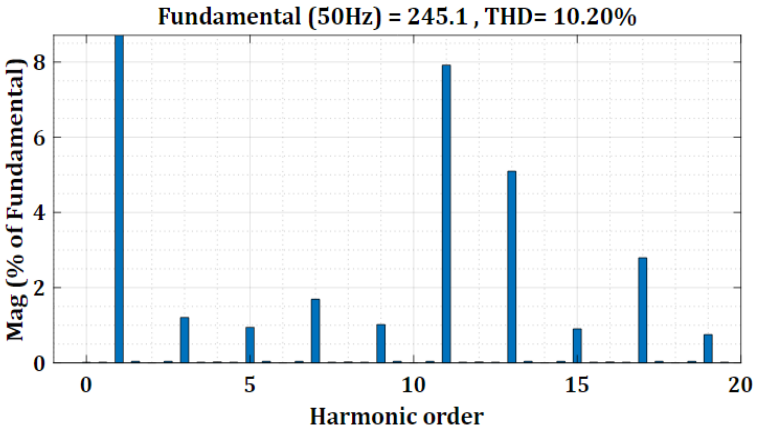


Figure 15. THD analysis of the proposed HMLI with PODPWM

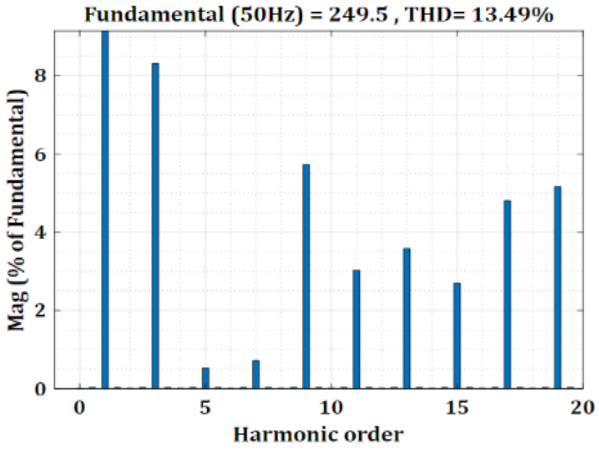


Figure 16. THD analysis of the proposed HMLI with APODPWM

Table 3. Comparison of THD analysis

THD %		
PD-PWM	POD-PWM	APOD-PWM
12.04	10.20	13.49

6. CONCLUSION

This study presents a novel hybrid multilevel inverter topology. In order to provide an output voltage, this nine-stage design requires two DC supplies, three diodes, and seven power switches. Numerous properties were present in the suggested hybrid system, including low voltage stress on the power switches and a high output voltage number of steps with fewer switches. The paper contains the conclusions for every formula that was utilized to regulate the system expansion's operation. Several current MLI topologies have been compared to the suggested topology in terms of switches, diodes, sources, levels, and cost factor. Additionally, this comparison brought the suggested system's robustness characteristics to light. Three distinct controlling strategies, the PDPWM, PODPWM, and APODPWM control schemes have been used to conduct the simulation test. Excellent results are obtained for three techniques, and THD obtained using FFT and meets the harmonics standard.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Gerri Ratnaiah	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
Ramya Ganesan		✓				✓		✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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BIOGRAPHIES OF AUTHORS

Gerri Ratnaiah received the B.Tech. and M.Tech. degrees in electrical and electronics engineering from Jawaharlal Nehru Technological University (JNTU) in 2005 and 2015, respectively. He is currently pursuing the Ph.D. degree in power electronics converters for electric vehicle applications at the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai, India. His research interests include step-up power electronics converters (DC/AC and DC/DC), multilevel inverter topologies and their control, and applications of power electronic converters in electric vehicles. He can be contacted at email: rg2879@srmist.edu.in.

Ramya Ganesan has done Bachelor of Engineering (B.E.) from Veltech Engineering College, Chennai, and Master of Engineering (M.E) from DMI College of Engineering, Chennai in the years 2009 and 2011, respectively. She obtained her Doctor of Philoshophy (Ph.D.) from Faculty of Engineering and Technology, SRM Institute of Science and Technology, Chennai, in the year of 2020. She has 13 years of teaching experience and currently working as an associate professor in the Department of EEE, Faculty of Engineering and Technology, SRM Institute of Science and Technology, Chennai, India. She has published 5 SCIE, 19 Scopus-indexed journal articles, and 7 patents. Three research scholars are pursuing Ph.D. degree under her supervision. She can be contacted at email: ramyag@srmist.edu.in.