International Journal of Applied Power Engineering (IJAPE)
Vol. 14, No. 3, September 2025, pp. 613~619
ISSN: 2252-8792, DOI: 10.11591/ijape.v14.i3.pp613-619

Minimizing the switching losses in the SiC MOSFET by using buried oxide

Ali Hlal Mutlaq[1], Sura Hamad Faraj[2], Majeed Rashid Zaidan[3], Ghanim Thiab Hasan[2], Ahmed Saad Names[2]
[1]Department of Medical Devices, Technical Technology, Al-Kitab University, Kirkuk, Iraq
[2]Department of Electrical Engineering, Al Shirqat Engineering College, Tikrit University, Tikrit, Iraq
[3]Department of Electrical Techniques, Baqubah Technical Institute, Middle Technical University, Baghdad, Iraq

Article Info

Article history:

Received Jul 23, 2024
Revised Apr 20, 2025
Accepted Jun 23, 2025

Keywords:

Buried oxide
Power loss
QGD
$R_{on,sp}$
SiC MOSFET

ABSTRACT

For optimizing the efficiency of the power switching devices, it is important to reduce the switching power losses. One method to minimize the switching power losses is to reduce the gate drain charge (Q_{GD}). In this paper, a 1.2 kV SiC MOSFET device with a buried oxide has been proposed to minimize Q_{GD}. The proposed design has been conducted by using the TCAD simulation program. The on-resistance ($R_{on,sp}$), QGD have been measured and analyzed based on the width and thickness of the buried oxide layer and compared with the measurement of traditional SiC MOSFET. The obtained results indicate that the Q_{GD} of 1.2 kV SiC MOSFET with buried oxide with WBO of 0.25 μm and TBO of 0.3 μm was reduced to about 31.3% which mean a minimize of power losses. The comparison results indicate that the proposed device with a buried oxide layer can be effectively used as an optimum solution for minimizing the power switching losses.

Corresponding Author:

Ghanim Thiab Hasan
Department of Electrical Engineering, Al Shirqat Engineering College, Tikrit University
Tikrit, Iraq
Email: ghanimdiab@yahoo.com

1. INTRODUCTION

With the increasing demand for high power electronic devices and the growing complexity of the power grid system and electric power applications such as automotive applications, high-voltage and high-current, SiC has been widely studied as a future power semiconductor that will replace Si IGBTs due to its wide power band gap and high thermal efficiency [1], [2]. Power semiconductors operating as switching devices need low gate charge in order to optimize energy efficiency, as most of the power dissipation takes place in switching processes [3]. In particular, it is desirable to have low gate drain charges because current and voltage are simultaneously applied on the device during the gate drain charge [4]. The term 'buried oxide' refers to a structure in which a portion of the ground plate area is filled with oxide by etching, which has the effect of lowering the capacitance between the gate and drain electrodes [5].

There are many studies on the performance investigation of SiC MOSFETs have been conducted [6]. Some of these studies concern the construction of SiC MOSFETs and some about their power losses, such as the parameters that can influence, in a certain way, the optimum function of a silicon carbide MOSFET as a driver [7]. Power losses, including parameters that can affect, in some way, the optimal function of the silicon carbide MOSFET as well as the driver, where, for example, Onasanya *et al.* [8] studied how the gate driver might be improved to obtain high energy density by using SiC MOSFETs. The power losses are a significant topic in large band gap semiconductor MOSFETs since minimizing the losses also

means more efficiency and thus the ability to reduce the heat sink size for example and hence the size of the product, but estimating the losses in SiC MOSFETs is very challenging, as the power losses are all linked to the parameters that in some way affect on each other. So, the optimization of a single parameter affecting the switching power losses in a SiC MOSFET can degrade the properties of another parameter [9].

Several newer SiC MOSFETs adopt an alternate gate oxide, i.e., buried oxide or a composite structure of a thin gate oxide with the buried oxide, to minimize the gate oxide field (and hence gate oxide reliability issues), while maintaining higher MOS channel carrier density and enabling very low gate charge characteristics [10]. In normal SiC MOSFETs with thick oxide under polycrystalline Si gate electrodes, high channel mobility occurs when the gate oxide capacitance per unit area increases and the gate charge amount is minimized. On the other hand, in a buried oxide SiC MOSFET, the junction capacitance reduces, the safe operating area improves, and the switching losses drop, since the gate oxide capacitance is halved and the current rating can double [11]-[14].

The MOSFET and the normally-off characteristics of the SiC power MOSFET can be improved by buried oxide layer (BO) or a breakdown pad (BP) structure [15]. The advantages of the BO structure are a simpler and lower-cost process, proven manufacturing capability, and low leakage [16]. The SiC buried oxide layer (SiC-BO) structure was first demonstrated on a 500 IEEE Electron Device Letters 0741-3106 c2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission [17]-[20]. High-voltage SiC power MOSFET with buried oxide for suppressed fringing fields has been investigated by Fu *et al.* [21]. The authors demonstrated that the BO-SiC MOSFET has enhanced gate-source voltage (V_{GS}), gate charge (QG), and switching speed by reducing the parasitic Miller effect and increasing the threshold voltage. However, for HV power MOSFETs, the fact that the current operating area (COA) of the SiC BO-MOSFET is smaller than that of the SiC MOSFET due to its higher total capacitance [22]-[25].

In this paper, we presented a 1.2 kV SiC MOSFET device with a buried oxide to enhance switching properties and electric field. The proposed design has been conducted by TCAD simulator. The proposed module was illustrated in Figure 1.

2. METHODOLOGY

In this paper, a 1.2 kV SiC MOSFET with a buried oxide has been designed by using a TCAD simulation program. The buried oxide has a width (W_{BO} = 2.5 µm) and thickness (T_{BO} = 0.3 µm). The gate charging properties, Q_{GD}, R_{on}, and HF-FOM of the proposed device will be measured, analyzed, and compared with the traditional device. Figure 1 illustrates the proposed device and its characteristics of the proposed device are illustrated in Table 1.

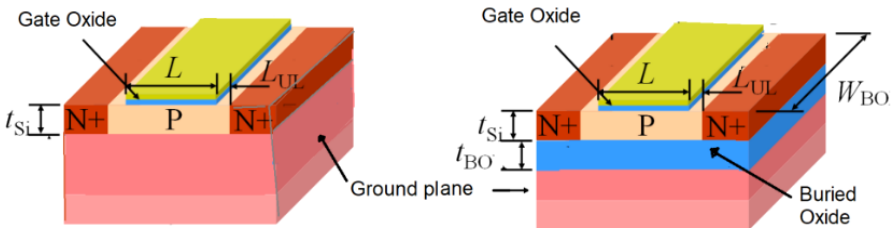


Figure 1. 1.2 kV SiC MOSFET: (a) traditional and (b) with buried oxide

Table 1. Characteristics of the 1.2 kV SiC MOSFET used in the simulation [25]

Parameters	Value
Buried oxide layer width	0.1, 0.15, 0.2, 0.25 (µm)
Buried oxide thickness T_{BO}	0.1, 0.2, 0.3(µm)
Channel dimension	0.45 (µm)
Shift thickness	12 (µm)
JFET width	1.6 (µm)

2.1. Power losses calculations in MOSFET gate

The loss of gate charge is the loss of power due to the charge of the MOSFET's gate and is dependent on the charge of the gate in the MOSFET [25]. It can be calculated using a simple formula, as (1).

$$P_G = Q_G \cdot V_{gs} \cdot f_{sw} \quad (1)$$

Where Q_g is the net charge through the gate when a MOSFET is on, V_{gs} is the voltage through the gate and the source, and f_{sw} is its switching frequency.

2.2. Power loss calculations in the MOSFET switching process

Whenever the MOSFET is switched on, a certain amount of energy goes into the process, the same goes when the device is switched off, these losses are called switching losses, when a device is switched on the I_d current begins to go up but its voltage V_{ds} does not drop until the current gets to its final value, once this is done, V_{ds} starts to drop until it gets to its terminal value which is very close to zero, and at that point, the MOSFET is at full operating mode. The dissipated power can be calculated as (2) [25].

$$P_{diss.ON} = \frac{1}{2} I_{d.ON\cdot} \cdot 2V_{ds} \cdot t_{ON} \quad (2)$$

Where $I_{d.on}$ represents the current that flows through the MOSFET's drain when it is switched on. V_{ds} is the voltage supplied to the drain, and T_{on} is time taken for this current to go up plus time for it to go down.

3. RESULTS AND DISCUSSION

3.1. Q_{GD}, Ron, and HF-FOM measurements and analysis

Figure 2 shows the Q_{GD} as a function of W_{BO} for a 1.2 kV SiC MOSFET device with a buried oxide for three different W_{BO}. From Figure 2, it can be seen that the Q_{GD} of the device with a traditional device has a higher value than that of the device with buried oxide. The value of Q_{GD} depends on the thickness of buried oxide layer. Moreover, the capacitance between the gate and drain electrodes decreases as the area occupied by the buried oxide increases. As the volume occupied by the buried oxide increases, the Q_{GD} decreases, while $R_{on,sp}$ increases due to current flow. Figure 3 shows the $R_{on,sp}$ as a function of W_{BO} for the proposed device.

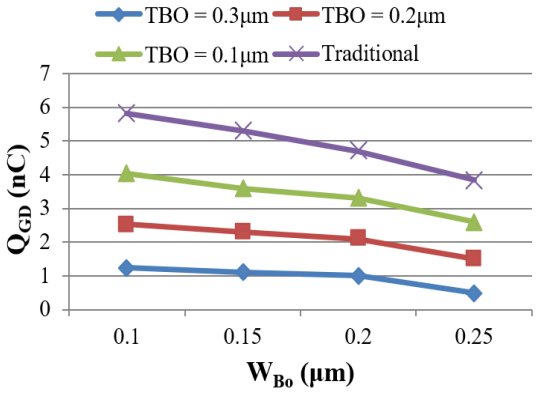


Figure 2. Q_{GD} values for the proposed device as a function of W_{BO}

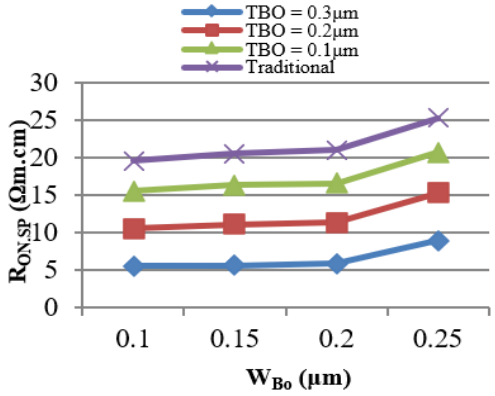


Figure 3. Comparison of the $R_{on,sp}$ values between the traditional and devices with buried oxide

From Figure 3, it can be seen that the device with buried oxide has larger $R_{on,sp}$ than those the traditional device. As W_{BO} and T_{BO} increase, the value of $R_{on,sp}$ increases. In order to compare the evaluate the performance of the two devices, we will compare the performance of the two devices by using HF-FOM, which is a parameter often used to evaluate the power efficiency of a particular device and is equal to the product of Q_{GD} and operating resistance. Figure 4 illustrates a comparison of HF-FOM in terms of W_{BO} between the traditional device and the device with buried structure. From Figure 4, it can be seen that the device with buried oxide has a lower HF-FOM value compared to device with traditional structure, which indicates that the proposed device is has better performance due to lower Q_{GD}.

Table 2 illustrates a comparison of the 1.2 kV SiC MOSFETs characteristics between the traditional device and the proposed device in case of (W_{BO} = 0.2 µm, T_{BO} = 0.1 µm). The values of $R_{on,sp}$, Q_{GD}, and Eox, for the device with buried oxide (W_{BO} = 0.25 and T_{BO} = 0.3 µm) are 4.8 Ω-cm^2, 1.70 N/cm^3, and 1.60 mV/cm^3, respectively. The buried oxide device displayed 47% decrease in Q_{GD}, a 32% decrease in Eox, max, and only a 6.0% improvement in $R_{on,sp}$, compared to the device with traditional structure. In addition, the total sum of the electric field of the device with buried oxide is less than the one with traditional structure. It is equal to 40.54 µJ and is 21% lower than the traditionally structured device. These values indicate that such buried oxide can significantly improve the switched characteristics of the 1.2 kV SiC MOSFET.

From Table 2, it can be seen that there is a decrease in QGD and HF-FOM by 32% and 27%, respectively, in the device with buried oxide compared to the traditional device, while $R_{on,sp}$ increases by only 7%. So, from the obtained results, it can be concluded that the SiC MOSFET performance can be improved by using the buried oxide layer, which results in some reduction in power switching losses. The graphical representation of the switching parameters is shown in Figure 5.

Table 2. Comparison between the 1.2 kV SiC MOSFET characteristics with buried oxide and traditional device in case of (W_{BO} = 0.25 µm), (T_{BO} = 0.3 µm)

Structure	Q_{GD} (nC)	$R_{on,sp}$ (mΩ-cm^2)	Etot. (µJ)	HF-FOM (pC-Ω)
Traditional	1.79	4.87	49.56	0.25
With buried oxide	1.25	5.18	40.54	0.17

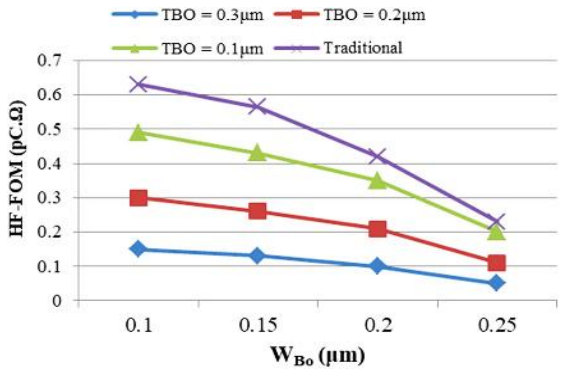
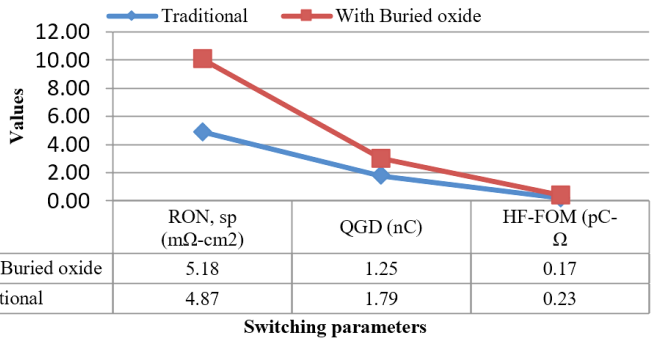


Figure 4. Comparison of the $R_{on,sp}$ values between the traditional and the proposed devices with buried oxide



	RON, sp (mΩ-cm2)	QGD (nC)	HF-FOM (pC-Ω
With Buried oxide	5.18	1.25	0.17
Traditional	4.87	1.79	0.23

Figure 5. Comparison representation of the switching parameters

4. CONCLUSION

In this paper, a 1.2 kV SiC MOSFET with a buried oxide has been designed which aims at improve the traditional SiC MOSFET performance. The proposed design has been conducted by using the TCAD simulation program. The $R_{on,sp}$ and Q_{GD}, for buried oxide devices have been measured and analyzed based on the width and thickness of the buried oxide and have been compared with the same parameters in traditional to achieve the optimum conditions with a buried oxide. The obtained results indicates that the buried oxide structure with wide (W_{BO} = 0.25 μm) and thickness (T_{BO} = 0.3 μm). The obtained results indicate that the on-operating specific resistance ($R_{on,sp)}$ increased slightly to 7%, but Q_{GD} and HF-FOM have been decreased to about 32.7% and 28% respectively. The comparison results show that the device with buried oxide is more efficient. So, the buried oxide structure can minimize the switching power losses, which results in some improvement in the performance of 1.2 kV SiC MOSFET efficiency.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Ali Hlal Mutlaq		✓	✓		✓				✓				✓	
Sura Hamad Faraj		✓				✓	✓		✓	✓		✓		
Majeed Rashid Zaidan	✓		✓	✓			✓			✓				✓
Ghanim Thiab Hasan	✓	✓		✓	✓	✓			✓	✓		✓	✓	✓
Ahmed Saad Names		✓				✓			✓			✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are openly available in Electronics Journal at https://doi.org/10.3390/electronics13050962, reference number [25].

REFERENCES

[1] G. Yang, X. Zhang, and A. J. Moshayedi, "Implementation of the simple hyperchaotic memristor circuit with attractor evolution and large-scale parameter permission," *Entropy*, vol. 25, no. 2, 2023, doi: 10.3390/e25020203.
[2] Q. Lai, Z. Wan, L. K. Kengne, P. D. Kamdem Kuate, and C. Chen, "Two-memristor-based chaotic system with infinite coexisting attractors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 6, pp. 2197–2201, 2021, doi: 10.1109/TCSII.2020.3044096.
[3] D. Peters *et al*., "Performance and ruggedness of 1200V SiC — Trench — MOSFET," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, IEEE, May 2017, pp. 239–242, doi: 10.23919/ISPSD.2017.7988904.
[4] Y. Wang, K. Tian, Y. Hao, C. H. Yu, and Y. J. Liu, "4H-SiC step trench gate power metal-oxide-semiconductor field-effect transistor," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 633–635, 2016, doi: 10.1109/LED.2016.2542183.
[5] H. Yoon and O. Seok, "Design of a 1.2 kV SiC MOSFET with buried oxide for improving switching characteristics," *Electronics (Switzerland)*, vol. 13, no. 5, 2024, doi: 10.3390/electronics13050962.
[6] H. Y. Xu, Y. Wang, M. T. Bao, and F. Cao, "Low switching loss split-gate 4H-SiC MOSFET with integrated heterojunction diode," *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 554–561, 2022, doi: 10.1109/JEDS.2022.3192420.
[7] G. Dai, W. Xie, X. Du, M. Han, T. Ni, and D. Wu, "Memristor-based D-flip-flop design and application in built-in self-test," *Electronics (Switzerland)*, vol. 12, no. 14, 2023, doi: 10.3390/electronics12143019.
[8] B. O. Onasanya, X. Dai, Y. Feng, and W. Zhang, "Fuzzy sandwich control of some nonlinear systems with a number of stochastically occurring impulses," *13th International Conference on Information Science and Technology, ICIST 2023 - Proceedings*, pp. 142–150, 2023, doi: 10.1109/ICIST59754.2023.10367063.
[9] D. Kim, N. Yun, S. Y. Jang, A. J. Morgan, and W. Sung, "An inclusive structural analysis on the design of 1.2kV 4H-SiC planar MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 804–812, 2021, doi: 10.1109/JEDS.2021.3109605.

[10] Y. Yu, Z. Cheng, Y. Hu, R. Lv, and S. Hu, "A novel asymmetric trench SiC metal–oxide–semiconductor field-effect transistor with a Poly-Si/SiC heterojunction diode for optimizing reverse conduction performance," *Micromachines*, vol. 15, no. 4, 2024, doi: 10.3390/mi15040461.
[11] G. Laarem, "A new 4-D hyper chaotic system generated from the 3-D Rösslor chaotic system, dynamical analysis, chaos stabilization via an optimized linear feedback control, it's fractional order model and chaos synchronization using optimized fractional order sliding mode control," *Chaos, Solitons and Fractals*, vol. 152, 2021, doi: 10.1016/j.chaos.2021.111437.
[12] G. T. Hasan, K. J. Ali, and A. H. Mutlaq, "Design of current controlled instrumental amplifier by using complementary metallic oxide semiconductor technology," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 29, no. 2, pp. 652–657, 2023, doi: 10.11591/ijeecs.v29.i2.pp652-657.
[13] Y. Yu *et al.*, "A novel asymmetric trench SiC MOSFET with an integrated JFET for improved reverse conduction performance," *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1546–1552, 2024, doi: 10.1109/TED.2023.3333285.
[14] M. R. Zaidan and S. I. Toos, "Optimal location of static var compensator to regulate voltage in power system," *IETE Journal of Research*, vol. 69, no. 4, pp. 2177–2185, May 2023, doi: 10.1080/03772063.2021.1886877.
[15] K. Han, B. J. Baliga, and W. Sung, "Accumulation channel vs. inversion channel 1.2 kV rated 4H-SiC buffered-gate (BG) MOSFETs: Analysis and experimental results," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, IEEE, May 2018, pp. 371–374, doi: 10.1109/ISPSD.2018.8393680.
[16] K. Han, A. Kanale, B. J. Baliga, and S. Bhattacharya, "Static, dynamic, and short-circuit performance of 1.2 kV 4H-SiC MOSFETs with various channel lengths," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, IEEE, Oct. 2019, pp. 47–52, doi: 10.1109/WiPDA46397.2019.8998803.
[17] U. Karki, N. S. Gonzalez-Santini, and F. Z. Peng, "Effect of gate-oxide degradation on electrical parameters of silicon carbide MOSFETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 6, pp. 2544–2552, 2020, doi: 10.1109/TED.2020.2990128.
[18] R. P. Naik and S. Sachin, "Design of low power CMOS circuits using multi threshold voltage CMOS technology," *International Journal for Research in Engineering Application & Management (IJREAM)*, vol. 3, no. 6, 2017.
[19] G. T. Hasan, A. H. Mutlaq, K. J. Ali, and M. A. Saad, "Modeling of magnetic sensitivity of the metal-oxide-semiconductor field-effect transistor with double gates," *International Journal of Electrical and Computer Engineering*, vol. 13, no. 3, pp. 2632–2639, 2023, doi: 10.11591/ijece.v13i3.pp2632-2639.
[20] H. Wang, B. Wang, B. Hu, L. Kong, F. Udrea, and T. Long, "4H-SiC trench gate lateral MOSFET with deep-shallow source trench for improved RESURF dose window and reduced oxide field," in *2022 IEEE Workshop on Wide Bandgap Power Devices and Applications in Europe (WiPDA Europe)*, IEEE, Sep. 2022, pp. 1–4, doi: 10.1109/WiPDAEurope55971.2022.9936422.
[21] H. Fu *et al.*, "Quasisaturation effect and optimization for 4H-SiC trench MOSFET with P+ shielding region," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4550–4556, 2021, doi: 10.1109/TED.2021.3096919.
[22] H. Xu, Y. Yang, J. Tan, H. Zhu, Q. Q. Sun, and D. W. Zhang, "Carrier stored trench-gate bipolar transistor with stepped split trench-gate structure," *IEEE Transactions on Electron Devices*, vol. 69, no. 10, pp. 5450–5455, 2022, doi: 10.1109/TED.2022.3200645.
[23] C. Xu, C. Wang, J. Jiang, J. Sun, and H. Lin, "Memristive circuit implementation of context-dependent emotional learning network and its application in multitask," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 9, pp. 3052–3065, 2022, doi: 10.1109/TCAD.2021.3116463.
[24] H. Lin, C. Wang, C. Xu, X. Zhang, and H. H. C. Iu, "A memristive synapse control method to generate diversified multistructure chaotic attractors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 42, no. 3, pp. 942–955, 2023, doi: 10.1109/TCAD.2022.3186516.
[25] W. Cui, J. Guo, H. Xu, and D. W. Zhang, "A high-density 4H-SiC MOSFET based on a buried field limiting ring with low Q_{gd} and R_{on}," *Micromachines*, vol. 16, no. 4, p. 447, Apr. 2025, doi: 10.3390/mi16040447.

BIOGRAPHIES OF AUTHORS

Ali Hlal Mutlaq is a lecturer at the Medical Instrumentation Technical Engineering Department, Engineering Technical College, Al-Kitab University, Kirkuk, Iraq, where he has been a faculty member since 2005. He graduated with a first-class honours B.Eng. degree in Electronic Engineering from Belgrade University, Serbia, in 1982, and M.Sc. in Electrical Engineering from Belgrade University, Serbia, in 1984. His research interests are primarily in the areas of wireless communications and networks, as well as in the area of electrical engineering. He can be contacted at email: ali.h.mutlaq@uoalkitab.edu.iq.

Sura Hamad Faraj is an Associate Professor at the Department of Electrical Engineering, Al-Shirqat Engineering College, Tikrit University, Iraq. Her research interests are primarily in the area of electrical and electronic engineering. She can be contacted at email: sura.faraj@tu.edu.iq.

Majeed Rashid Zaidan received a B.Sc. and M.Sc. degree in Electrical Engineering from the University of Technology, Baghdad, Iraq, in 1986 and 2003, respectively. Currently, he is a lecturer at Baqubah Technical Institute, Middle Technical University. He has focused his research on FACTS devices, power systems, and electrical machines. He can be contacted at email: majeedrzn@mtu.edu.iq.

Ghanim Thiab Hasan is an Associate Professor at the Department of Electrical Engineering, Al-Shirqat Engineering College, Tikrit University, Iraq, where he has been a faculty member since 2006. He graduated with a first-class honours B.Eng. degree in Electrical and Electronic Engineering from Belgrade University, Serbia, in 1984, and M.Sc. in Electrical Engineering from Belgrade University, Serbia, in 1986. His research interests are primarily in the area of electrical and electronic engineering. He can be contacted at email: ganimdiab@yahoo.com.

Ahmed Saad Names is an associate lecturer at the Department of Electrical Engineering, Al Shirqat Engineering College, Tikrit University, Iraq, where he has been a faculty member since 2023. He graduated in Electrical Engineering from Tikrit University, in 2011, and M.Sc. in Electronic and Communication Engineering from Baghdad University in 2016. His research interests are primarily in the areas of electrical, communication, and electronic engineering. He can be contacted at email: ahmed.alnames@tu.edu.iq.