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Design of a binary weighted multilevel voltage source inverter for renewable energy purposes

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ABSTRACT

The flexibility and linearity of renewable energy generation techniques motivate the efforts to find high-performance circuitries capable of integrating the generation stations of renewable energy with the utility grid. As a result of its potential for power modules exploited in new generations of semiconductor switching devices, the voltage source inverter (VSI) has become widespread in the applications of renewable energy systems. In this paper, a new configuration of multilevel VSI is introduced. It is constructed of a unidirectional voltage supply having 15-nonzero levels and feeding a single-phase VSI equipped with an extra-freewheeling circuit. The output voltage of this configuration has 31 different voltage levels following a sinusoidal path. The unidirectional voltage supply is built of eight solid-state switching devices and four binary weighted DC voltage sources, which are realized by using appropriate solar panels. The simulation results of the introduced configuration have revealed almost sinusoidal output voltage and current for both inductive and resistive appliances. The number of employed switching devices is largely reduced compared to a conventional multilevel VSI. No harmonic reduction circuit or traditional pulse width modulation technique is employed in the current design. This system is designed and tested on PSpice.

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1. INTRODUCTION

Over the years, inverter technologies have advanced significantly. Multilevel approaches have seen notable attempts to approach sinusoidal waveforms for output voltages or currents. A three-level voltage source inverter (VSI) and star-connected multiphase stator windings with segregated neutral points were used in [1] to provide two distinct multiphase supplies. Nevertheless, a multilayer VSI was controlled using a method called phase disposition switching frequency optimum pulse width modulation (PD-SFO PWM) to generate three-phase, five-level AC voltages [2]. To provide a multilayer output current [3] using fewer switching devices, a multilevel current source inverter (CSI) was controlled via a multicarrier PWM switching approach. Depending on how the power cells (modules) in a cascaded structure are connected in series, multilevel converters using individual low-voltage components can work at medium or even high voltages [4]. For n-level voltage source inverters, a time domain study was utilized to determine a direct correlation between sampling, carrier, and fundamental frequencies at different modulation indices using sinusoidal pulse width modulated (SPWM) [5]. While the inverter's rating needs to be three times or more than the capacity of loads with high starting currents, it should be 25–30% greater than the appliances with

low starting currents [6]. Due to their increasing viability as a technology for numerous applications, such as drive systems and conversion in renewable energy, multilevel inverters have attracted a lot of interest from both academia and industry [7], [8]. Many studies were conducted to develop new multilevel inverter topologies that would take into account the advancements in switching devices, which are typically used in the construction of inverters, the switching frequencies used in the inverter controlling circuits, which cause electromagnetic interference, and minimized switching losses that increase overall efficiency to improve the inverter voltage profile and efficiency [9]–[13].

The design of static synchronous compensators, or STATCOMs, is often based on the design principles of the inverter. In order to exchange real power or reactive power for load current and voltage balancing with little harmonic association, a STATCOM can be constructed with a single H-bridge or with cascaded H-bridges and managed using a variety of techniques [14]–[16]. To meet the voltage level requirements in power transmission systems, the performance of high-voltage DC voltage source converters was examined in [17]. Conventional 2-level inverters have limitations when operating at high sampling frequencies due to high switching losses. To address this issue, multilevel inverters with low switching frequencies and reduced total harmonic distortion are used, which removes the need for additional filters and even large transformers[18]–[23]. A study compared Icosθ and enhanced synchronous reference frame second-order generalized integrator frequency-locked loop (SRF SOGI-FLL) controllers, focusing on power quality, DC-link voltage regulation, and harmonic reduction capabilities in a distribution STATCOM [24]. In contrast, cascaded H-bridges multilevel inverters based on stacked T-shape voltage generation modules were introduced in [25] to achieve reduced current conducting switches devices in the load paths. Four H-bridges built on the basis of a voltage source inverter were cascaded in [26] to create a high voltage single-phase STATCOM equipped with an adaptive current controller and a balancing method for the voltages of its DC capacitor to meet the requirements of load current balancing in high voltage AC networks. Two-stage DC-DC converters were discussed in [27] as workable solutions to these problems because the integration of multi-terminals hybrid high voltage DC grids connecting line-commutated converters VSC-based networks counters several challenges like DC fault isolations and achieving high-speed power reversal without any interruption. The issue of power point of maximum tracking in solar systems in power-producing stations was addressed by the proposal of a dependable voltage source inverter powered by a specific PWM approach [28]. Detailed reviews were introduced in [29], [30] concerning the developments of multilevel converters and multilevel technologies. To approach sinusoidal current waveforms for both resistive and inductive loads, a multilevel voltage source inverter with almost sinusoidal output voltage and current is configured in this paper by using a unidirectional voltage supply with 15 non-zero levels to feed a single-phase voltage source inverter.

2. THE PROPOSED MULTILEVEL VOLTAGE SOURCE INVERTER

The proposed multilevel VSI is shown in Figure 1. It is a VSI powered by a single-sided multilevel supply. The multilevel supply's output voltage v_{ML} is unidirectional and has a sinusoidal envelope with each half cycle. The load output voltage v_L will have a sinusoidal envelope and be bidirectional based on the VSI operation as shown in Figure 1. The configuration in Figure 1 is proposed as a photovoltaic power plant unit.

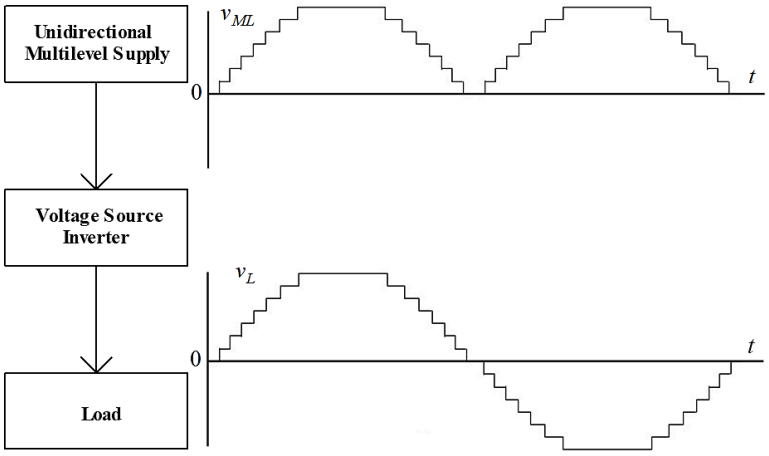

Figure 1. The proposed multilevel VSI

2.1. The unidirectional multilevel supply

Figure 2 depicts the multilevel unidirectional supply. In this figure, a 4-bit analog to digital converter (4-bit ADC) receives the full-wave rectified output voltage of a sinusoidal AC source with an amplitude of 10 V and a frequency *f* of 60 Hz as an analog input V_{in}. The conversion of this analog input to digital is initiated by using the output voltage of a 33 kHz square wave generator. The digital output of the 8-bit ADC is D_3, D_2, D_1, and D_0, where D_0 represents the least significant digit and D_3 stands for the most significant digit. If the 8-bit ADC is designed such that it has a maximum analog input V_{in} of 10 V and a minimum input of zero value, then the ADC will target sixteen possible voltage levels starting from 0 V level and ending with 9.375 V level. The difference between two adjacent voltage levels is 0.625 V. When V_{in} is greater than zero and less than 0.625 V, then the ADC digital output is 0000, whereas its output is 1111, when V_{in} is in the range of 9.375 V to 10 V. This is true for all successive voltage levels; for instance, if V_{in} is greater than 0.625 V and less than 1.25 V, then the ADC output will be 0001, or in other words only D_0 is logic 1. The ADC output digits D_0, D_1, D_2, and D_3 are exploited to control the solid state switches S_1, S_2, S_3, and S_4, respectively, whereas their digital compliments D_0*, D_1*, D_2*, and D_3*, are used to control, the switches S_1*, S_2*, S_3*, and S_4*, respectively. The DC voltage sources V_B, $2V_B$, $4V_B$, and $8V_B$ are connected in series to the switches S_1, S_2, S_3, and S_4, respectively. The voltage V_B is the base voltage for this system. The unidirectional output voltage v_{ML} can be given by (1).

$$v_{ML} = V_B\,(D_0 + 2D_1 + 4D_2 + 8D_3) \tag{1}$$

Figure 3 shows the status of the ADC most significant digits. This figure shows the variation of the output digits D_0, D_1, D_2, and D_3 with V_{in}. Here, V_{in} represents the ADC analog input, which is a full-wave rectified sinusoidal waveform.

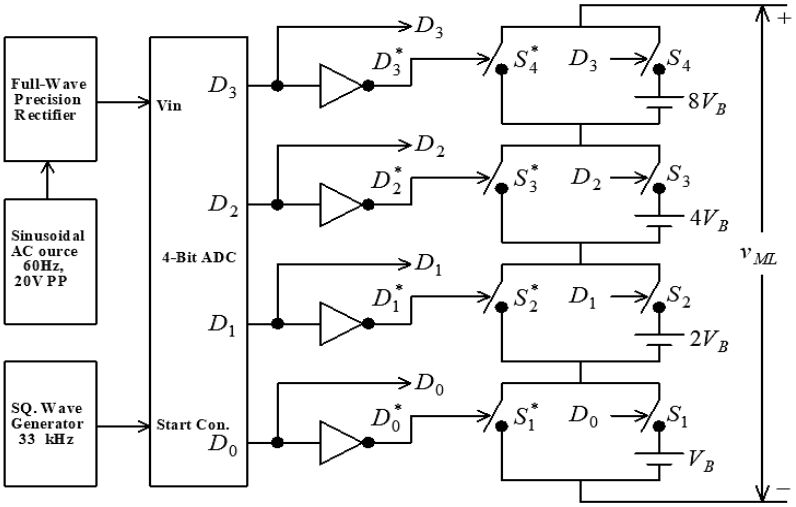

Figure 2. The proposed 15-nonzero level unidirectional voltage supply

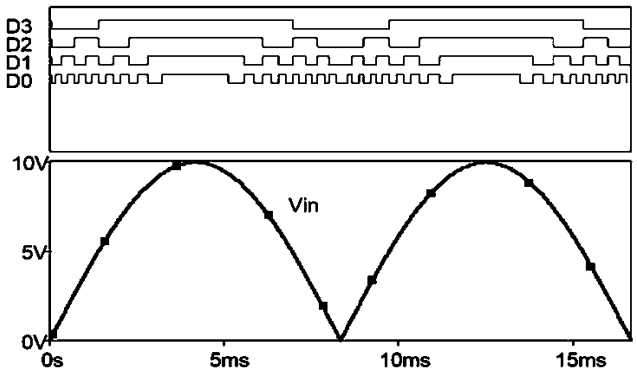

Figure 3. The variation of the ADC output digits D_0, D_1, D_2, and D_3 with its analog input V_{in}

Table 1 shows the switching mechanism of the proposed multilevel unidirectional voltage supply. The multilevel output voltage v_{ML} depends on this mechanism. The stepping waveform of v_{ML} follows a sinusoidal envelope.

Table 1. The switching mechanism of the 15-nonzero levels supply

D_3	D_2	D_1	D_0	S_4	S_3	S_2	S_1	S_4*	S_3*	S_2*	S_1*	v_{ML}
0	0	0	0	OFF	OFF	OFF	OFF	ON	ON	ON	ON	0
0	0	0	1	OFF	OFF	OFF	ON	ON	ON	ON	OFF	V_B
0	0	1	0	OFF	OFF	ON	OFF	ON	ON	OFF	ON	$2V_B$
0	0	1	1	OFF	OFF	ON	ON	ON	ON	OFF	OFF	$3V_B$
0	1	0	0	OFF	ON	OFF	OFF	ON	OFF	ON	ON	$4V_B$
0	1	0	1	OFF	ON	OFF	ON	ON	OFF	ON	OFF	$5V_B$
0	1	1	0	OFF	ON	ON	OFF	ON	OFF	OFF	ON	$6V_B$
0	1	1	1	OFF	ON	ON	ON	ON	OFF	OFF	OFF	$7V_B$
1	0	0	0	ON	OFF	OFF	OFF	OFF	ON	ON	ON	$8V_B$
1	0	0	1	ON	OFF	OFF	ON	OFF	ON	ON	OFF	$9V_B$
1	0	1	0	ON	OFF	ON	OFF	OFF	ON	OFF	ON	$10V_B$
1	0	1	1	ON	OFF	ON	ON	OFF	ON	OFF	OFF	$11V_B$
1	1	0	0	ON	ON	OFF	OFF	OFF	OFF	ON	ON	$12V_B$
1	1	0	1	ON	ON	OFF	ON	OFF	OFF	ON	OFF	$13V_B$
1	1	1	0	ON	ON	ON	OFF	OFF	OFF	OFF	ON	$14V_B$
1	1	1	1	ON	ON	ON	ON	OFF	OFF	OFF	OFF	$15V_B$

2.2. The voltage source inverter

To calculate the fundamental component of the load voltage v_L simply, a VSI driven by seven nonzero-level unidirectional supply is considered here. This voltage is shown in Figure 4. In this figure, $V_m sin\varphi$ stands for the sinusoidal envelope of v_L, where V_m is its amplitude and φ is equal to $\omega t = 2\pi ft$.

It should be noted that there are eight voltage levels in total (including the zero level) and that the voltage step V_B is $V_m/8$. If it is required to construct a multilevel voltage with N nonzero levels, then the voltage step V_B will be $V_m/(N+1)$. Considering the shaded rectangle in Figure 4, it can be written as (2).

$$iV_B = V_m \, sin\varphi_i \tag{2}$$

Where, i is a number varying from 0 to N and referring to a certain voltage level. Using the Fourier series, the fundamental component A_1 corresponding to the load voltage v_L can be calculated as (3).

$$A_1 = \frac{1}{\pi}\int_0^{2\pi} v_L \, sin\varphi d\varphi = \sum_{i=0}^{i=N}\left(\frac{4}{\pi}\right)\int_{\varphi_i}^{\varphi_{i+1}} iV_B \, sin\varphi d\varphi = \sum_{i=0}^{i=N}\left(\frac{4iV_B}{\pi}\right)(cos\varphi_i - cos\varphi_{i+1}) \tag{3}$$

According to (2), φ_i and φ_{i+1} can be equated to (4) and (5).

$$\varphi_i = sin^{-1}\left(\frac{iV_B}{V_m}\right) = sin^{-1}\left(\frac{i}{N+1}\right) \tag{4}$$

$$\varphi_{i+1} = sin^{-1}\left(\frac{i+1}{N+1}\right) \tag{5}$$

Substituting (4) and (5) into (3) and simplifying gives as (6).

$$A_1 = \sum_{i=0}^{i=N}\left(\frac{4iV_B}{\pi}\right)\left(\sqrt{1-\left(\frac{i}{N+1}\right)^2} - \sqrt{1-\left(\frac{i+1}{N+1}\right)^2}\right) \tag{6}$$

The ratio (A_1/V_m) is very important. It denotes how far the fundamental component of the load voltage is closer to its envelope. Dividing (6) by V_m and taking into account that $V_m = (N+1)V_B$ gives as (7).

$$\frac{A_1}{V_m} = \sum_{i=0}^{i=N}\left(\frac{4i}{\pi(N+1)}\right)\left(\sqrt{1-\left(\frac{i}{N+1}\right)^2} - \sqrt{1-\left(\frac{i+1}{N+1}\right)^2}\right) \tag{7}$$

If the base voltage V_B is 12 V, then for 15 nonzero levels (N=15) configuration, the amplitude V_m of the sinusoidal envelope of v_L will be $(N+1)$ V_B = 192 V. This value of V_m is suitable for a 60 Hz, 127 V system. Taking V_m = 192 V and conditioning the value of V_B according to the value of N in (5) and (6) result in the calculated parameters listed in Table 2. Going over this table denotes that the configuration with 15 nonzero levels is very close to the voltage amplitude (179.6 V) of the 60 Hz, 127 V system.

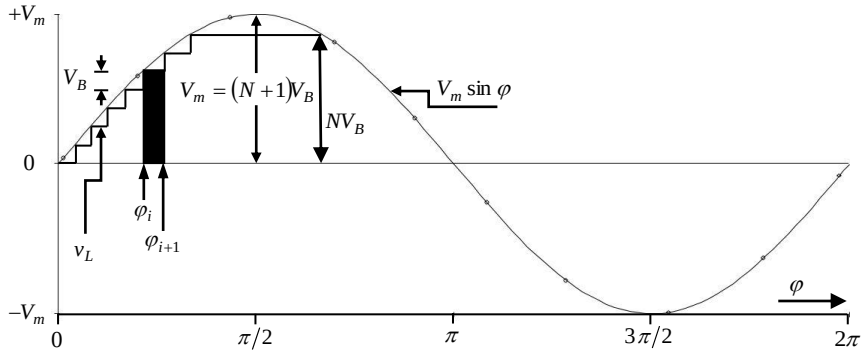

Figure 4. The load output voltage with seven nonzero levels for each half cycle

Table 2. The fundamental of v_L with nonzero levels

N	A_1 (Volts)	V_B (Volts)	V_m (Volts)	A_1/V_m
3	152.0064	48	192	0.7917
7	173.6448	24	192	0.9044
15	183.3216	12	192	0.9548
31	187.872	6	192	0.9785

2.3. The circuit design of the proposed system

The circuit of the proposed system is shown in Figure 5. It includes the unidirectional 15-nonzero levels voltage supply feeding a modified voltage source inverter in addition to the controlling and driving circuits. Here, the 4-bit ADC is realized through an 8-bit ADC. The output digits D_3, D_2, D_1, and D_0 in the 4-bit ADC are replaced by the most significant four digits DB_7, DB_6, DB_5, and DB_4 in the 8-bit ADC, respectively.

In both unidirectional voltage supply and modified voltage source inverter, the insulated gate bipolar transistor (IGPT) CM100DY-12E is used, which is equipped with a fast recovery freewheeling diode. It is characterized by: maximum collector current (I_{Cmax}) = 100 A, maximum collector-to-emitter voltage (V_{CEmax}) = 600 V, and maximum power dissipation (P_{DM}) = 400 W. The smoothing circuit is designed such it can damp down the voltage spikes at the output of the unidirectional voltage supply and it does not affect its output current. The freewheeling circuit operates during inductive loads, wherein it offers an additional recovery path to load reactive components. The DC voltage sources V_B, $2V_B$, $4V_B$, and $8V_B$ can be realized by solar cell panels with their corresponding suitable charge controllers. If V_B is chosen as 12 V, then the voltage sources V_B, $2V_B$, $4V_B$, and $8V_B$ will be 12 V, 24 V, 48 V, and 96 V, respectively. According to this base voltage, the sinusoidal envelope of v_L will have an amplitude V_m of 192 V and a fundamental component of 183.3216 V, which is suitable for a 127 V, 50 Hz system. For instance, the 12 V source can be realized by connecting four 18 V, 300 W solar panels in parallel and equipping them with a 12 V charge controller. The 18 V, 300 W solar panel is characterized by: maximum power (p_{max}) = 300 W, open circuit voltage (VOC) = 20 V, maximum power voltage (V_{mpp}) = 18 V, and maximum power current (I_{mpp}) = 15 A. The 24 V source can be represented by four 34.6 V, 600 W solar panels connected in parallel and regulated with a 24 V charge controller. The 34.6 V, 600 W solar panel is characterized by: p_{max} = 600 W, VOC = 41.7 V, V_{mpp} = 34.6 V, and I_{mpp} = 17.34 A. Two configurations of 24 V voltage source connected in series and equipped with 48 V charge controller is a good realization of the 48 V DC voltage source. The total power of the 48 V configuration is 4.8 kW. The 96 V DC voltage source can be represented by two configurations of 48 V voltage source connected in series and equipped with a 96 V charge controller. The total power of this configuration is 9.6 kW. The maximum possible power of these configurations of solar panels is 18 kW. The capacitor C_2 in the extra freewheeling circuit is very important in the determination of the inductive current rating. Since this system is designed to drive 60 Hz, 127 V loads, a 60 Hz, 20 V peak-to-peak sinusoidal voltage source is used to drive both the VSI and 8-bit ADC (after full-wave rectification as its analog input V_{in}). To start analog to digital conversion, a 33.33 kHz signal source is used. The diodes D_{S1}*, D_{S2}*, D_{S3}*, and D_{S4}*, which are connected in series with S_1*, S_2*, S_3*, and S_4*, respectively, are used to prevent a possible short circuit upon the voltage sources V_B, $2V_B$, $4V_B$, and $8V_B$. All circuitries in the above design are obvious, except the IGPT driving circuit which appears as a PSpice part shown in Figure 6. PSpice is used in this work because it is very close in performance to real hardware.

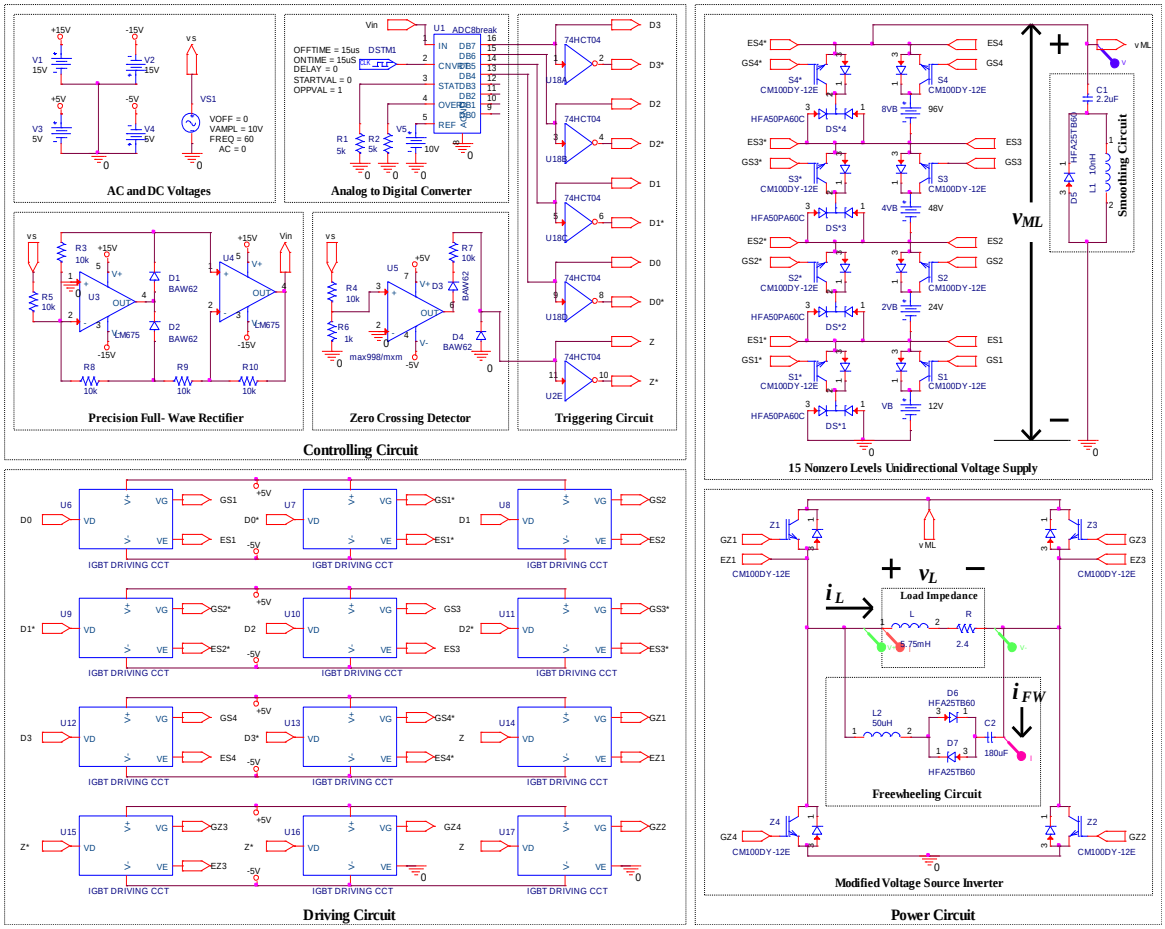

Figure 5. The PSpice circuit design of the proposed system

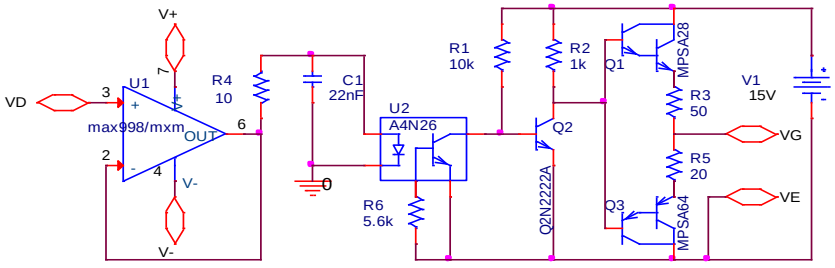

Figure 6. The IGPT driving circuit

3. RESULTS AND DISCUSSION

The performance of the proposed multilevel configuration was investigated through a series of PSpice tests carried out on the circuit shown in Figure 5. The targeted parameters are the load voltage v_L, load current i_L, multilevel voltage v_{ML}, the freewheeling current i_{FW}, the frequency spectrum $F(v_L)$ of load voltage v_L, and frequency spectrum $E(i_L)$ of load current i_L. Figure 7 shows the generated multilevel voltage v_{ML} during resistive loads. Figures 7(a) and 7(b) show the multilevel voltage v_{ML} and the freewheeling current i_{FW}, respectively. The current i_{FW} exhibits almost negligible levels and v_{ML} has 15 equidistant nonzero levels.

The system was tested at different current ratings. Figure 8 concerns a 30 A resistive load. Figure 8(a) shows the load voltage v_L and load current i_L during a resistive load of 30 A (peak value), whereas, Figure 8(b) shows their frequency spectrums $F(v_L)$ and $F(i_L)$, respectively. Figures 8(c) and 8(d) show v_{ML} and i_{FW}, respectively. During resistive loads, the freewheeling circuit is unnecessary and the capacitor C_2 is set to 5 µF.

Figure 9 shows the performance during a resistive load of 60 A (peak value). Figure 9(a) shows v_L and i_L, whereas Figure 9(b) shows their frequency spectrums. Figures 9(c) and 9(d) show v_{ML} and i_{FW}, respectively.

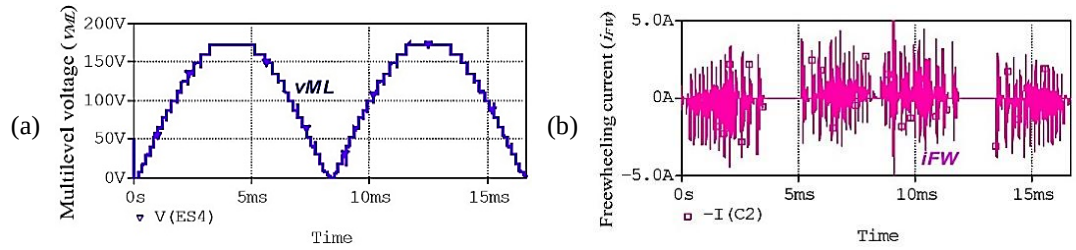

Figure 7. The multilevel voltage v_{ML} and freewheeling current i_{FW} during resistive loads: (a) v_{ML} and (b) i_{FW}

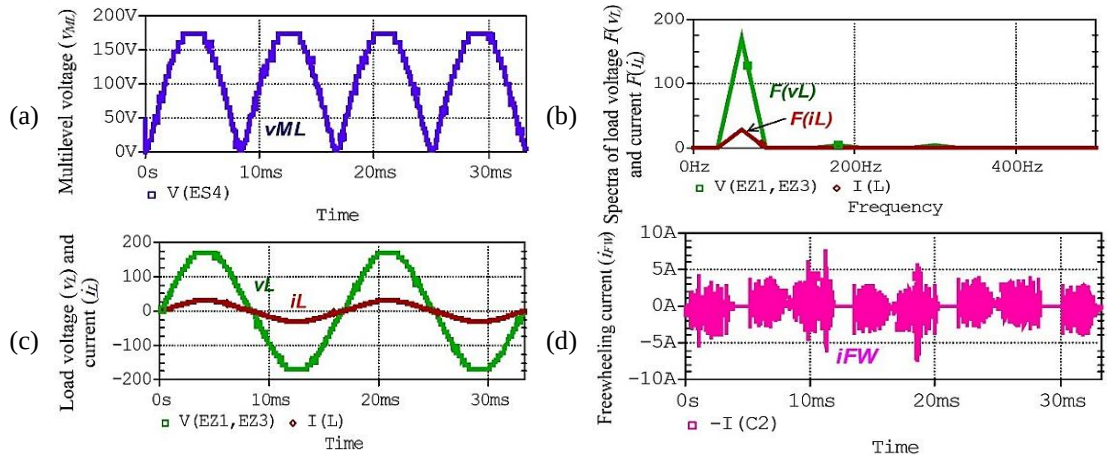

Figure 8. System performance during a resistive load of 30 A (peak value): (a) v_L and i_L, (b) $F(v_L)$ and $F(i_L)$, (c) v_{ML}, and (d) i_{FW}

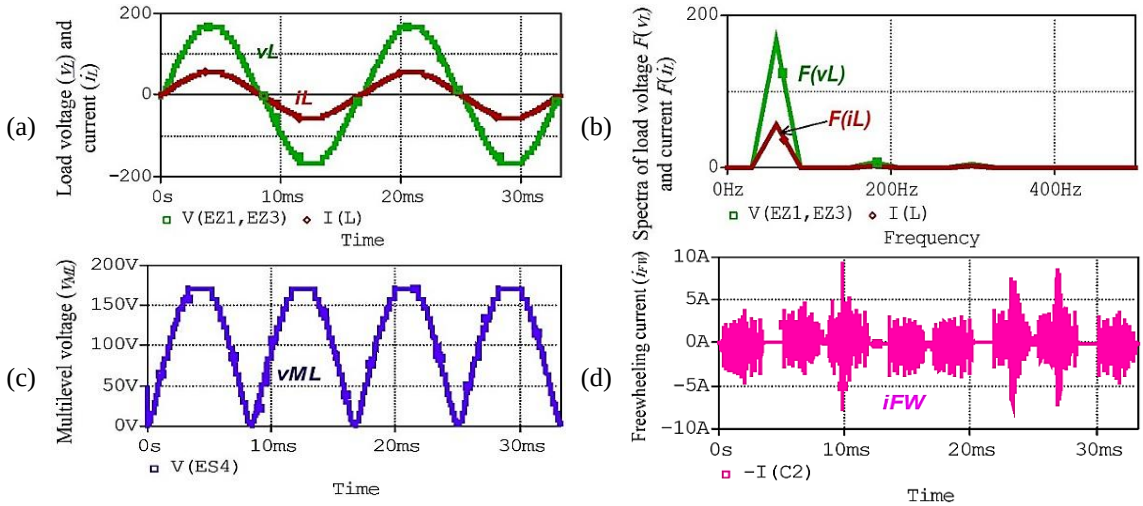

Figure 9. System performance during a resistive load of 60 A (peak value): (a) v_L and i_L, (b) $F(v_L)$ and $F(i_L)$, (c) v_{ML}, and (d) i_{FW}

During inductive loads, the freewheeling circuit is necessary. Thus, the capacitor C_2 is set to 180 µF. Figure 10 shows the system response to an inductive current demand of 30 A (peak value) and 0.8 power factor. Figure 10(a) shows v_L and i_L, whilst Figure 10(b) shows their corresponding spectrums. Figures 10(c) and 10(d) correspond to v_{ML} and i_{FW}, respectively.

Figure 11 shows the system response to an inductive current demand of 60 A (peak value) at 0.8 power factor. Going over Figures 8-11, it can be concluded that the proposed system has an abrupt response to the appliance current. Both v_L and i_L have negligible harmonic contents. This is verified by their corresponding frequency spectrums $F(v_L)$ and $F(i_L)$. This system is suitable for fast varying loads and can also satisfy the demand of loads with high starting currents. The system is flexible in increasing its rating.

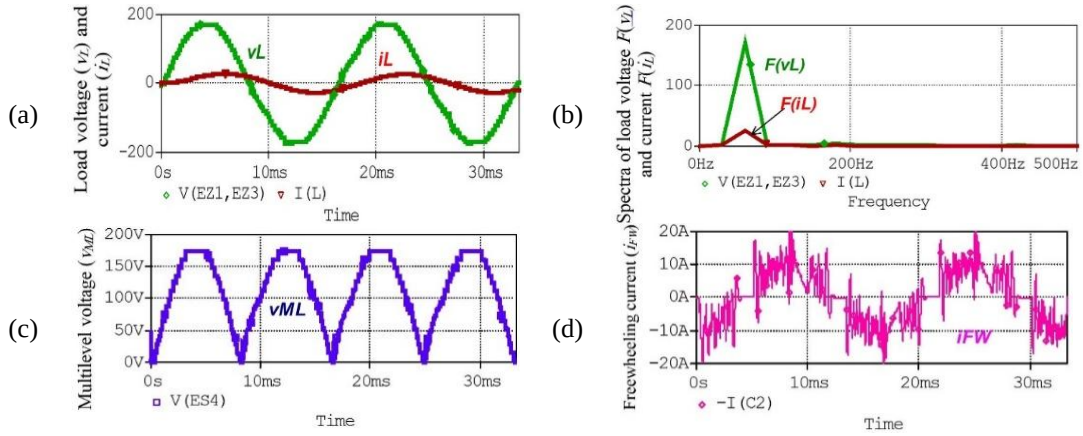

Figure 10. System performance during an inductive load of 30 A (peak value) and 0.8 power factor: (a) v_L and i_L, (b) $F(v_L)$ and $F(i_L)$, (c) v_{ML}, and (d) i_{FW}

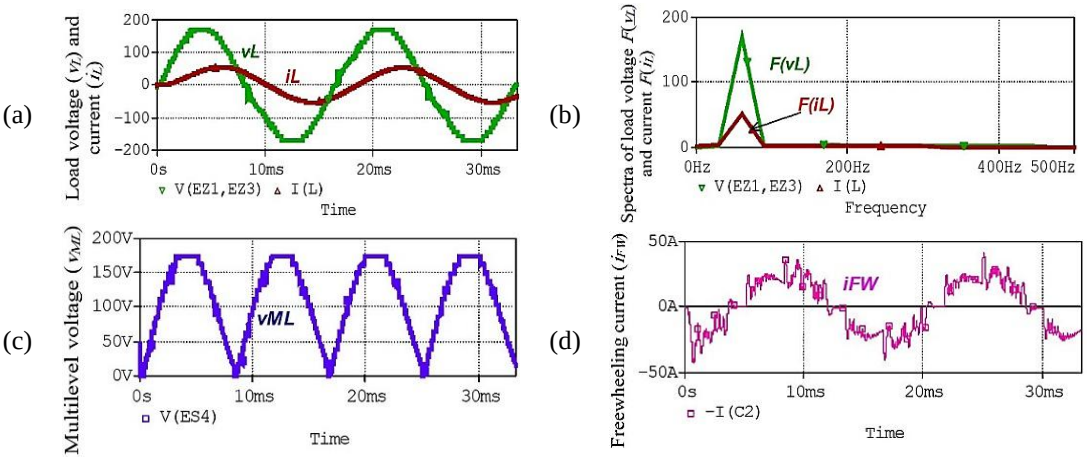

Figure 11. System performance during an inductive load of 60 A (peak value) and 0.8 power factor: (a) v_L and i_L, (b) $F(v_L)$ and $F(i_L)$, (c) v_{ML}, and (d) i_{FW}

4. CONCLUSION

Since multilevel voltage source inverters are a good choice in renewable energy systems, a 31-level single-phase voltage supply is built in this paper by connecting a voltage source inverter to a 15-nonzero level unidirectional power supply that is constructed using binary weighted four DC voltage sources generated by combinations of solar panels. The simulation results have revealed almost sinusoidal voltage and current during resistive loads with negligible harmonic association, whereas the current is a pure sinusoid during inductive loads. The system has a very fast response that is suitable for varying and high starting current loads. The system has a high design flexibility; thus, its rating can be increased without constraints. The system's performance can be improved by increasing the non-zero levels in the unidirectional power supply to 31. This upcoming enhancement will produce, to a certain degree, an ideal sinusoidal load voltage, even for resistive loads.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Abdulkareem Mokif Obais	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	
Ali Abdulkareem Mukheef	✓	✓		✓	✓	✓	✓		✓	✓	✓		✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Derived data supporting the findings of this study are available from the corresponding author, [AMO], on request.

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