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A novel 9-level fourfold-boost switched capacitor inverter (N9L-FBSCI) configuration utilizing fewer components and optimized active switches

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ABSTRACT

Multilevel inverter (MLI) topologies are more important in high-voltage applications where the most common design tends to have significant disadvantages, including being very component when it comes to the switch voltage stress, control scheme, and also not self-voltage balanced. These problems lead to higher cost, lower efficiency, and lower reliability. This paper will therefore develop a new nine-level fourfold-boost switched capacitor inverter (N9L-FBSCI) without increasing the number of components but ensures greater voltage gains and ease of use. It uses only one DC source, eight active switches, and two capacitors with a self-balancing mechanism of the voltage, avoiding extra balancing of the voltage. A four fold voltage gain is achieved using fewer switching devices per stage and less blocking voltage to control across switches. An efficient control is achieved by a level-shifted phase disposition PWM (LS-PDPWM) technique. Analytical and comparative testing against recent MLI design proves that the topology proposed has better voltage boosting and efficiency using the least number of components. Simulation and experimental verification prove the practical efficiency of the N9L-FBSCI, which can achieve a 400 V peak output with low total harmonic distortion. The topology has a high potential in renewable and industrial fields with cost effective high performance. Experimental and simulation data support an output voltage of 400 V at an output load current of 2 A with RL loading (100 Ω, 100 mH) delivering 400 W power output. The efficiency in the case of the inverter reaches its peak at 97.84% and voltage and current total harmonic distortion (THD) of 16% and 6%, correspondingly. The present proposed N9L-FBSCI has a better voltage gain and fewer components than available nine-level topologies without altering the delight of the wave position.

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1. INTRODUCTION

The primary concept of MLI is to combine multiple DC voltage sources to achieve enhanced power output. For instance, [1] introduces a nine-level inverter. This design is notable for its simplicity, requiring only one input source, a few components, while featuring self-voltage balancing capabilities that streamline modulation. A key feature is its dual voltage-boosting capacity. The architecture of single-stage switched-capacitor modules for inverters was explored in [2]. However, it achieves a voltage gain of two. A nine-level inverter utilizing switched capacitors with quadruple-boost capabilities was proposed in [3]-[5], keeping costs low. Despite this, the design imposes high voltage stress on switching devices. A boost inverter in [6]

produces a nine-level output voltage waveform, achieving an output twice as high as the input. Similarly, the architecture in [7] enhances voltage levels, achieves multi-level output, and implements passive voltage balancing but requires more components, leading to higher stress on switches. In [8], is proposed with a quadruple boost and a design of 11 switches and three diodes. Compact SCMLI designs are presented in [9] to improve output voltage quality. The system in [10]-[12] utilizes minimal devices to generate nine levels but experiences high voltage stress, with components operating at their limits. The nine-level inverter in [13] uses a minimal design of ten switches and two floating capacitors (FCs), providing a voltage-doubling feature suitable for higher voltage applications. A transformer-less T-type hybrid boost inverter in [14] delivers higher power density and reduced semiconductor ratings but requires more components. In [15], a single-source quadruple boost multilevel inverter (QB-MLI) with fewer resources is described, incorporating 10 switches, two capacitors, two sources, and one diode. Meanwhile, [16]-[18] proposes a photovoltaic (PV)-based nine-level inverter with improved leakage current and voltage bucking effects, albeit at the cost of increased component count. The SCMLI configuration in [19] employs 13 switches, 22 capacitors, one diode, and a single source, using nearest-level modulation to enhance efficiency and minimize switching losses. For double boost voltage gain, [20] an inverter system utilizing 11-switch and 2 capacitors for nine nine-level boost output is presented, though requiring more components for the desired output. A two-fold voltage boost is achieved by [21] using a grounded, single-source nine-level inverter for high-frequency AC microgrids. The inverter in [22] incorporates 13 switches and two capacitors for a nine-level output, emphasizing voltage boosting and effective use of components. Similarly, [16], [23] describe a compact inverter with one power source and fewer components, using switched capacitors to create virtual DC sources, though with significant voltage stress on polarity circuits. The design in [24] focuses on simplicity, controllability, and voltage boosting, though standing voltages can impact efficiency. A boost inverter with 10 switches and two capacitors offering nine output levels is described in [25], but higher power operation can stress components and affect system reliability. In [26], a quadra boost converter with minimum switches is outlined, requiring more robust components for nine-level outputs. The self-balancing capacitor design in suffers from high standing voltage, while describing a high-efficiency boost inverter with quadruple gain but requiring the most active components for a specific level.

This discussion highlights the potential for designing inverter topologies with fewer components, reduced standing voltages, and minimal active devices while achieving high voltage gains. The principal aim of this work is to describe the proposal of the novel nine-level four-fold-boost switched capacitor inverter (N9L-FBSCI), and experimentally prove the theoretically proposed N9L-FBSCI to be high voltage gain based on a single DC source, very fewer switches, and self-balanced capacitors - however with quality waves and achievable efficiency that fulfils high-voltage power conversion applications when it needs to be in compact size. The article is structured as follows: Section 2 explains the proposed design, its operation, control strategies, and includes a comparative analysis of recent topologies with a power loss study. Section 3 presents simulation and experimental results, while Section 4 provides conclusions.

2. PROPOSED CONFIGURATION

Figure 1 depicts the suggested design N9L-FBSCI, which has one DC source, Vdc, and nine switches, S1–S9. Splitting the system into two primary parts simplifies investigation. The first unit (U1) features five switches (S1-S5), diodes (D1), and capacitors (C1 and C2). The second unit (U2) possesses 4 switches (S6-S9). The first unit provides voltage, whereas the second unit enhances it, resulting in two different magnitudes. Without needing a complete bridge at the terminal ends, the switches in U2 are positioned to produce the required AC output. The voltage stress on the first unit devices is restricted to Vdc and 2Vdc, while the second unit switches encounter 4 Vdc. The circuit switching scheme for inductive load operation in Figure 2 helps the inverter work in various load conditions.

Figure 2 also demonstrates the nine operational states of the N9L-FBSCI. For instance, at the +4 Vdc level, switches S1, S6, S9, and S3 are activated, allowing energy stored in C1, C2, and the input source to supply the load. At +3 Vdc, energy is drawn from C2 and the input source by activating S3, S6, S9, and D1 as shown in Figure 3. During this process, capacitor C1 is recharged to Vdc through parallel operation with the input source.

At the +2 Vdc level, switches S1, S6, S9, and the body diode of S4 are turned on, supplying energy to the load from C1 and the input voltage. Simultaneously, C2 is charged to 2Vdc by operating in parallel with the power source. At +Vdc, switches D1, the body diodes of S4, S6, and S9 are activated, with C1 recharging to Vdc during parallelization with the source, as depicted in Figure 2.

At the zero-output level, switches D1, S2, S7, and S9 are turned on. Here, C1 is charged to Vdc by operating in parallel with the source, but no energy is transferred to the load. For negative voltage levels, switches S1, S3, S8, and S7 are activated at −4 Vdc, delivering energy to the load through C1, C2, and the

input source, as shown in Figure 2. At −3 Vdc, energy is supplied from C2 and the input source by activating D1, S2, S3, S8, and S7 while C1 is recharged to Vdc in parallel with the source.

At −2 Vdc, switches S1, the body diode of S4, S5, S8, and S7 are turned on. The load is powered by the energy stored in C1 and the input source, while C2 charges to 2 Vdc in parallel with the source. For −Vdc, switches D1, S2, the body diode of S4, S8, and S7 are activated, supplying energy from Vdc to the load and recharging C1 to Vdc, as shown in Figure 3. Each of the quasi-square waveform's Fourier decomposition (V_{oi}) might be described as (1)-(3).

$$V_{\text{oi}} = \frac{2V_{\text{dc}}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{\cos(k\theta_{\text{i}})}{k} \sin(k\omega t) \quad (1)$$

$$V_{\text{out}} = \sum_{i=1}^{4} V_{\text{oi}} \quad (2)$$

$$V_{\text{out}} = \frac{2V_{\text{dc}}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \sum_{i=1}^{4} \frac{\cos(k\theta_{\text{i}})}{k} \sin(k\omega t) \quad (3)$$

Where V_{oi}: output voltage component contributed by the i-th switching level; V_{dc}: input DC voltage; k: harmonic order (odd integers only: 1, 3, 5, ...); θ_i: switching angle corresponding to the i-th level; ω: angular frequency of the output waveform ($\omega = 2\pi f$); and V_{out}: total output voltage of the inverter waveform.

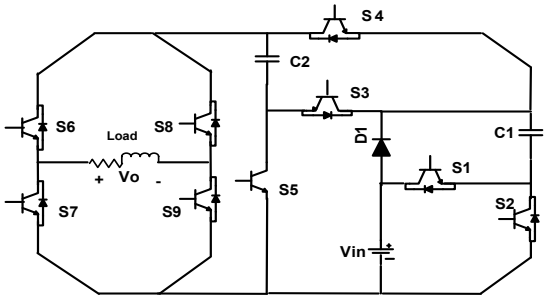

Figure 1. N9L-FBSCI topology

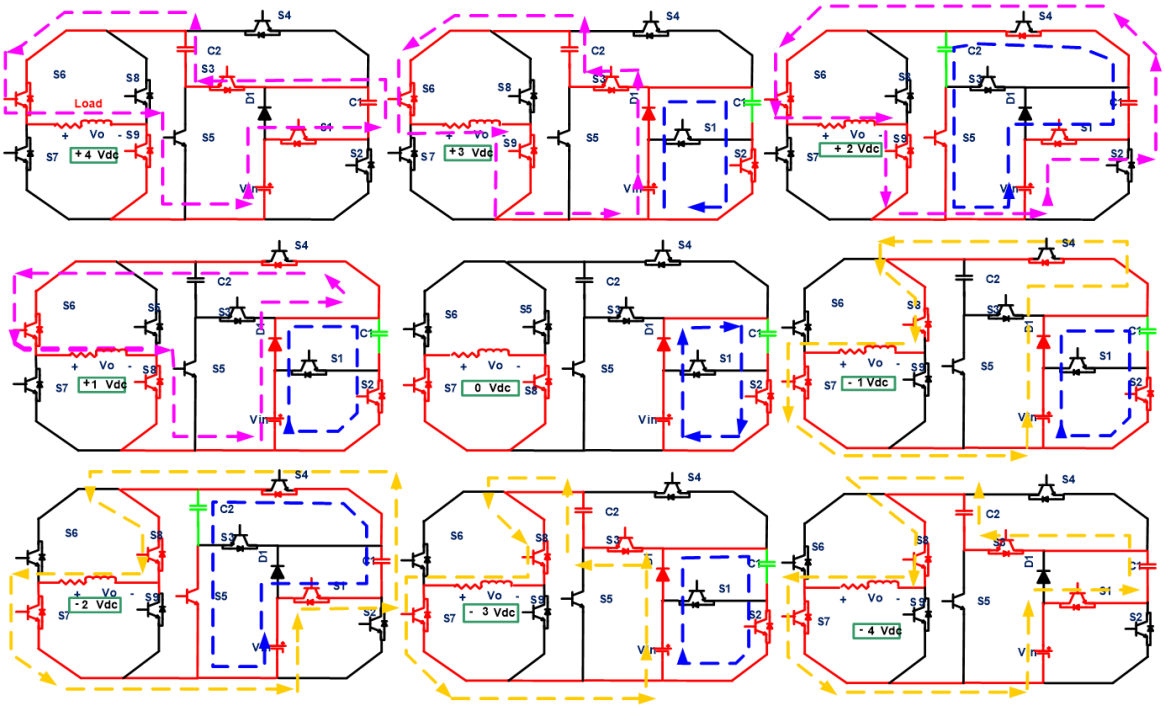

Figure 2. N9L-FBSCI with multiple modes of level generation

2.1. Control strategy

The LSPWM approach for N-level inverters utilizes N−1 carrier signals with consistent frequency and amplitude, covering a peak-to-peak range. Due to its great performance, conceptual clarity, and versatile control choices, LS-PDPWM modulation is becoming more common in multi level inverters (MLIs). This approach generates a nine-level voltage output using eight carrier signals that are perfectly matched to guarantee constant frequencies and peak-to-peak amplitudes. This array of synchronized carriers is called "phase disposition (PD) PWM method." Figure 3(a) shows the basic frequency-modulating wave centrally aligned with the zero-reference line. Carrier magnitudes range from 0 to +4 and -4 to 0, as shown. When the modulating wave exceeds the carrier wave, the operating mechanism triggers. A comparator circuit compares a sinusoidal modulating signal with a triangular carrier wave. This information is processed by logical circuitry to create inverter component switching signals. The suggested nine-level switching signals are shown in Figure 3(b). Synchronized carrier signals and quick triggering and switching signals allow this control method to precisely modulate and alter the voltage output. Figure 3(c) shows the block representation of the control circuit.

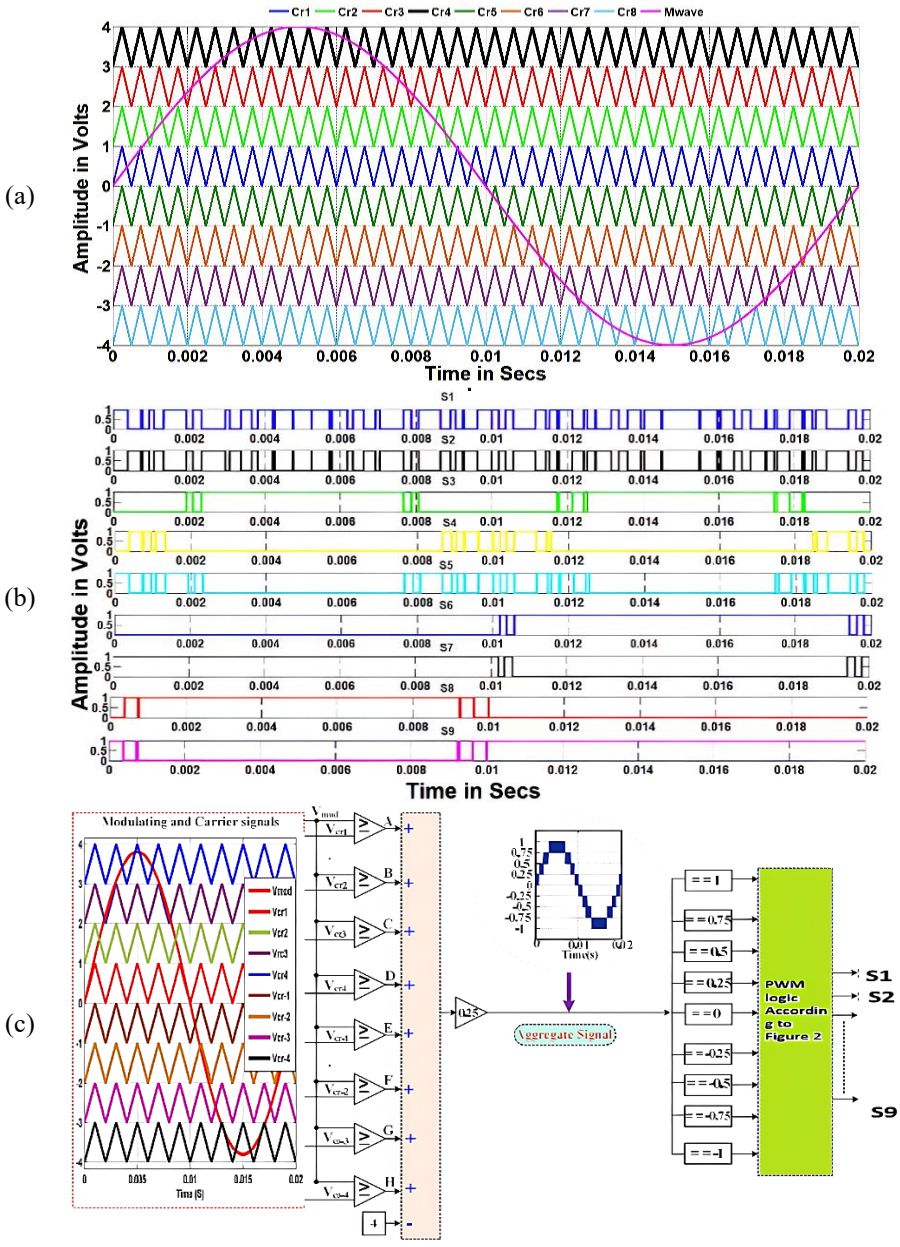

Figure 3. N9L-FBSCI switching behavior according to the PD method: (a) pattern of carriers, (b) switching signal, and (c) block diagram of control circuit

2.2. Comprehensive comparison

The performance of the proposed N9L-FBSCI inverter is evaluated through a detailed comparison of key parameters, including switch count, DC sources, capacitors, voltage boost, and efficiency. Table 1 compares the proposed N9L-FBSCI with selected converter designs reported in [3], [7], [8], [15], [16], [19], [20], [26]. This comparison highlights its reduced component count and superior voltage gain.

Table 1. Comparison with recently reported MLIs (single phase configurations)

MLIs	NL	NSW	NDCS	NC	ND	TNC	MCS	BF	%η
[3]	9	12	2	2	0	14	6	4	80.5
[7]	9	12	1	3	0	16	6	4	97.6
[8]	9	8	1	3	3	15	4	4	93
[15]	9	10	1	2	1	14	5	4	98.2
[16]	9	11	1	3	2	17	5	4	96.08
[19]	9	13	1	2	1	17	6	4	90.94
[20]	9	10	1	2	0	14	5	2	98.86
[26]	9	10	1	2	0	13	5	4	97.3
Proposed	9	8	1	2	2	13	4	4	97.84

NC: number of capacitors, NDS: number of DC sources, NSW: number of switches, ND: number of diodes, CS: maximum conducting switches, BF: boosting factor, TNC: total number of components, η: efficiency

Compared to most designs, the N9L-FBSCI uses fewer switches (NSW) and capacitors (NC), achieving better voltage boosting while maintaining simplicity. Although some configurations, like [1] and [9], use fewer switches, they require more components and offer lower voltage gains. Similarly, while [6] employs two DC sources, the proposed inverter matches others with just one DC source.

The N9L-FBSCI also limits active switches to five per level and reduces conducting switches (MCS) compared to most alternatives. While configurations like [2] and [15] achieve lower conducting switches, they involve more components and reduced voltage gains. Comprehensive comparisons of blocking voltages, charging loops, total components, and efficiency percentage confirm that the N9L-FBSCI outperforms existing designs in terms of simplicity, voltage boost, and efficiency.

3. RESULTS OF N9L-FBSCI

The N9L-FBSCI model was simulated using MATLAB-Simulink to validate the effectiveness of the proposed approach. Level-shifted PWM schemes were implemented and integrated into the N9L-FBSCI framework to demonstrate its practical application. The system design consists of a single DC source rated at V = 100 V, nine IGBT switches, and two capacitors (C1 and C2) with voltage ratings of V and 2 V, respectively. These elements work in unison to produce a 9-level output waveform with a peak voltage of 400 V. The performance of the N9L-FBSCI was assessed at a switching frequency of 2 kHz and across different modulation indices. The system was tested under steady-state conditions, including dynamic load variations at a modulation index of one, as well as in operating modes where the modulation index was below and above unity. As illustrated in Figures 4 and 5, the FFT analysis shows the voltage and current waveforms for an RL load (100 Ω, 50 mH). The output demonstrates a peak fundamental voltage of 400 V, with a voltage total harmonic distortion (THDV) of 14.24% and a current total harmonic distortion (THDi) of 4.06%. The experimental findings further validated the performance of the N9L-FBSCI design. Each FGA25N120 IGBT was controlled using a TLP250 driver circuit, with gate signals generated by the dSPACE 1104 controller. The efficiency of the inverter was obtained at the point of measurement with a Yokogawa WT310E precision power analyzer. The experimental setup for the N9L-FBSCI is shown in Figure 6. Figures 7 and 8 display the output voltage and current waveforms for an RL load (100 Ω, 50 mH) and their corresponding spectral analysis. The experimental results achieved a peak fundamental voltage of 399.2 V and a peak current of 2 A, with THDV recorded at 16% THDi at 6%.

In achieving cost-effective implementation, a circuitually appropriate output filter (e.g., LC or LCL) must be called upon to reduce harmonic distortion and guarantee conformance with regulations, particularly in grid-tied implementation or applications with sensitive loads. The filter design is normally application specific, based upon the load characteristics, switching frequency, and the required attenuation bandwidth. This filtering will be integrated into the next prototypes according to the specifications of certain use cases (PV-grid integration or motor drive) applications.

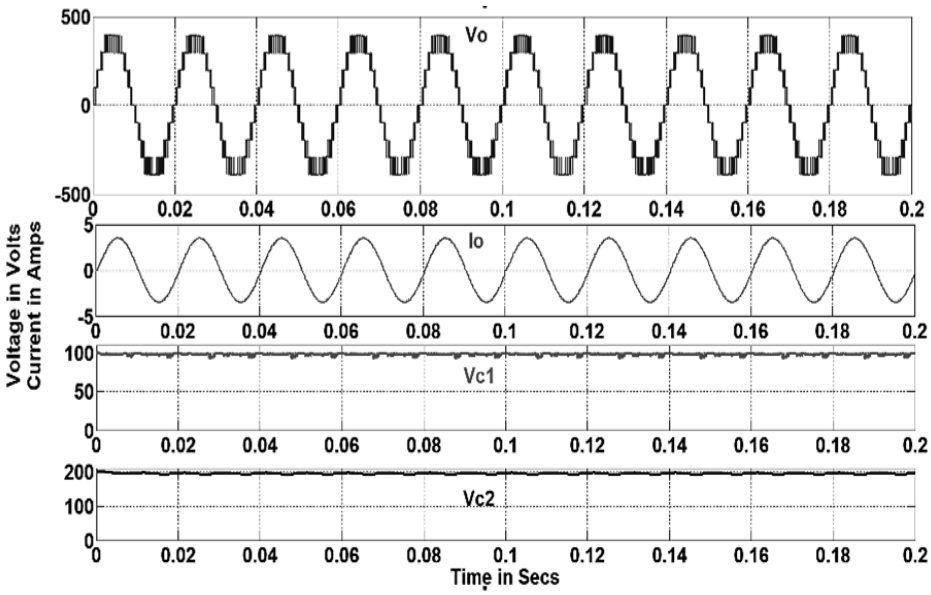

Figure 4. Simulated results showing N9L-FBSCI voltage and current waveforms with RL loading

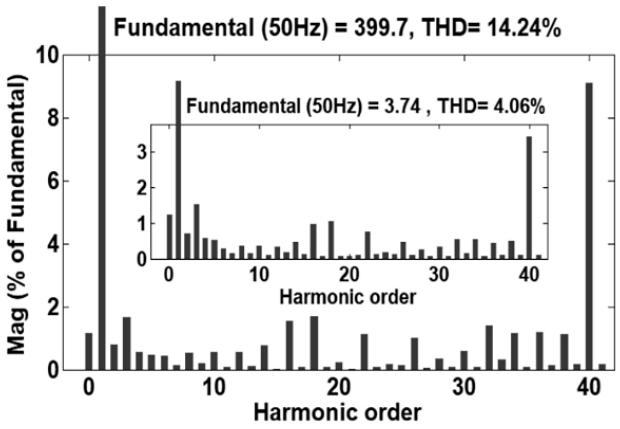

Figure 5. The N9L-FBSCI showcasing the harmonic spectrum of voltage and current outputs

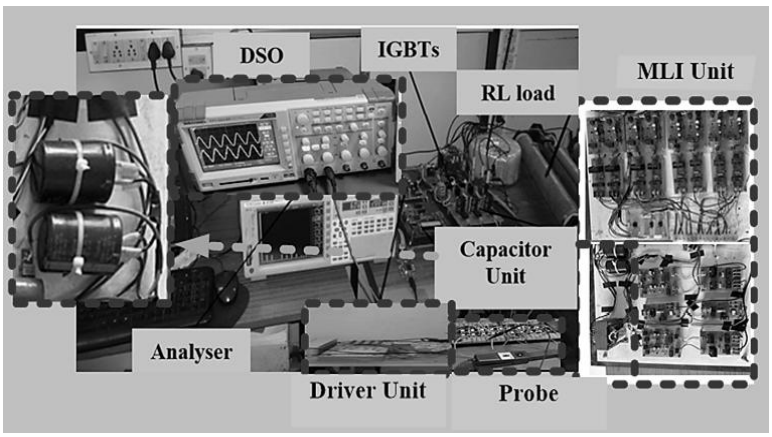

Figure 6. Experimental set up of N9L-FBSCI

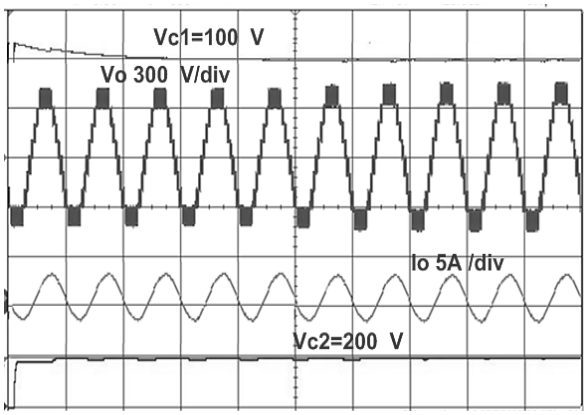

Figure 7. Experimental results showing N9L-FBSCI voltage and current waveforms with RL loading

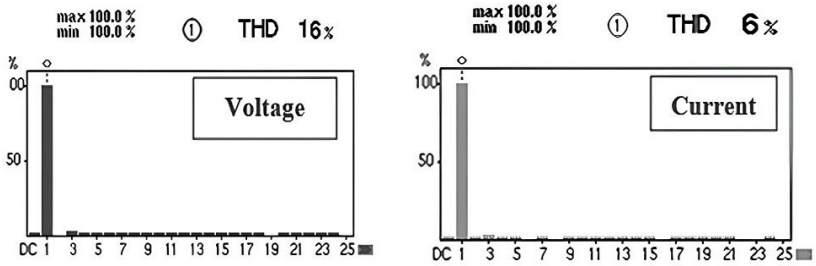

Figure 8. The N9L-FBSCI showcasing the harmonic spectrum of voltage and current outputs

4. CONCLUSION

This research introduces a novel N9L-FBSCI configuration, designed to achieve higher voltage output with nominal components. The proposed design integrates an innovative switched capacitor (SC) arrangement, demonstrating the ability to achieve high voltage levels with fewer components by utilizing a quadruple boost capability. Capacitor voltage self-balancing is guaranteed by this topology by default, removing the need for auxiliary circuits and increasing system control effectiveness.

Key factors, including component count, voltage gain, and voltage stress were compared to equivalent inverter configurations as part of a thorough performance review. Comparative analysis across various criteria reveals that the proposed design outperforms many recent inverter configurations reported in the literature. It achieves superior performance while synthesizing the AC output without relying on a conventional full-bridge structure, thereby reducing voltage stress, which is capped at 2 Vdc.

The effectiveness of the N9L-FBSCI configuration was validated through both simulation and experimental studies. The experimental results closely align with the simulation findings, confirming the suitability of the design for real-world applications. The findings clearly highlight the advantages of the N9L-FBSCI configuration. The design enables elevated voltage levels and delivers substantial voltage amplification via its fourfold boost capability. This consistency underscores the practical viability of the N9L-FBSCI for diverse high-voltage applications.

The performance of the converter with 400 V peak voltage, 2 A load current, and 400 W power rating is checked by simulation and hardware tests. The values of THD voltage and current were recorded as 16% and 6% after respectively, and the inverter reached the maximum efficiency of 97.84%. Demonstrated voltages and imposition of less varying voltages across switches (limited to 4 Vdc, with little change in voltages across components), and the voltage boosting capabilities are better than with similar topologies, which use more switches or more than one source. The outcomes establish the appropriacy of the N9L-FBSCI to short adjustable applications in renewable vigor sources and industry drives.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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I. Kumaraswamy	✓			✓				✓		✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that there is no conflict of interest regarding the publication of this manuscript.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [NS], upon reasonable request.

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