Voltage stress mitigation in high-gain DC-DC converters via dual Z-source DC-DC converter

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ABSTRACT

This paper presents a novel dual Z-source DC-DC converter designed to address the limitations of conventional high step-up converters used in renewable energy applications such as solar photovoltaic systems and fuel cells. Traditional boost and impedance-source converters often suffer from high voltage stress, low efficiency at higher power levels, and complex multi-stage configurations. To overcome these challenges, the proposed topology integrates a hybrid structure comprising symmetrical inductors and capacitors, enabling high voltage gain at reduced duty cycles while minimizing component stress. The converter is analytically modelled and evaluated under continuous conduction mode, and its performance is verified through MATLAB/Simulink simulations and experimental validation using a hardware prototype. The results demonstrate that the proposed converter achieves a voltage gain of up to 10× with a duty cycle below 0.5, while maintaining efficiency above 95% and significantly reducing voltage stress across switching devices. Compared to existing high step-up converters, the proposed design offers improved efficiency, reduced component count, and enhanced reliability. These features make it a promising solution for efficient and sustainable energy conversion in modern renewable energy systems.

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1. INTRODUCTION

The renewable energy production requires converters for power electronics [1]. In response to the depletion of fossil fuels and air pollution, green energy was developed by using renewable resources [2]. The benefits of solar photovoltaic systems are their unrestricted availability and low maintenance requirements [3]. A major problem with RES, like fuel cell and solar array stacks, is their low direct current (DC) output voltage [4]. The proposed study's objective from an environmental perspective is to reduce the distribution system's reliance on fossil fuel-derived energy to prioritize green energy. Typically, DC to DC converters is employed to enhance electricity production and regulate power generation under a range of temperature and environmental circumstances. Only step-up voltage ratios are feasible with BC, which is frequently employed for DC-DC conversion in solar power applications [5].

High duty ratio, low efficiency at greater power, diode reverse recovery issues, high voltage switching, and are a few disadvantages of traditional boost DC-DC converters [6]. Furthermore, efficiency is reduced and overall cost is raised because this method requires the use of several solar panels. Increasing the output energy of solar cells with a high step-up (HS-U) DC-DC converter is another method to deal with this problem [7]. They were intended to boost the voltage gain, and in theory, the more cascaded units employed, the higher the voltage gain that must be achieved [8]. Nevertheless, it increases the circuit's cost and complexity and reduces its conversion efficiency.

Strong voltage gains and low duty ratio of the Z-source (ZS) converter were first introduced by researchers [9]. Nevertheless, these advantages, the power converter has several disadvantages, including uneven input current, severe voltage stress on semiconductors, and incompatibility between the input energy source and the load [10]. As a result, impedance-source-based converters are gaining more attention in research [11]. Traditional boost DC–DC converters, while widely used, suffer from high voltage stress, low efficiency at higher power levels, and complex designs that often require high duty ratios and multiple stages. These drawbacks lead to increased losses, larger component counts, higher costs, and reduced reliability [12]. Even advanced Z-source and quasi-Z-source converters offer high step-up ratios, but they still face significant voltage stress on semiconductor devices, uneven input current, and reduced power density due to additional components [13]. In renewable energy systems, especially under varying irradiance and load conditions, mitigating voltage stress is crucial for extending component life and maintaining efficiency. As a result, our work suggests a novel dual ZS DC-DC converter with low device voltage stress and strong step-up capacity. The major contribution of the proposed method is:
- The proposed converter can generate higher voltage gains than 10 times for duty cycles less than 0.5.
- By utilizing a hybrid structure with symmetrical inductors and capacitors, the converter reduces losses during operation and improves energy efficiency.
- A comparison is also made between the proposed topology and other high-step-up DC-DC converters to clarify its advantages and limitations.

This paper's remaining sections are structured as follows: An overview of the relevant works is provided in section 2. Section 3 explains the suggested topology and the converter's control techniques. Section 4 compares the suggested converter to alternative topologies and presents the results of simulations and experiments. Section 5 ends with a conclusion.

2. LITERATURE SURVEY

Samadian *et al.* [14] introduced a new three-winding connected inductance (HS-U) quasi ZS DC-DC converter based on a multiplier voltage approach. The accuracy of the suggested converter has finally been confirmed by the construction of a 400-W prototype in the lab. Three DC-DC converters were introduced by Salim *et al.* [15] for increased power and reduced voltages in renewable energy-based power systems. The analytical method is examined from the perspective of efficiency and switching stress in this study.

Kishor and Patel [16] suggested an improved high-gain DC-DC converter featuring two BC cycles in 2022. This converter is able to raise a 12 V supply to 98.8 V at a duty ratio of 0.3, demonstrating its superiority over similar converters. In 2023, Shaw *et al.* [17] presented non-isolated boost DC-DC converters with huge voltage gains. To confirm that the suggested structures are effective in terms of improved boosting capability, experimental data are shown for various duty cycles with fixed input voltage. In 2023, Kalahasthi *et al.* [18] suggested a ZVS-based non-isolated high step-up DC–DC converter using a voltage multiplier and two linked inductors (CIs) at a lower duty and turns ratio. The operational effectiveness at full load is 95.11%. Energy-efficient interleaved DC–DC converter-based low voltage stress that was proposed by Hasanpour *et al.* [19] in 2024 is appropriate for AC load application. To assess the results of the steady-state simulation and demonstrate the advantages of the recommended converter, a 1 kW 20–400 V model must be constructed as the last stage [19]. Zhou *et al.* [20] suggested a ZS DC-DC converter for solar energy that has low voltage stress and high gain. The modified experiment model has a 200 W total power rating, a 400 V output rating, and an input voltage range of 40 to 80 V [21], [22]. The experiment validates the precision and viability of the converter's theoretical analysis [23].

3. PROPOSED DUAL Z-SOURCE DC-DC CONVERTER

In this section, a dual Z-source network has been proposed that combines a conventional Z-source modified quasi-ZS network. Figure 1 shows the proposed method's general block. In place of the modified quasi-Z-source n network II, the suggested Z-source network (L1, L11, C1, C12, D1 and L2, L21, C2, C21, D2) substitutes the classical Z-sources network chokes (LI and L2). The proposed circuit configuration is shown in Figure 2 and consists of two quasi-Z source n/w $(L_1 - C_{11} - L_{11} - C_{12} - D_{11})$ and $(L_2 - C_{21} - L_{21} - C_{22} - D_{21})$ combined with a conventional Z-source network (C_1 -L_1 -C_2 -L_2). Also included are two additional diodes (D1 and D2), an output capacitor, and a proposed converter. The innovative design integrates fewer active switches compared to cascaded or multi-stage converters, leading to a simpler and more compact circuit. The dual inductors and capacitors in the hybrid configuration reduce voltage and current ripples, ensuring smoother operation and better output quality.

The converter's efficiency is taken to be 100%. After that, the output current I_o can be written as (1).

$$I_o = \frac{1-2D}{1+2D} * I_i \quad (1)$$

The inductors' current average is represented by $iL_1, iL_2, iL_{11}, iL_{21}$ respectively, the mean current of D_1, D_2, D_{11}, D_{21} is represented by $iD_1, iD_2, iD_{11}, iD_{21}$ and the mean current of MOSFET S is represented by I_S.

$$ID_1 = I_i \quad (2)$$

$$ID_2 = ID_{11} = ID_{12} = I_o \quad (3)$$

$$I_s = I_i - I_o \quad (4)$$

$$IL_1 = IL_2 = I_i \quad (5)$$

$$IL_{11} = IL_{12} = I_o \quad (6)$$

The continuous conduction mode (CCM) functioning of the suggested converter results in a low magnetic inductance, which reduces the size of the primary inductor winding. However, a small turn ratio for the linked inductor is implied by the significant voltage gain. The suggested converter appears more effective than the majority of earlier step-up converters because of its lower leakage inductance. The waveforms of current and voltage for the recommended topology are depicted in Figure 3.

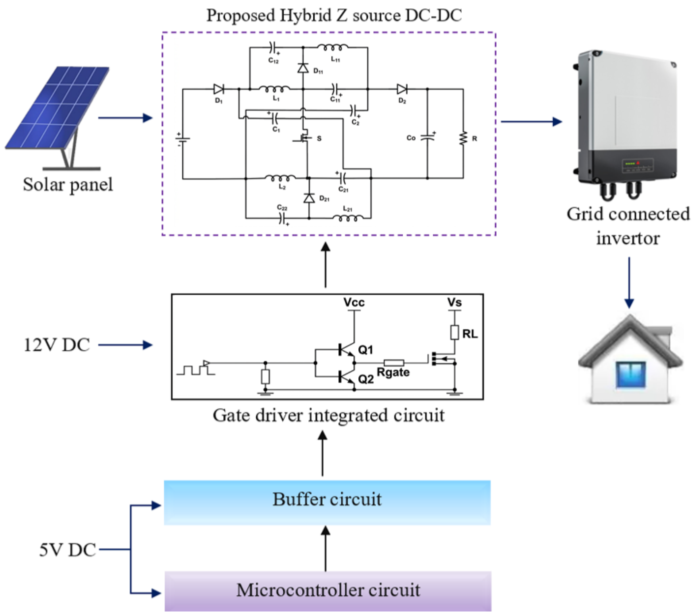


Figure 1. Proposed dual Z-source

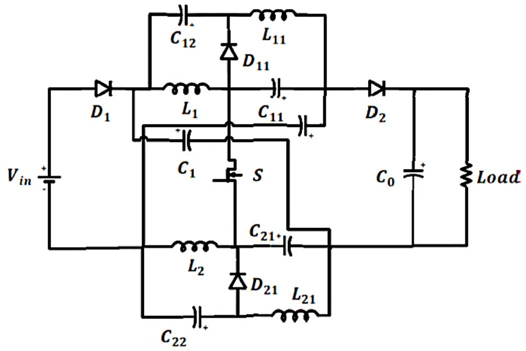


Figure 2. The power circuit of the proposed dual converter

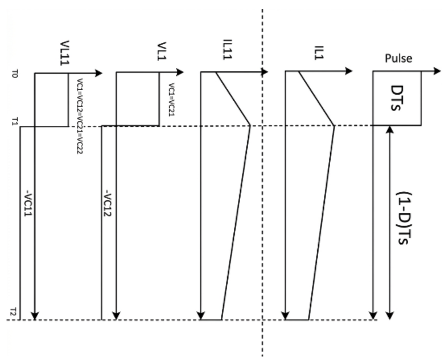
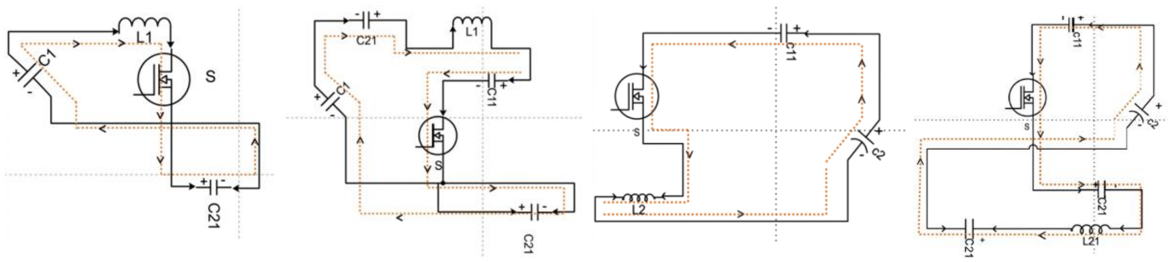


Figure 3. Proposed converter's theoretical waveforms in CCM

3.1. Modes of proposed convertor

Mode 1: Switch S is turned on during this mode [t0-t1]. The off-state function is utilized by each diode. In Figure 4, the present flow path is displayed. The four inductor-based charging loops are connected to one another. $(C_{11} - L_1 - S - C_{12})$ comes first, followed by $(C_1 - C_{12} - L_{11} - C_{11} - S - C_{21})$, $(C_2 - C_{12} - S - L_2)$ and $(C_{11} - S - C_{21} - L_{21} - C_{22})$. During this time, L_1, L_2, L_{11}, L_{21} are all billed simultaneously. Through the output capacitor C_0, power is sent to the load R. As can be used to represent the voltage across the inductors. Figures 4(a)-4(d) represent four charging loops of the inductor during mode 1.

Mode 2: The switch S is not on. Every LED is in the on state. The converter's current flow path in state mode 2 is depicted in Figure 5. A series connection is made between the charging capacitor C_0 and the load R via L_1, L_2, L_{11} and L_{21}. L_1 and L_2 charge C_{12} and C_{22} in the meantime. V_i, C_{21} and L_2 from the DC source charge C_1 and V_i, C_{22} and L_1charge C_2 from the source.



(a) (b) (c) (d)

Figure 4. Charging loops of mode 1: (a) path 1, (b) path 2, (c) path 3, and (d) path 4

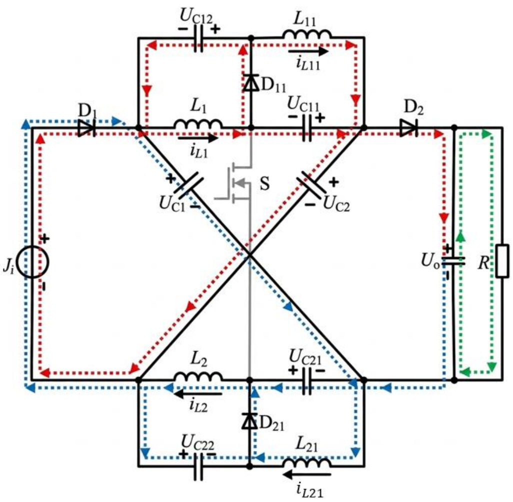


Figure 5. Charging loops of mode 2

4. RESULTS AND DISCUSSION

Compared to existing methods, the proposed topology significantly outperforms the others in this section when it comes to producing low-duty cycle ratios with high voltage gain. The strain on different parts will also be lessened at the same time. Utilizing MATLAB Simulink software, a simulation was executed.

The analysis of this dual z-source converter is validated by a hardware model of the suggested chopper in Figure 6. The experimental parameters are established in a way that is generally in agreement with calculations made in theory. A 60 V input voltage is used for this test, and a 250 V output voltage is produced. To convert the input AC voltage to DC voltage, the full bridge rectifier will employ the stepped-down voltage. The needed topology converter circuit then receives this DC voltage as input. To work, the switch needs a gate voltage of at least 12 volts, which will be provided separately. A microcontroller circuit is used to switch the PWM signal and duty cycle. We are using the Arduino UNO, a microcontroller with an ATMEGA28P CPU, in this instance. The optocoupler is the gate driver IC that we are employing. To protect the controller end and converter end, a driver IC is utilized.

Figure 7(a) (see Appendix) displays the duty cycle, and the output current is shown on the second display. Waveform of output voltage is shown on the third display. The output voltage and current for a 40 V input voltage are 400 V and 0.45 A, respectively. It has a 200 W output power. Figure 7(b) shows duty cycle. The second display shows capacitor voltage VC_{12}. Third display shows capacitor voltage VC_1 waveform. For the input voltage of 40 V, VC_{12} obtained is ≈90 V and VC_1 is ≈220 V. Figure 7(c) shows duty cycle. The second display shows inductor current IL_2 waveform. The third display shows inductor current IL_{11} waveform. For the input voltage of 40 V, IL_2 obtained is ≈6 A, and IL_{11} is ≈0.45 A. Figure 7(d) shows duty cycle. The second display shows diode voltage VD_{21} waveform. The third display shows the switch voltage V_s waveform. For the input voltage of 40 V, VD_{21} obtained is 200 V, and Vs is ≈200 V.

The output voltage is 250 volts for a 60-volt input DC power. The resulting voltage waveform is displayed in Figure 8(a). The capacitor voltage VC1 is 54 volts for a 60-volt input DC power. In Figure 8(b), the output waveform is displayed. The capacitors C11, C12, C21, and C22 have similar voltages due to the topology's symmetry. Additionally, the inductor voltages are the same. Therefore, in order to achieve a greater peak voltage, they can employ a lower duty cycle ratio. The voltage that exists across the switch of the capacitor is 80 volts when the supplied DC voltage is 60 volts. Figure 8(c) shows the oscilloscope waveform of the voltage stress across the diode. The rapid rise and fall times highlight the diode's fast switching capability, while the flat intervals between pulses indicate its low forward conduction voltage during the on-state. In Figure 8(d), the output waveform is displayed.

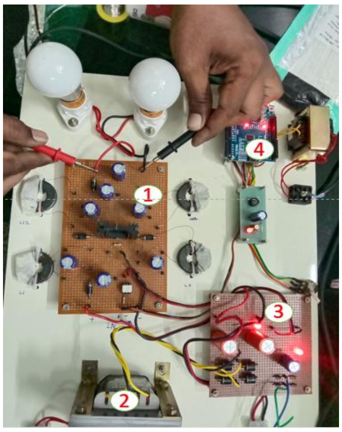


Figure 6. Hardware setup

(a) (b) (c) (d)

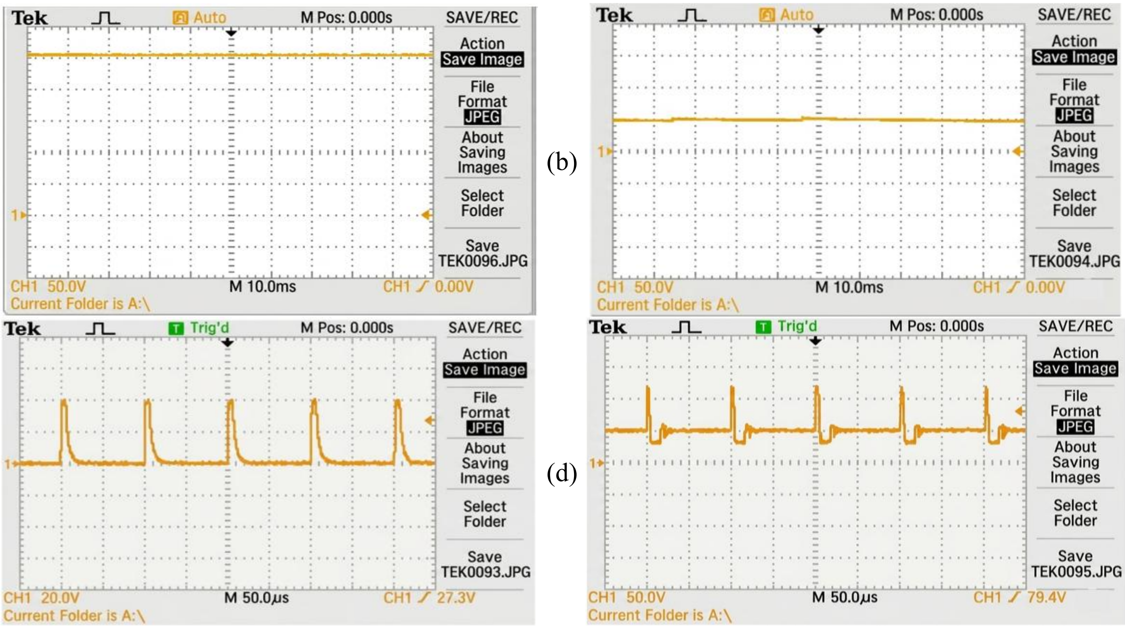


Figure 8. Simulation result: (a) output voltage, (b) capacitor voltage, (c) voltage stress across diode, and (d) voltage stress across the switch

4.1. Discussion

Recently, various studies have been carried out by researchers to improve high step-up DC–DC converter performance, including the topologies in [24]-[26]. The proposed dual Z-source DC–DC converter is implemented and assessed through MATLAB/Simulink simulations and validated using a hardware prototype. The study has demonstrated a high degree of efficiency in achieving large voltage gains at low duty cycles while minimizing device voltage stress. Voltage gain, efficiency, component stress, and duty cycle limitation are the four measures that have been used to assess the performance of the suggested approach. For an input voltage of 40 V, the proposed converter achieves an output voltage of 400 V (10× gain) at a duty cycle below 0.5, with an efficiency exceeding 95% and a switch voltage stress of approximately 80 V. The proposed method is contrasted with the converters in [24]-[26], which achieve lower voltage gains at similar or higher duty cycles and exhibit higher voltage stresses.

Thus, by contrasting the findings of this study with those of other investigations, it is evident that the proposed methodology offers a more efficient and reliable solution for renewable energy integration. The limitation of the proposed converter is that its performance has been validated for specific power ratings and input voltage ranges; efficiency and gain characteristics may vary for different operating scales or environmental conditions. To overcome these limitations, future research will focus on scaling the proposed design for higher power ratings, integrating it with different renewable energy sources, and optimizing control strategies to maintain high efficiency under dynamic load and irradiance variations. These initiatives aim to further enhance the adaptability and robustness of the converter in practical renewable energy systems. Additionally, it focuses on optimizing the design to lower the passive component count and ensuring closer alignment between simulation and prototype configurations.

5. CONCLUSION

In this study, a dual Z-source DC-DC converter with excellent step-up performance and low device voltage stress is presented in this work. Using the introduced converter, a high-voltage gain of approximately ten times could be obtained at a duty cycle below 0.5. By using a hybrid structure with symmetrical inductors and capacitors, the converter reduces losses during operation and improves energy efficiency. Additionally, a comparison analysis is conducted to examine the advantages and distinctions between the suggested topology and alternative techniques. Additionally, an experimental prototype is constructed, and associated data are provided to demonstrate the specific presentation of the proposed converter and validate the benefits and analysis. Hardware results validate the converter's theoretical performance, demonstrating consistent high voltage gain and low component stress under practical conditions.

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AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
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Arockiaraj Sesaiya		✓		✓		✓		✓		✓			✓	
Bhavani Ramachandran		✓	✓		✓			✓		✓		✓		
Ramya Hyacinth Lourdusamy	✓			✓		✓	✓		✓		✓		✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

INFORMED CONSENT

The author certifies that they have explained the nature and purpose of this study to the above-named individual, and they have discussed the potential benefits of this study participation. The questions the individual had about this study have been answered, and we will always be available to address future questions.

ETHICAL APPROVAL

The author's research guide has reviewed and ethically approved this manuscript for publication.

DATA AVAILABILITY

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

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APPENDIX

(a)

(b)

(c)

(d)

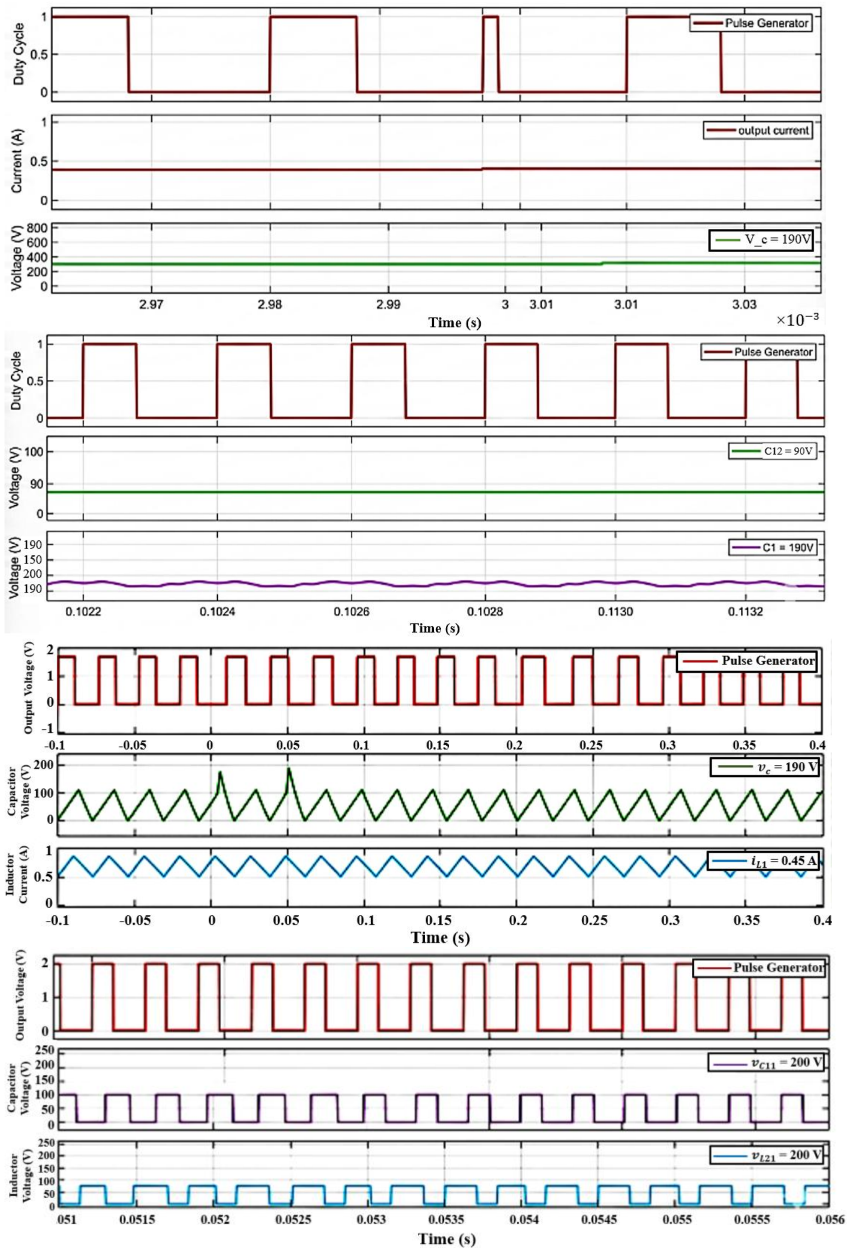

Figure 7. Simulation output: (a) output voltage and current, (b) capacitor voltage, (c) inductor current, and (d) diode and switch voltage

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