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Simulation and comparison of trapezoidal triangle carrier signal with different reference signal for 1500 V DC bus 3 level ANPC inverter

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ABSTRACT

High voltage application to generate staircase output to reduce the total harmonic distortion (THD), the multilevel topologies gaining more and more attractions, and new topologies have been developed. This paper discuss about the advantage of active neutral point clamp (ANPC) topology over neutral point clamp (NPC), flying capacitor neutral point clamp (FCNPC) and T-type neutral point clamp (TNPC) topologies are discussed when it used for DC bus voltage of 1500 V. For ANPC topology several PWM techniques are used to calculate the total harmonic distortion, including phase opposition pulse width modulation (PODPWM), phase disposition pulse width modulation (PDPWM), and alternative phase opposition disposition pulse width modulation (APODPWM), phase shifted pulse width modulation (PSPWM), bus clamping PWM (BCPWM), trapezoidal triangle PWM (TRPWM), third harmonic injected PWM (THIPWM), and sinusoidal PWM (SPWM), three-phase sinusoidal signals with a 13th harmonic signal (THISDPWM). Also, the parasitic inductance model of ANPC topology is discussed. To use 1200 V switching device the most efficient PWM technique for a 1500 V DC bus, 3 phase 3 level ANPC inverter is determined by comparing the RMS value of phase voltage, THD, and peak voltage across the switching device. PSIM has been used to simulate a 3 level inverter using various PWM techniques.

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1. INTRODUCTION

India's per capita electricity consumption increased by 45.8% (438 kWh), from 957 kWh in 2013–14 to 1,395 kWh in 2023–24, primarily due to the addition of 129 GW of renewable energy capacity [1]. In 2024, India's solar energy capacity is expected to reach 94.17 GW. A total 261.15 GW of installed and pipelined solar projects were in the country as of November 2024, suggesting a strong foundation for future growth and expansion in the solar sector [2]. To transmit such a high power rating, the standard operating voltage of 690 V AC is insufficient. In order to improve cost performance, 1140 V AC system is being suggested [3]. Conventional two-level inverters have been found to be unsuitable for medium and high voltage utility grids when used as an interface between energy sources and the grid because they have fewer output voltage levels and, consequently, higher harmonics in the injected grid current.

Multilevel topologies are becoming more and more popular, and new topologies have been created. High voltage is used to create staircase output in order to lower the total harmonic distortion (THD). In this paper phase opposition pulse width modulation (PODPWM), phase disposition pulse width modulation

(PDPWM), alternative phase opposition disposition pulse width modulation (APODPWM), phase shifted PWM, bus clamping PWM (BCPWM), trapezoidal triangle PWM (TRPWM), third harmonic injected PWM (THIPWM), and three-phase sinusoidal signals with a 13th harmonic signal (THISDPWM) are some of the PWM techniques used to analyze the total harmonic distortion for ANPC topology. Additionally, the ANPC topology's parasitic inductance model is covered. By comparing the RMS value of phase voltage, THD, and peak voltage across the switching device, the most effective PWM technique for a 1500 V DC bus, three phases, and three level ANPC inverter is identified for use with 1200 V switching devices. Several PWM techniques have been used in PSIM to simulate a three-level inverter.

Several innovative modulation techniques for ANPC are incorporated into the control algorithm. The optimization targets can be divided into the following three categories: i) the main objective is that the peak voltage should't exit 1200 V as the switching device used for 1500 V application is 1200 V IGBT; ii) reducing the output voltage THD; and iii) to raise the rms output voltage by using appropriate modulation technique.

2. METHOD

Multilevel topologies are classified by various ways like the convectional and non-convectional [4], based on single DC source and multiple DC source [5], based on voltage source inverter and current source inverter [6], based on H-bridge and non H-bridge topologies, based on symmetric DC source and asymmetric DC source [7]-[9]. A single DC source is used in a combination of centralized, medium voltage grid-onnected inverters with different power ratings. This is commonly referred to as the central inverter system. In central inverter with single DC source the topologies like NPC, FCNPC, ANPC, and TNPC are used. The comparison of these topologies is given in Table 1 [10].

The uneven distribution of losses between the inner and outer switching devices in each converter leg is one of the disadvantages of the 3L-NPC topology [11]-[14]. The asymmetrical semiconductor-junction temperature distribution caused by the semiconductors' separate heat sinks and cooling systems limits the maximum power rate, output current, and switching frequency of the inverter for a given semiconductor technology and has an impact on the cooling system design. In NPC inverter topology when it's operated on 1500 V DC bus with half a rating of the device can have very high dv/dt at the switching and that may damage the switching device. In T-NPC topology the switching device can block the entire DC bus voltage and hence the voltage rating of the switching device depends upon the DC bus voltage so when operates on 1500 V DC bus system the switching device rating should be very high and hence the cost of the overall system will increases [15]. FC-NPC topology has major advantages over NPC, ANPC and TNPC topology in term of capacitor voltage balancing but the major disadvantage of this topology is the larger number of capacitor and complex control mechanism [13]. The ANPC topology first proposed by ABB. Figure 1 depicts the structure of a three-level ANPC (3L-ANPC) that uses switching devices in place of the clamp diodes in a three-level NPC topology [16]. The switching states of the 3L-ANPC topology are summarized in Table 2 it includes four extra zero states in addition to the same positive and negative switching states as the 3L-NPC converter [17], [18].

Table 1. Comparison of three level topologies based on component

Components	NPC	ANPC	FC NPC	TNPC
Freewheeling diodes	6	0	0	0
Switching devices	12	18	12	18
DC link capacitor	2	2	2	2
Flying capacitor	0	0	2	0
Balancing capacitor	0	0	1	0
DC sources	1	1	1	1
Total components used	21	21	18	21

Table 2. Switching states for ANPC topology

State	T1	T2	T3	T4	T5	T6
P	1	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	0	1	1	0
0	1	0	1	0	0	1
0	0	0	1	0	0	1
N	0	0	1	1	1	0

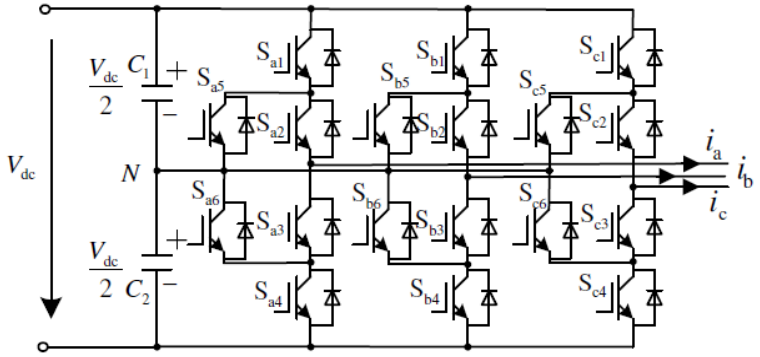

Figure 1. Topology for 3 level ANPC inverter

3. PWM METHOD FOR 3-LEVEL ANPC

The control algorithm incorporates multiple novel modulation techniques based on the carrier signal and reference signal is available for ANPC inverter [19]. In this paper trapezoidal triangle signal is used for carrier signal and various reference signal will be compare for purposes can be used to categorize the optimization targets [20]. For the 3 level ANPC inverter there are 48 switching states are available, some of the switching states are dangerous and can cause the short circuit of the DC bus voltage. When the switch S_{a5} and/or S_{a6} are in ON condition some of the switching states are no longer dangerous. All the switches operate in different combination to generate three level output voltage. Depending upon the switching time the switches may operate in either high frequency mode (HF) or operate on output law frequency (LF), the basic principle is describing in references [21]. Figure 2 shows the different PWM method based on HF/LF combination is describes. The zero state, in which the current travels via various conduction pathways, is where these PWM techniques diverge from one another.

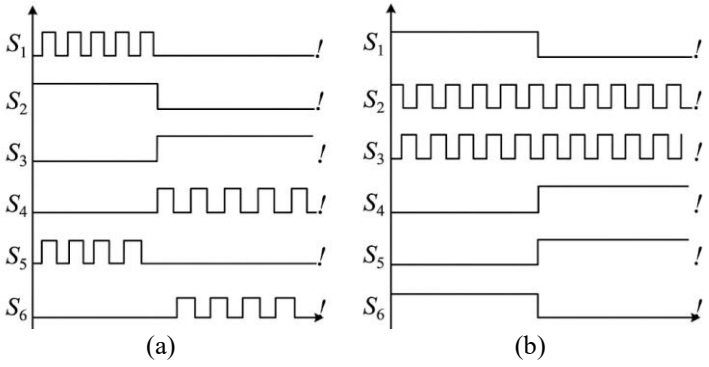

Figure 2. Different PWM methods for ANPC inverter: (a) PWM1 and (b) PWM2

3.1. Trapezoidal triangle PWM

To generate the above PWM pulses the sin-trapezoidal triangle comparison techniques are used. These techniques do not require any optimization techniques, extensive offline calculations, or look-up tables for the desired switching states of power switches, in contrast to the other optimized PWM techniques [22]-[24]. Due to its low switching losses, reduced harmonics in the output voltage waveform, and simplicity of implementation, this technique is advantageous. In this method, the reference signal (V_r) is compared with the trapezoidal triangle carrier signal (V_c) to generate the PWM pulses [25], [26]. Limiting the magnitude of a triangular wave produces that trapezoidal wave. Figure 3 displays the gate pulse that is produced when a sine wave is compared to the trapezoidal reference signal [27]. Based on the phase arrangement, these techniques are further classified as given below.

3.1.1. Phase disposition PWM (PDPWM)

The PDPWM method for a three-level inverter involves shifting two carrier signals vertically with DC offset equal to the carrier magnitude on either side of the zero reference (V_r). This is illustrated in

Figure 3(a) and involves the same carrier signals in terms of frequency, amplitude, and phase. The PWM pulse for a three-level inverter is produced by individually comparing the carrier signals with a reference signal, as shown in Figure 3(a) [28], [29].

3.1.2. Phase opposition disposition PWM (PODPWM)

Every carrier signal in the PODPWM technique has the same frequency and amplitude but a different phase. As seen in Figure 3(b), two carrier signals for a 3-level inverter that are located above the zero reference frame are 180° out of phase. These signals are out of phase with the carrier signals that are located below the zero reference [28], [29].

3.1.3. Alternative phase opposition disposition PWM (APODPWM)

All of the carrier signals in this technique are the same frequency and amplitude, but they are positioned so that neighboring carriers are 180° out of phase. In this opposite-phase arrangement, two carriers are positioned alternately above and below the zero reference line for a three-level inverter. The necessary switching pulses are then produced by comparing these carriers with a sinusoidal reference signal as seen in Figure 3(c). APODPWM offers balanced voltage distribution across inverter switches, enhances waveform quality, and lowers some lower-order harmonics [28], [29].

3.1.4. Phase shifted (PS) PWM

There is (m-1) carrier signals of equal frequency and magnitude that are equally phase shifted over one switching period for an m-level inverter. As shown in Figure 3(d), two carrier signals for a three-level inverter have the same frequency, amplitude, and DC offset but a 90° horizontal phase shift. As illustrated in Figure 3(d), the carrier signals and the sinusoidal reference (Vr) are then compared to create the appropriate PWM pulses [28], [29].

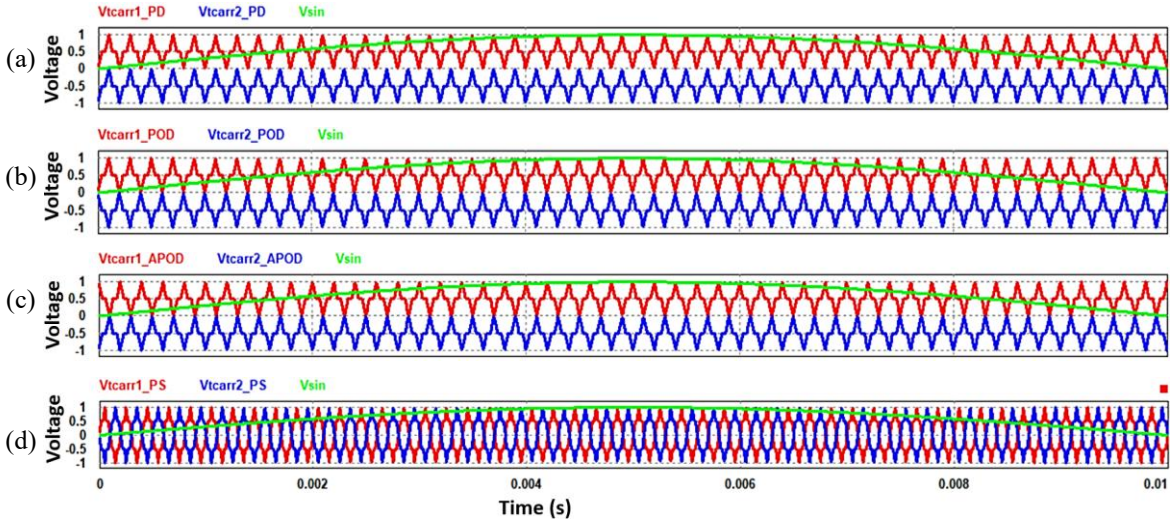

Figure 3. Different trapezoidal triangle carrier based PWM method for ANPC inverter: (a) phase disposition PWM (PDPWM), (b) phase opposition disposition PWM (PODPWM), (c) alternative phase opposition disposition PWM (APODPWM), and (d) phase shifted (PS) PWM

3.2. Generation of various reference signal

The various reference signals are given below:

3.2.1. Sinusoidal pulse width modulation (SPWM)

An extensively used method for regulating the output voltage of inverters is sinusoidal pulse width modulation, or SPWM. This technique creates switching pulses by comparing a high-frequency triangular carrier signal with a sinusoidal reference signal. As seen in Figure 4(a), the pulse widths are determined by the points where the reference and carrier signals intersect. By producing an output that is almost sinusoidal, SPWM lowers harmonic distortion. It offers good control over the inverter's output voltage and frequency and is easy to implement [29]. The mathematical expression is given (1).

$$Vr = sin(\omega t), Vy = sin\left(\omega t - \frac{2\pi}{3}\right), Vb - sin\left(\omega t + \frac{2\pi}{3}\right) \quad (1)$$

3.2.2. Third harmonic injected PWM (THIPWM)

The third harmonic injected PWM is created by superimposing a third harmonic component on top of the fundamental component. The fundamental's maximum amplitude is enhanced by including a third harmonic component in the output and reference signals as shown in Figure 4(b). By eliminating the third harmonic component, this method improves the use of the DC supply [30].

$$X = K * \sin(3\omega t)$$
$$Vr = sin(\omega t) + X, Vy = sin\left(\omega t - \frac{2\pi}{3}\right) + X, Vb - sin\left(\omega t + \frac{2\pi}{3}\right) + X \quad (2)$$

3.2.3. Ninth-order harmonic injected PWM

A variant of the THIPWM that was previously discussed is the ninth harmonic injection pulse width modulation. It is simply the addition of the third and ninth harmonics to the basic sine wave as seen in Figure 4(c). It offers low harmonic distortion and a higher fundamental voltage. In addition to permitting over modulation, the resulting flat-topped waveform further enhances the frequency spectra of the AC and DC terms [30].

$$X = K * sin(3\omega t); K = 0.19$$
$$Y = M * sin(9\omega t); M = -0.029$$
$$Vr = sin(\omega t) + X + Y, Vy = sin\left(\omega t - \frac{2\pi}{3}\right) + X + Y, Vb = sin\left(\omega t + \frac{2\pi}{3}\right) + X + Y \quad (3)$$

3.2.4. Thirteenth order harmonic injected PWM

In this method the thirteenth order reference wave is created by adding 13th order into the saturated fundamental component which magnitude is limited between -1.5 to 1.5 and the resultant waveform will be added to the fundamental sine wave and hence the peak amplitude is modified as shown in Figure 4(d). The mathematical expression is given in (4) [31].

$$X = q * Bm * sin(\omega t + \alpha), q \epsilon [-1,1], Bm \epsilon [-1.5,1.5], \alpha = 0°, -120° and -240° K * sin(3\omega t); K = 0.19$$
$$Y = r * Am * sin(13\omega t + \alpha): r = 0.01$$
$$Vr = sin(\omega t) + X + Y, Vy = sin\left(\omega t - \frac{2\pi}{3}\right) + X + Y, Vb = sin\left(\omega t + \frac{2\pi}{3}\right) + X + Y \quad (4)$$

3.2.5. Sixty degree bus clamp pulse width modulation (SDBCPWM)

A variation on the third harmonic injected PWM technique, the sixty degree PWM method involves holding the switch high (or low) for sixty degrees of each half cycle of the fundamental. As a result, switching losses are decreased and the fundamental voltage component is raised. The periodic signal obtained by adding all of the harmonics with the fundamental is depicted in the Figure 4(e) as having a flat part. This technique's name refers to the flat portion covering the phase angle of sixty degrees [32].

$$Vr = sin(\omega t + \alpha) + f1(\theta)\{Vc - max(Vr, Vy, Vb)\} + f2(\theta)\{-Vc - min(Vr, Vy, Vb)\} \quad (5)$$
$$\alpha = 0°, -120° and -240°$$
$$f1(\theta) = 0 (when\ 0° < \theta < 60°)$$
$$= 1 (when\ 60° < \theta < 120°)$$
$$f2(\theta) = 1 (when\ 0° < \theta < 60°)$$
$$= 0 (when\ 60° < \theta < 120°)$$

3.2.6. Thirty degree bus clamping pulse width modulation PWM (TDBCPWM)

In the bus clamping PWM generation method every phase remains clamp at thirty degree of every half cycle in both positive and negative cycle as shown in Figure 4(f). For 30° (π/6 radians) of the fundamental output cycle, one inverter leg (phase) of TDBCPWM is clamped to either the positive or negative DC bus. In order to maintain symmetry, this clamping takes place every 60 degrees. By keeping one switch ON (or OFF) for the clamped duration while the other two phases continue their regular modulation, the clamping alters the traditional sinusoidal PWM. The effective number of switching transitions per cycle is lowered as a result. TDBCPWM raises the DC bus utilization in comparison to SPWM, enabling a higher output voltage fundamental component without raising the DC link voltage [32].

$$Vr = sin(\omega t + \alpha) + f2(\theta)\{Vc - max(Vr, Vy, Vb)\} + f1(\theta)\{-Vc - min(Vr, Vy, Vb)\} \quad (6)$$

3.2.7. Triangle saturated common mode pulse width modulation (TSCMPWM)

Sinusoidal reference wave is added by a saturated triangle wave to generate the triangle saturated common mode pulse width modulation signal (TSCMPWM) as shown in Figure 4(g) [30]-[32].

$$\begin{aligned} X &= 2\pi C * sin - 1\{sin(3\omega t)\} \\ Y &= V1 \\ &= 0.11C\ (when\ X > 0.11C) \\ &= -0.11C\ (when\ X < -0.11C) \end{aligned}$$

$$Vr = sin(\omega t) + Y, Vy = sin\left(\omega t - \frac{2\pi}{3}\right) + Y, Vb = sin\left(\omega t + \frac{2\pi}{3}\right) + Y \quad (7)$$

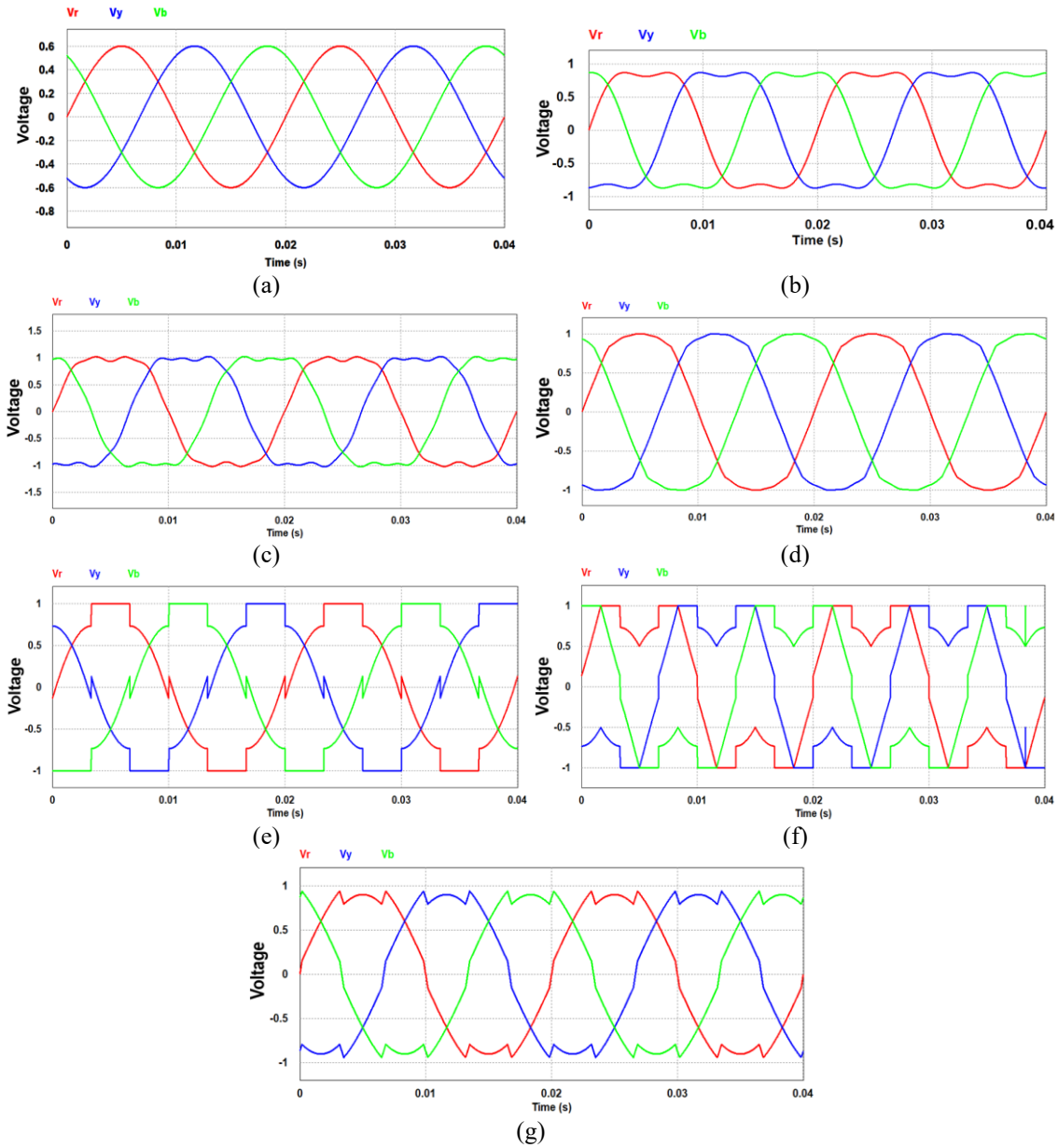

Figure 4. The modulating signal with different PWM techniques: (a) SPWM, (b) THIPWM, (c) ninth order harmonic injected PWM, (d) thirteenth order harmonic injected PWM, (e) SDBCPWM, (f) TDBCPWM, and (g) TSCMPWM

3.3. Parasitic inductance model of 3 level ANPC inverter

When the switching frequency is at higher side the interconnection between the components causes the stray inductance which can have higher di/dt and these may leads to high voltage spike at the semiconductor device which may damage it. As compare to NPC inverter ANPC inverter has more commutation path between the DC link capacitor to the switching devices, in between switching devices modules, and between switching devices and load connected. Figure 5 shows the one leg of ANPC inverter having 3 dual IGBT modules connected. Switch S1 and S5 are the upper module, switch S4 and S6 are the lower module, and switch S2 and S3 are the clamp module. L_q is the parasitic inductance of half bridge module and can be obtained this value from ROHM's technical manual [33]. L_{qclamp} is the parasitic inductance between the busbar and switching module [34]-[36]. L_{qinv} is the parasitic inductance at AC side and L_{bus} is the parasitic inductance at DC side busbar connection. The value of parasitic inductance can be minimized by using the laminated busbar and provide proper switching to the devices [37].

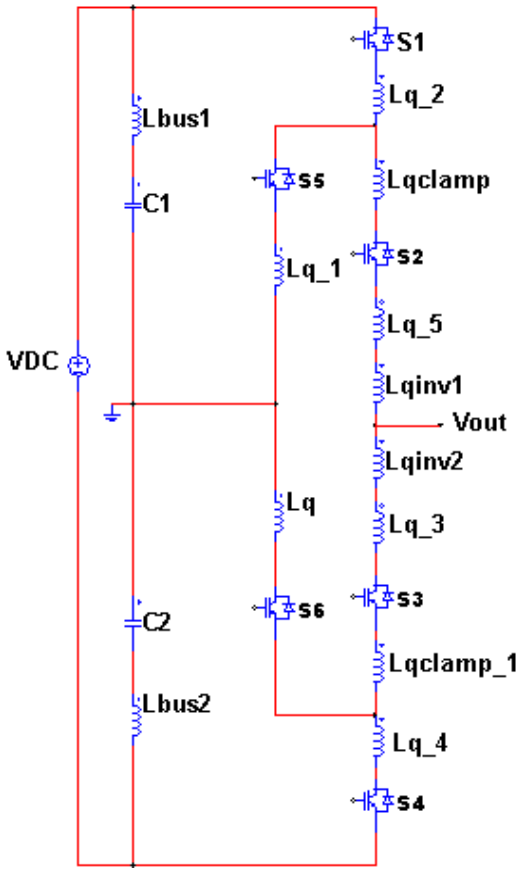

Figure 5. ANPC inverter R-phase bridge arm parasitic inductance model

3.4. Simulation of 3 level ANPC inverter with different PWM generation techniques

In this paper simulation is carried out with following parameters. The simulation parameters are selected as below: V_{dc} = 1500 V, C_1 = 28.2 mF ,C_2 = 28.2 mF, R_{load} = 27 mΩ, L_{load} = 2400 µH, L_q = 30 nH, L_{qclamp} = 120 nH, L_{qinv} = 120 nH, L_{bus} =120 nH. Switching frequency f_{swich} = 5 kHz. 1200 V IGBT is selected as a switching device. In the simulation IGBT saturation voltage = 2.2 V, Transistor resistance = 0.25 mΩ, Diode threshold voltage = 0.7 V, and diode resistance = 4 mΩ. To generate the PWM pulses carrier wave can be obtained by using trapezoidal wave with different combination of PDPWM, PODPWM, APODPWM, and PSPWM techniques and its compare with the reference wave generated by different techniques as seen in Figures 6(a) to 6(c).

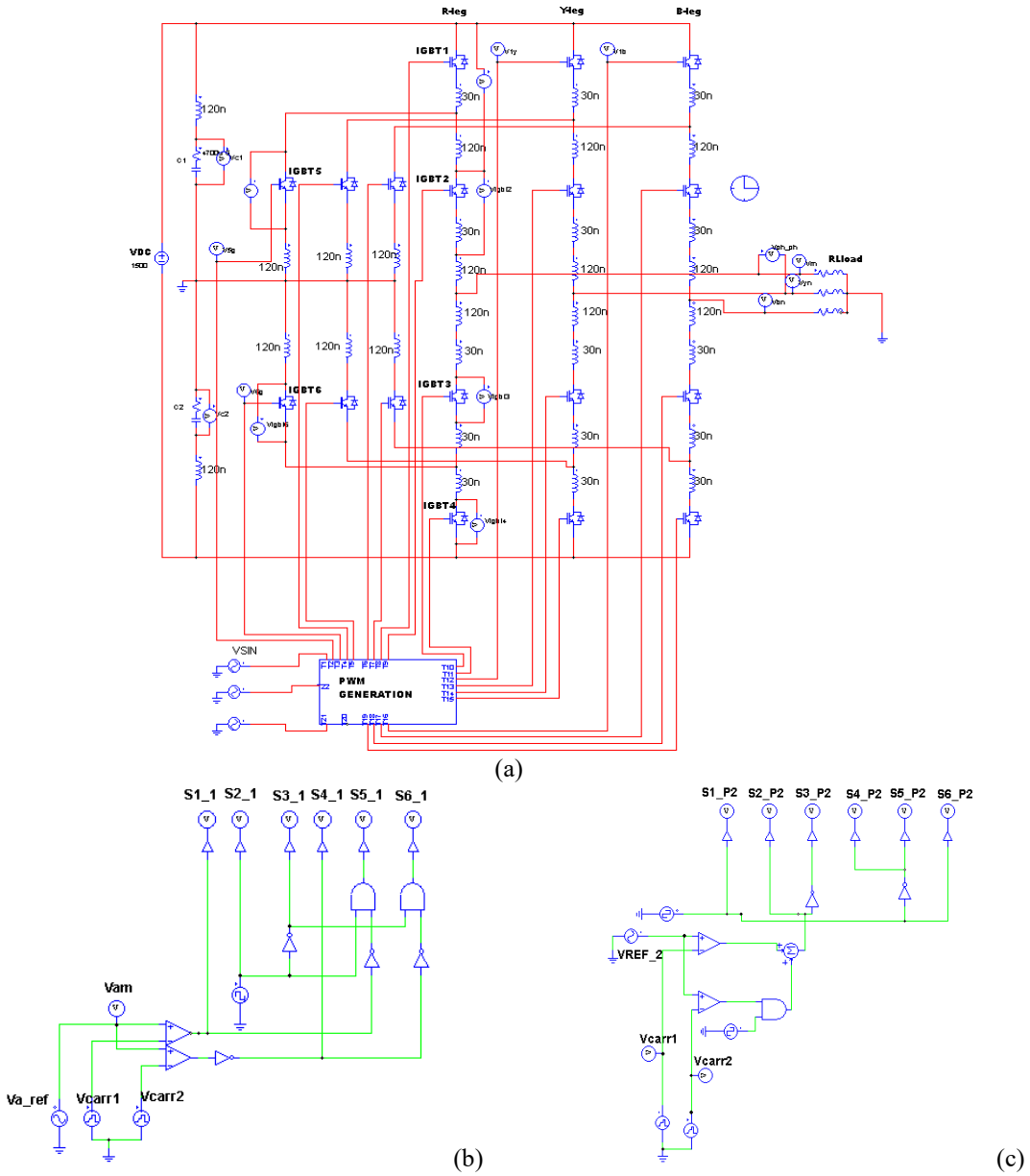

Figure 6. ANPC inverter: (a) simulation schematic diagram, (b) generation of PWM1, and (c) generation of PWM2

4. RESULTS AND DISCUSSION

In this section, it is explained the results of research and at the same time is given the comprehensive discussion. Results can be presented in figures, graphs, tables, and others that make the reader understand easily [14], [15]. The discussion can be made in several sub-sections.

PSIM software is used for the simulation and the data presented here in different sections. The modulation index is taken as 1 and measures the THD value of output phase voltage and the peak voltage across each switching devices. To generate the gate pulses of PWM1 and PWM2 techniques for switch S1 to S6 the carrier wave generated by trapezoidal wave arranged in PDPWM, PODPWM, APODPWM, and PSPWM are compared with the reference wave generated from the SPWM, THIPWM, ninth order harmonic injected PWM, thirteenth order harmonic injected PWM, SDBCPWM, TDBCPWM, and TSCMPWM.

4.1. PWM1 fed ANPC inverter output voltage, THD, and peak voltage across switch

From the given Figures 7, 8, and Table 3, it can be seen that the lowest voltage THD 27.41% and rms voltage 1051 V with voltage peak across each device obtained less then 1200 V in PDPWM with reference signal taken as 13th order harmonic injection method. The highest rms voltage 1141 V obtained

when PSPWM technique is used in 9th order harmonic injection and TDBCPWM method but the voltage THD obtained are 37.51% and 36.53%, respectively. However, the peak voltage of TDBCPWM fed reference signal crosses the 1200 V.

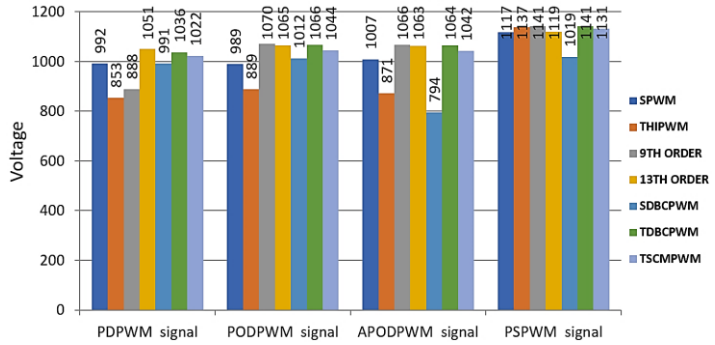

Figure 7. Comparison of RMS output voltages for PWM1

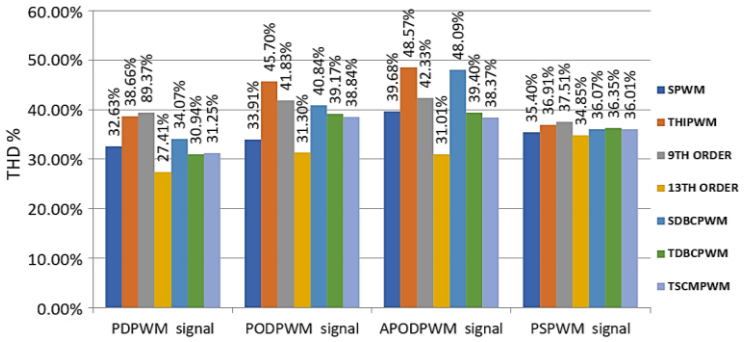

Figure 8. Comparison of %THD of output voltage for PWM1

Table 3. PWM1 fed ANPC inverter peak voltage across switch

Reference waveform	Method	Peak voltage across each IGBT (volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM signal	887	878	870	909	871	879
	PODPWM signal	794	792	791	804	791	792
	APODPWM signal	854	804	790	804	791	804
	PSPWM signal	854	805	798	864	798	805
THIPWM	PDPWM signal	1,018	958	939	1,033	940	958
	PODPWM signal	985	920	921	983	922	920
	APODPWM signal	855	841	827	866	827	841
	PSPWM signal	1,210	929	905	943	908	929
9TH ORDER	PDPWM signal	1,001	916	918	987	919	917
	PODPWM signal	860	824	784	803	787	824
	APODPWM signal	1,057	872	842	914	845	872
	PSPWM signal	920	868	804	835	807	868
13TH ORDER	PDPWM signal	943	882	890	944	891	882
	PODPWM signal	1,017	912	872	895	875	912
	APODPWM signal	1,085	946	894	898	898	947
	PSPWM signal	1,294	1,012	905	973	909	1,012
SDBCPWM	PDPWM signal	855	817	787	821	789	817
	PODPWM signal	855	810	790	792	793	810
	APODPWM signal	841	821	814	846	814	821
	PSPWM signal	908	967	973	849	804	870
TDBCPWM	PDPWM signal	868	874	926	833	818	874
	PODPWM signal	954	865	858	944	858	865
	APODPWM signal	837	793	797	832	793	793
	PSPWM signal	1,247	1,409	1,458	1,104	933	1,047
TSCMPWM	PDPWM signal	829	823	793	809	796	823
	PODPWM signal	859	825	794	815	797	825
	APODPWM signal	848	818	795	806	798	818
	PSPWM signal	908	860	800	837	800	860

4.2. PWM2 fed ANPC inverter output voltage, THD and peak voltage across switch

Figures 9, 10, and Table 4 show that lowest voltage THD obtained is 30.35% with carrier signal in PDPWM mode and reference signal in 3rd harmonic injection method with rms output voltage 1018 V and the peak voltage across the entire switching device is less than 1200 V. The highest rms voltage obtained by carrier signal in PSPWM carrier signal with SPWM type reference signal. From the PWM1 and PWM2 techniques, based on the extensive experimental data comparing 7 modulation techniques and 4 carrier signals across different performance metrics, the following technical discussions are drawn in Tables 5 and 6.

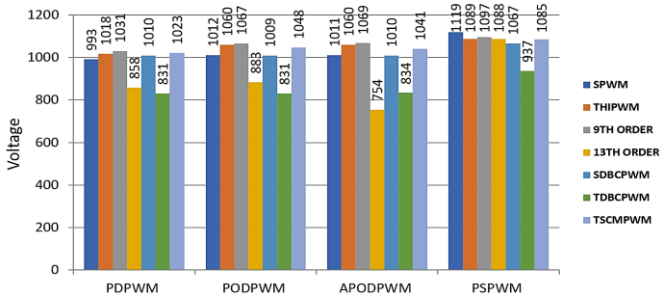

Figure 9. Comparison of RMS output voltages for PWM2

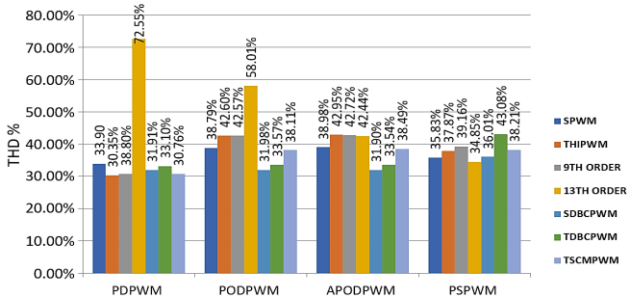

Figure 10. Comparison of %THD of output voltage for PWM2

Table 4. PWM2 fed Inverter output voltage, THD and Peak voltage across switch

Reference waveform	Method	Peak voltage across each IGBT (volt)					
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
SPWM	PDPWM signal	855	922	1,441	832	807	867
	PODPWM signal	853	899	982	845	808	837
	APODPWM signal	854	835	1,029	845	806	835
	PSPWM signal	915	991	1041	1,059	790	794
THIPWM	PDPWM signal	790	791	776	798	779	791
	PODPWM signal	790	791	779	799	779	791
	APODPWM signal	790	790	778	798	778	790
	PSPWM signal	798	875	943	887	747	875
9TH ORDER	PDPWM signal	786	783	768	797	770	783
	PODPWM signal	812	981	1022	811	789	789
	APODPWM signal	787	781	769	794	770	781
	PSPWM signal	953	1,122	1,306	1,076	782	885
13TH ORDER	PDPWM signal	797	787	1,071	789	798	787
	PODPWM signal	823	803	1,349	813	801	804
	APODPWM signal	793	788	1,062	790	789	788
	PSPWM signal	783	1,951	1,183	884	775	980
SDBCPWM	PDPWM signal	834	978	1,050	839	826	823
	PODPWM signal	831	1,017	1,074	833	819	822
	APODPWM signal	894	1,192	1,175	890	824	847
	PSPWM signal	737	1,943	1,897	899	762	1,042
TDBCPWM	PDPWM signal	813	807	812	806	813	804
	PODPWM signal	915	857	1070	1,086	855	858
	APODPWM signal	918	867	993	855	900	861
	PSPWM signal	830	1328	1,053	960	678	1,056
TSCMPWM	PDPWM signal	868	832	1,383	893	836	832
	PODPWM signal	868	833	1,398	892	820	833
	APODPWM signal	832	1,388	1,517	818	826	825
	PSPWM signal	945	2,240	1,322	1144	785	1,052

Table 5. Comparative analysis for 3 level ANPC inverter with PWM1 techniques

Priority of application	Suggested method	Performance indicator
THD	13th-order + PDPWM	THD = 27.41%, RMS = 1051 V,
Max RMS voltage	PSPWM (any modulation)	RMS = 1141 V (9th/13th/TDBCPWM)
Peak voltage across device performance (switching device reliability)	SPWM + PDPWM	Peak voltage across IGBT≤909 V, THD = 32.63%
Overall balanced performance	13th-order + PODPWM	THD = 31.30%, RMS = 1065 V, IGBT ≤ 1017 V
When operated on 1200 V switching device the failure possibilities higher in	SDBCPWM + PODPWM	RMS = 794 V, THD = 48.09%

Table 6. Comparative analysis for 3 level ANPC inverter with PWM2 techniques

Priority of application	Suggested method	Performance indicator
THD	THIPWM + PDPWM	Best THD (30.35%) + safe IGBT stress (776–798 V)
Max RMS voltage	SPWM + PSPWM	Max RMS (1119V)
Peak voltage across device performance (switching device reliability)	9th ORDER-PDPWM	Balanced THD (30.80%) + RMS (1031 V) + IGBT stress ≤ 797V
Overall balanced performance	THIPWM + PDPWM	THD: 30.35% (2nd lowest), RMS = 1018V, peak voltage across IGBT ≤ 798 V (safest)
When operated on 1200 V switching device the failure possibilities higher in	13th-order ANY carrier + PSPWM	THD > 42%, voltage instability

5. CONCLUSION

A comparative analysis of the components used for various topologies for a three-level inverter used in a 1500 V DC bus system has been conducted, and the results show that the ANPC inverter offers more benefits than the other topologies. Several reference signals have been compared for a three-level ANPC inverter using PSIM software, and the simulation is run using a trapezoidal signal with a different phase shift as the carrier signal. These PWM techniques compare the peak voltage across the switching device, the rms value of the output phase voltage, and the percentage THD value of the output phase voltage to analyze the performance of the three-level ANPC inverter. The simulation results show that comparison of PWM1 and PWM2 techniques for 3 level ANPC inverter that the application priority has a significant influence on the PWM strategy choice. 13th-order + PODPWM (PWM1) and THIPWM + PDPWM (PWM2) are notable for their overall balanced performance, providing a good trade-off between THD, RMS voltage, and switching device stress. Importantly, because of high THD (>42%) and voltage instability, the inverter is more likely to fail when using 1200 V-rated IGBTs with SDBCPWM + PODPWM (PWM1) and 13th-order + PSPWM (PWM2). PSPWM (PWM1) is favored when optimizing RMS output voltage is the top concern, whereas THIPWM + PDPWM (PWM2) is the most balanced and dependable method for real-world applications. Importantly, because of high THD (>42%) and voltage instability, the inverter is more likely to fail when using 1200 V-rated IGBTs with SDBCPWM + PODPWM (PWM1) and 13th-order + PSPWM (PWM2). PSPWM (PWM1) is favored when optimizing RMS output voltage is the top concern, whereas THIPWM + PDPWM (PWM2) is the most balanced and dependable method for real-world applications.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [MNP], upon reasonable request.

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