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Trapezoidal PWM scheme for voltage gain inverter

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ABSTRACT

The trapezoidal modulating wave-based high voltage gain 9-level inverter (HVG9LI) addresses significant difficulties related to the growing usage of capacitors, DC sources, and semiconductor switches. The proposed HVG9LI generates a nine-level resultant voltage with few components, exhibiting the capacity to double the output voltage gain. Furthermore, the HVG9LI utilizes a trapezoidal modulating wave and variable frequency carrier (TM-VFC) pulse width modulation method to increase the resulting voltage and enhance the voltage output quality. The performance and practicability of the HVG9LI with TM-VFC are evaluated across several modulation techniques and indices implemented by using MATLAB/SIMULINK and tested experimentally.

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1. INTRODUCTION

Multilevel inverters (MLIs) produce high-quality output voltages with low total harmonic distortion (THD), enhanced efficiency, and scalability to renewable and industrial applications, making them essential in current power electronics. The research community has improved MLI topologies, modulation methods, and hardware improvements for high-performance power conversion devices. This page discusses current MLI design, pulse width modulation (PWM), and application advances from several research. New inverter topologies have enabled greater voltages with fewer switches and simplified circuits. In [1], a low component count generates AC voltages efficiently, streamlining architecture and boosting dependability. Effectively incorporates 1:2:4 binary ratios to reduce circuit complexity and increase power quality [2]. Additional advancements in high-performance output using binary input combinations are shown [3]. Trinary source-based inverters provide modularity, scalability, and component reduction [4], [5]. Optimized inverter designs for high-performance motor applications are also stressed in [6], [7]. MLIs are also suitable for industrial and motor drive systems since trinary DC source asymmetrical inverters can power induction motor drives [8]. MLI performance has improved because to advanced PWM approaches. In boosting inverter setups, harmonic suppression and energy utilization are beneficial [9], [10]. Modularity and waveform enhancement are highlighted by the modular seven-level inverter (M7LI) with level-shifted variable frequency control [11], [12]. The improved structure inverter reduces on-state switches to improve reliability and power losses [13]-[15]. Low THD and better switching loss control make the hybrid PWM scheme appropriate for high-frequency applications [16]. Additionally, reconfiguring inverters using trapezoidal PWM improves solar waveform quality [17]. The analysis of symmetric multilevel inverters using unipolar PWM shows that MLIs may reduce THD and boost solar energy system efficiency [18]. The dual source inverter generates polarity and reduces device count, making it efficient for renewable energy and motor driving applications [19].

In [20]-[22], component reduction methods and multicarrier PWM are shown to be beneficial. Finally, improved carrier-level PWM techniques for power quality enhancement in inverters demonstrate the latest harmonic mitigation and voltage profile improvements in power distribution systems [23]-[25]. These studies demonstrate multilevel inverter technology advances in topology design, modulation, and component optimization. The HVG9LI inverter uses trapezoidal modulating wave-based PWM.

2. NINE LEVEL EIGHT SWITCHES MLI CIRCUIT

2.1. Explaining circuit topology and operation principles

i) Reduced active components: The design minimizes the number of active components by incorporating only a single input, Vin, as shown in Figure 1, and employing just eight power transistors. This simplification contributes to a more streamlined system.
ii) Simplified control logic: The control logic is streamlined through the use of complementary switching pairs (Si, Si') ranging from 1 to 4. The use of a NOT gate to derive signals for one switching pair reduces the controller's requirement to four independent control signals. This approach enhances the simplicity of the control logic.
iii) Natural capacitor balance: The system achieves inherent voltage balance among supercapacitors C1 and C2, aligning with the magnitude of Vin. Additionally, the voltage across floating capacitor C3 naturally maintains a level of 0.5 Vin. This self-regulating voltage balance eliminates the need for sensors or auxiliary control algorithms, contributing to a further simplification of the control process.
iv) Improved output capabilities: The system exhibits a twofold voltage gain, enabling the attainment of a nine-level output. This showcases enhanced boost and multilevel output capabilities, ultimately elevating the overall performance of the configuration.

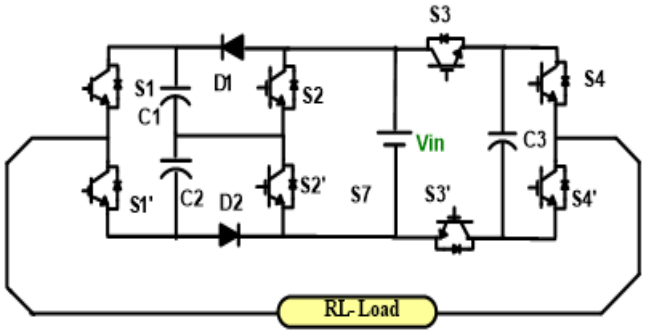


Figure 1. Topology of proposed HVG9LI circuit

2.2. HVG9LI working mode

The proposed topology's operational states for the positive and negative half cycles are shown. Table 1 lists the four transistors' switching states while taking switching pairs' complementary actions into account. This section deals the three-bridge switched-capacitor inverter (TBSCI) operations, focusing on the positive half cycle and assuming a pure resistive current condition. The voltage across C1/C2 stays at Vin whereas the voltage across C3 stays at 0.5 Vin under continuous circumstances. When Level 0.5 is attained, S2' is activated, which causes diode D1 to conduct forward. Consequently, the voltage across capacitor C1 (SC C1) is parallel to the DC source and constrained to the amplitude of Vin. S1, S3, and S4 are engaged simultaneously when the floating capacitor C3 in the load current channel is discharged and placed into forward series, producing an output voltage of 0.5 Vin. Level 1 eliminates the need for the floating capacitor C3 by alternating between turning S3 on and off. Vin is the voltage output that is produced when the load-current path includes the DC source in this setup by turn on S1', S2', S3', and S4'. Upon reaching Level 1.5, D2 conducts ahead due to S2 activation. Consequently, SC C2's amplitude is clamped to Vin and linked in parallel to the DC source. In the meantime, the ON states of S1', S3', and S4' result in an output voltage of 1.5 Vin. Furthermore, capacitors C1 and C3 are discharging because they are positioned in forward series within the load current path. Level 2 is where S3 is turned on and then turned off. A total output voltage of 2 Vin is obtained by connecting C1 directly in series with the DC supply by turn on S1', S2', S3', and S4'. S2' is activated, and D2 is forward conducting at Level −0.5. When its amplitude is limited to Vin, switch capacitor C2 is placed in parallel with the DC source. In this mode, the DC source appears in reverse series while the floating capacitor C3 is in forward series along the load current path, with S1', S3', and S4'

switched on. C3 is charging, the output current is inverted, and the overall output voltage is -0.5 Vin. The remaining levels in the negative half cycle are subject to the same rules. The operation maintains symmetry in the negative half cycle since C1 and C2 are connected in series with the DC source throughout a cycle. The suggested TBSCI architecture provides a twofold voltage increase in terms of boost and multilevel output, and it produces a nine-level output. This feature increases the inverter's versatility and functionality while also improving its overall performance. TBSCI circuit architecture has several benefits, such as reduced active components, simplified control logic, integrated capacitor voltage balance, and the ability to produce a multilevel output in addition to boost. When combined, these characteristics raise the stability and efficiency of the suggested inverter design.

Table 1. HVG9LI on and off state condition

Level	2	1.5	1	0.5	0	-0.5	-1	-1.5	-2
S1	1	1	1	1	1	0	0	0	0
S1’	0	0	0	0	0	1	1	1	1
S2	1	1	0	0	0	1	1	0	0
S2’	0	0	1	1	1	0	0	1	1
S3	0	1	0	1	1	1	1	1	1
S3’	1	0	1	0	0	0	0	0	0
S4	0	0	0	0	1	0	1	0	1
S4’	1	1	1	1	0	1	0	1	0

3. TM-VFC PWM TECHNIQUE

This approach involves the utilization of a rectified trapezoidal reference and a triangle carrier to initiate an m-level inverter. Figures 2(a) to 2(d) show the process entails employing carriers with matching frequencies and identical magnitude carriers, wherein the modulating waveform undergoes continuous comparison with the reference wave. Through logic circuits, basic driving pulses are derived, leading to the generation of corresponding switching pulses.

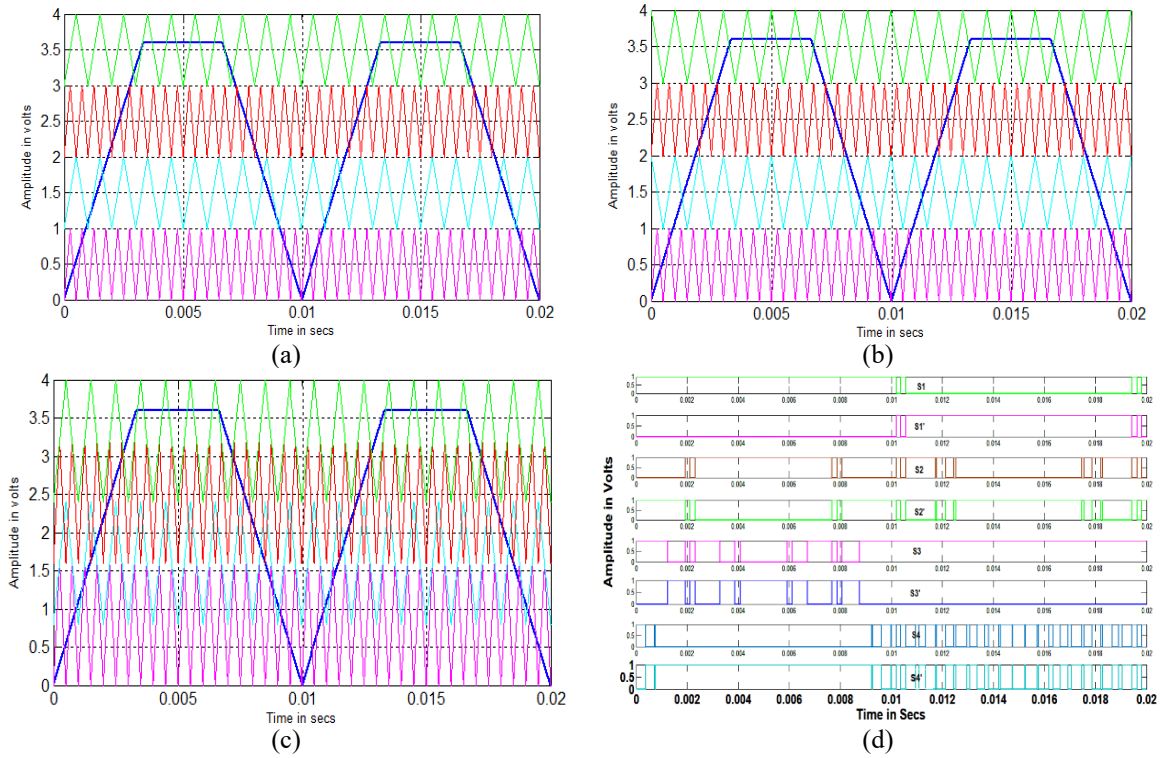
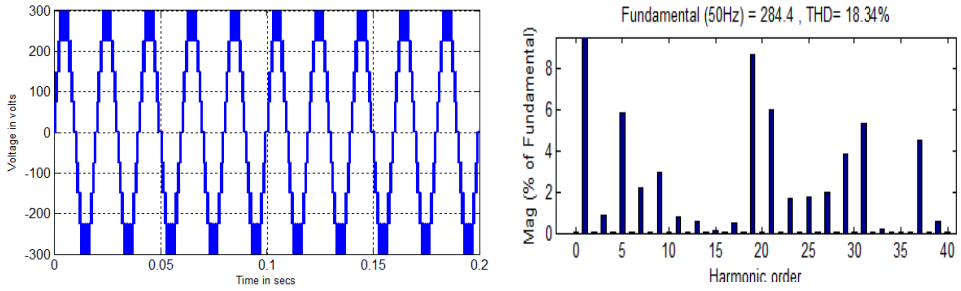


Figure 2. Use of the trapezoidal-based PWM technique: (a) PD, (b)APOD, (c) CO multicarrier waveform, and (d) pulse waveform

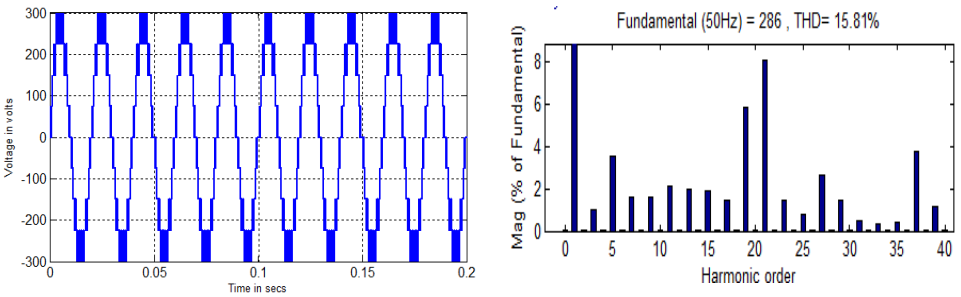
4. FINDINGS OF HVG9LI

Conducting the performance verification of HVG9LI arrangement using the TM-VFCPWM method and simulating it in MATLAB/SIMULINK is a crucial step. The resulting output is a 9-level waveform with voltage levels of 0, ±75, ±150, ±225, and ±300. For the simulation, the input parameters are taken as V = 150 Vdc and an R-load of 100 ohms. As illustrated in Figures 3(a) and 3(b), the HVG9LI produces a 9-level output waveform along with the corresponding voltage harmonic spectrum at a modulation index (MI) of 0.9. The obtained waveform shows a THD of 18.34% and delivers a maximum fundamental voltage of 284.4 V. Dominant harmonic orders are observed at the 5th, 19th, 21^{st,} and 31st positions. Moving to Figures 4(a) and 4(b) for MI 0.9 with TM-VFCAPODPWM, the HVG9LI waveform and spectral response display a peak voltage magnitude of 286 V and a THD of 15.81%. The 19th and 21st harmonic orders remain prominent. Figures 5(a) and 5(b) illustrate HVG9LI outcomes for MI 0.9 with TM-VFCCOPWM, achieving a maximum fundamental voltage of 294.8 V with a THD of 21.26%. Notably, the 5th, 19th, 21st, 31st, and 37th harmonics dominate. Table 2 shows that a modulation index of 1, when using TM-VFCAPODPWM, provides a better harmonic spectrum than the other modulation indices. From Table 3, its observed that TM-VFCOPWM yield better voltage profile. Table 4 reveals that distortion factor is less in TM-VFCAPODPWM techniques compare to all PWM.



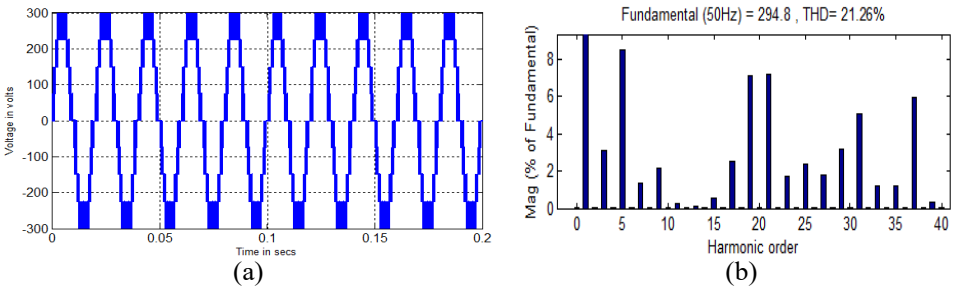
(a) (b)

Figure 3. Performance characteristics of TM-VFCPDPWM: (a) resultant voltage - TM-VFCPDPWM and (b) analysis of the voltage FFT (modulation index 0.9)



(a) (b)

Figure 4. Performance characteristics of TM-VFCAPODPWM: (a) resultant voltage TM-VFCAPODPWM and (b) analysis of the voltage FFT (modulation index 0.9)



(a) (b)

Figure 5. Performance characteristics of TM-VFCOPWM: (a) resultant voltage TM-VFCOPWM and (b) analysis of the voltage FFT (modulation index 0.9)

Table 2. % THD for various modulation indices

ma	PD	APOD	CO
1	13.33	10.55	17.56
0.95	16.74	13.82	19.64
0.9	18.34	15.81	21.26
0.85	17.59	16.94	22.64
0.8	16.21	17.80	23.91

Table 3. VRMS for various modulation indices

ma	PD	APOD	CO
1	224.7	220.1	316.6
0.95	213.3	211.1	305.6
0.9	201.1	202.2	294.8
0.85	186.9	191.8	283.3
0.8	176.4	180.2	270.1

Table 4. Distortion factor for various modulation indices

ma	APOD	PD	CO
1	0.0019745	0.0012005	0.0040894
0.95	0.0023806	0.0012579	0.0045327
0.9	0.0026135	0.0018558	0.0048284
0.85	0.0029036	0.0021869	0.0055815
0.8	0.0028285	0.0019272	0.0063756

This section describes the experimental results obtained with the SPARTAN-3 FPGA platform for the HVG9LI. Since FPGAs generally incorporate built-in PWM controllers, the implementation process becomes straightforward. Therefore, real-time execution of the selected inverter using FPGA has been carried out in this study. The TM-VFCPWM technique for the chosen inverter, employing a trapezoidal reference that demonstrated superior performance in simulations, was developed with the help of Xilinx System Generator software.

The gate-signal generator model, created with system generator, was compiled into a bitstream and loaded onto the FPGA for real-time execution. Using the FPGA implementation of the TM-VFCPWM strategy, the nine-level output voltages of the HVG9LI were realized, and the corresponding metrics—THD, fundamental RMS voltage (VRMS), percentage efficiency, and distortion factor (DF)—were measured and evaluated. Figure 6 illustrates the laboratory setup developed for the HVG9LI. In Figures 7(a) and 7(b), the inverter produces a nine-level waveform and its accompanying voltage harmonic spectrum at a modulation index of 0.9.

The produced voltage waveform exhibits a THD of 20.34%, with a maximum fundamental voltage of 264.2V. Dominant harmonic orders are observed at the 15th and 21st orders. Moving to Figures 8(a) and 8(b) for MI 0.9 with TM-VFCAPODPWM, the HVG9LI waveform and spectral response display a peak voltage magnitude of 266.2 V and a THD of 17.81%. The 15th and 21st harmonic orders remain prominent. Figures 9(a) and 9(b) illustrate HVG9LI outcomes for MI 0.9 with TM-VFCCOPWM, achieving a maximum fundamental voltage of 284.8 V with a THD of 23.26%. Notably, the 15th and 21st harmonics dominate. From Table 2, the complete examination reveals that a modulation index of 1 with TM-VFCAPODPWM yield superior harmonic spectrum in comparison with the other modulation indices. From Table 3, its observed that TM-VFCOPWM yield better voltage profile. Table 4 reveals that distortion factor is less in TM-VFCAPODPWM techniques compare to all PWM. Table 5 shows the distortion factor for various modulation indices implemented in the HVG9LI.

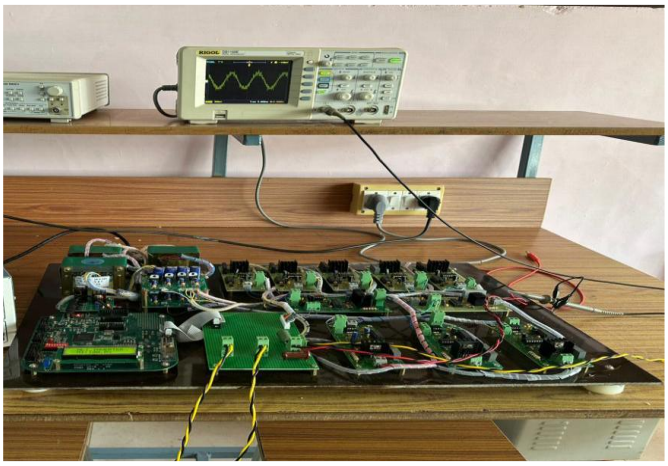
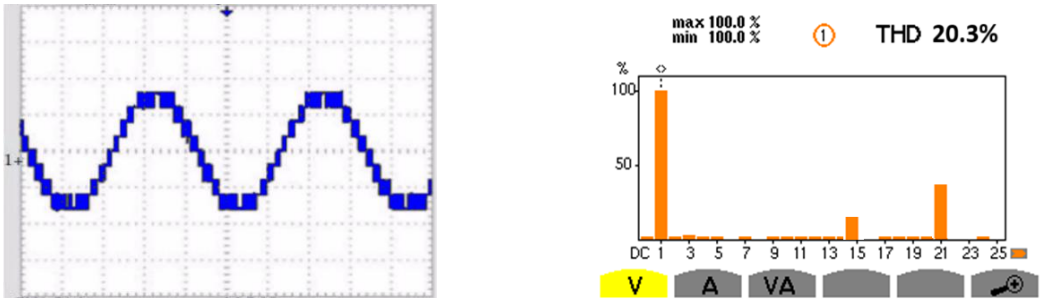
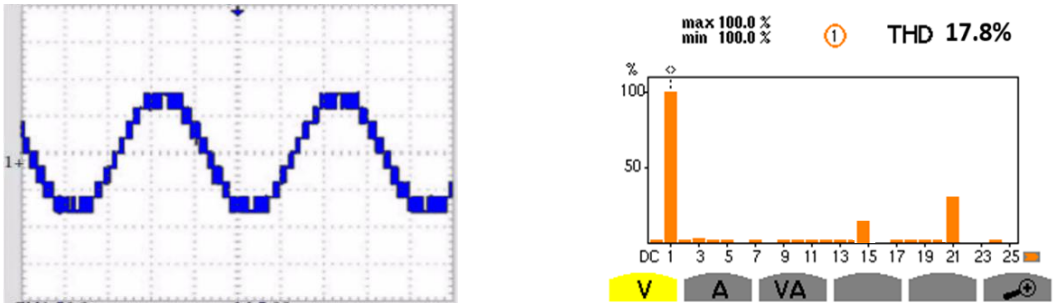


Figure 6. HVG9LI laboratory setup



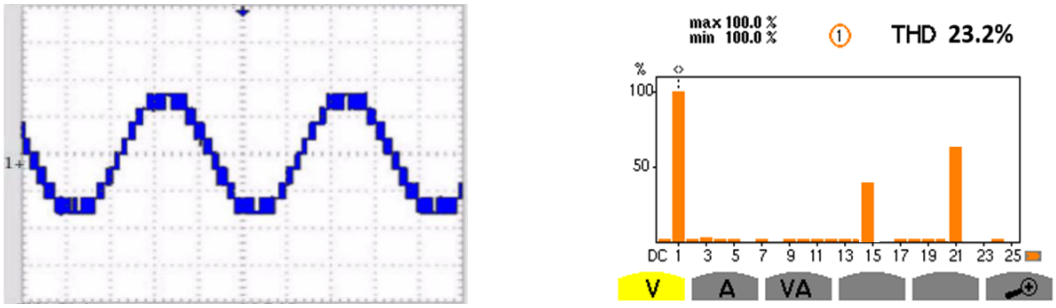
(a) (b)

Figure 7. Performance characteristics of TM-VFCPDPWM: (a) experimental resultant voltage - TM-VFCPDPWM and (b) analysis of the voltage FFT (modulation index 0.9)



(a) (b)

Figure 8. Performance characteristics of TM-VFCAPODPWM: (a) experimental resultant voltage - TM-VFCAPODPWM and (b) analysis of the voltage FFT (modulation index 0.9)



(a) (b)

Figure 9. Performance characteristics of TM-VFCOPWM: (a) experimental resultant voltage - TM-VFCOPWM (b) analysis of the voltage FFT (modulation index 0.9)

Table 5. Distortion factor for various modulation indices

ma	PD	APOD	CO
1	0.003095	0.001393	0.005209
0.95	0.003501	0.00145	0.005653
0.9	0.003734	0.002048	0.005948
0.85	0.004024	0.002379	0.006701
0.8	0.003949	0.002119	0.007496

5. CONCLUSION

This paper introduces a TM-VFCPWM for HVG9LI with minimal components designed to achieve a nine-level output. Additionally, a TM-VFCPWM approach uses PD, APOD, and CO strategies and has been implemented in the HVG9LI to improve the quality of the resulting voltage. The effectiveness of the suggested topology is illustrated through a simulation and laboratory configuration, where essential characteristics such as %THD, root mean square (RMS), and distortion factor are assessed. The utilization of

the TM-VFCAPOD PWM technique with a modulation index (ma) of 1 lead to an improved voltage THD of 10.55% and low distortion factor. TM-VFCOPWM technique with provides the highest DC bus utilization. The simulation and laboratory outcomes confirm the efficacy and feasibility of the suggested HVG9LI.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Harikrishna Naraboyana	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	
I. Kumaraswamy	✓	✓				✓		✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

DATA AVAILABILITY

Data availability is not applicable to this paper as all data generated or analyzed are fully included in the manuscript.

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