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Development of 15/33 level constant and variable DC source inverter for different loading conditions

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ABSTRACT

In this paper, a design of symmetric and asymmetric multilevel inverter (MLI) with few quantities of switch is presented. The structure can be able to operate with both symmetric and asymmetric sources. The presented model is capable of producing output levels of 15 with symmetric structure and 33 with asymmetric structure. The tendered circuit is constructed with 14 switches and 7 sources. The presented MLI can be placed in moderate-voltage applications such as: electrical machine drives. The circuit's switching sequences are framed by a detailed discussion from its operation. In MATLAB/Simulink, the inverter is simulated for resistive, resistive-inductive, and induction motor loads, and the results are portrayed. Also, the working of the inverter is monitored in terms of harmonics presence in the load signals. Additionally, the presented MLI is developed in real time to evaluate its performances. The results obtained from the real time inverter are found satisfactory.

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1. INTRODUCTION

Present days, a numerous industrial application needs high power. Besides, few industrial components need medium or low power to operate. Certain industrial loads required a lot of power may benefit from using a high-power source, while other loads may suffer as a result. Since its introduction in 1975, the multilevel inverter (MLI) has served as a high power and medium voltage option. In high power and medium voltage scenarios, the MLI is employed in industrial applications as a substitute [1].

Because of its enhanced voltage and current waveforms, the MLI are popular in high power, and power quality-challenge applications. Also, the MLIs have revolutionized the field of power electronics due to higher operating voltage capability, decreased voltage stress and voltage harmonic components, fault-tolerant operation, and improved efficiency. Advancement of multi-level inverters is currently in vogue which includes wind energy, electric vehicle technologies, and solar systems. A variety of circuit components which makes MLI that includes switches, diodes, and voltage sources [2], [3]. MLIs provide a few advantages over two-level inverters, including quality output power, voltage, and current. Also provides low total harmonic distortion (THD), switching loss, dv/dt, electromagnetic interference with improved efficiency. The MLI can also operate at high voltage and power levels [4]. An inverter is designed to generate twenty one voltage steps with less switching components connected to an impedance load [5]. Previous study [6] designed a 7-level inverter with a dual strategy to improve the linear modulation level. The study in [7] designed a 1-kW transformer-based MLI with bidirectional switches to produce 15 voltage levels at the load.

The study in [8] presented a new type of inverter, called the "WE" inverter, to increase the output voltage. In the presented work it is found that, operating the inverter with lower modulation index gives poor performance and it is proposed to operate the inverter with larger modulation index value.

Here, a flip MLI structure with ladder voltage steps is designed to produce 11 levels at the load. The inverter is designed in such a way; it utilizes the input voltage source in uniform manner to get balance in the voltage sources [9]. Previous study [10] introduced a new design for a 3-phase, 7-level inverter made with switched capacitors. The presented topology is more efficient and cost-effective due to RSC, voltage boost, and low voltage stress. Two different MLIs, such as cascaded and flying capacitor is combined in such way to produce 9 voltage steps at the load terminal is discussed [11]. Previous study [12] designed a nine-level inverter to reduce the voltage generation with that of power circuit components. Authors have analyzed the impact of loads on input voltages, and discussion is made on the influence of wide band gap devices on MLI performance [13]. The study in [14] evaluated the performance of a novel 15-level multilevel inverter (MLI) topology. This design utilizes only two direct current (DC) sources and focuses on achieving a lower standing voltage across the components.

Rivera and Babaei [15] propose a systematic placement strategy for level shifters to minimize the required number of components (9 switches and 3 DC sources) while ensuring robust operation of the inverter. A 13 voltage steps symmetric inverter [16] designed using diodes, capacitors, switches and dc sources with the quantity of 3, 1, 12 and 2 respectively. With the same quantity of circuit components, the proposed inverter is able to give 17 voltage steps when the dc sources are operated in asymmetric manner. From the above study, it is depicted that designing a multilevel inverter with fewer components count for dynamic loading condition is challenge one. Therefore in [17] a MLI which generates higher voltage level is designed for dynamic loading conditions using 14 power switches 7 DC sources is performed. Two symmetrical circuit structures, known as circuit-1 and circuit-2, are proposed in [18] and it has the ability to produce nine voltage levels at the load. The 11-level output, for example, reached a peak voltage of 145 V with a THD of 11.14%. Using asymmetric DC sources, without H-bridges, an MLI topology in [19] achieves a 25-level output voltage using just eleven switches in MATLAB/Simulink. A new switched capacitor module [20] is presented that eliminates the need for high-blocking-voltage switches by generating numerous inverter levels without the use of H-bridges. Reducing size and complexity [21]-[25], the inverter's functioning is further optimized by the use of novel pulse width modulation methods. From the above examination, it is seen that designing an inverter to produce higher voltage steps is possible by selecting fixed DC sources and variable DC sources. Conventional MLIs greatly involve a more number of switching components, leading to the development of new designs with fewer switches.

Majority research on MLI focuses on reducing THD, switching losses, and complexity. Some designs use asymmetric sources without H-bridges, leveraging pulse width modulation techniques to achieve high performance with fewer components. Therefore, in this article, a novel DC voltage clamping unit is presented, which is capable of producing a 3-voltage level using equal DC sources, and it is capable of generating a higher voltage level by selecting unequal voltage sources. The following are the contributions in this article:

- A novel MLI topology is designed with a reduced number of switches (9) and DC voltage sources (3), demonstrating a symmetric and asymmetric configuration.
- Optimized design enables efficient circuit modeling and operation for generating high-level outputs with fewer components compared to traditional topologies.
- Utilization of an edge control PWM technique for triggering, ensuring efficient and reliable switching operations.
- MATLAB/Simulink-based simulation for the proposed MLI is carried out, showcasing robust performance under different loads: resistive loads, RL loads, and induction motor loads.
- Hardware implementation using FPGA SPARTAN 6 controller validates the practical applicability of the design.

2. DESIGN OF MLI

In this section, an MLI design is presented which incorporates 14 unidirectional switches and 7 DC sources, allowing for both symmetric (equal voltage) and asymmetric (unequal voltage) setups. It employs a sinusoidal PWM technique for triggering, producing output waveforms with 15 and 33 levels. Each switch is connected to a driver circuit, and control pulses are generated by comparing a sine reference with logic-based circuits. In the symmetric configuration, the output ranges from 0 V to ±70 V, while the asymmetric setup with E4 to E6 set at 4 VDC-extends the output to ±64 V. The inverter can generate finely stepped voltage waveforms through various switch combinations, and the design work of the proposed structure is discussed here. The design structure of the proposed MLI configuration is shown in Figure 1 which consists of 14

switches (S1-S12') and 7 voltage sources (E1, E2, E3, E4, E5, E6, E7). Here, all the 14 switches are uni-directional in nature; consequently, the design circuit includes an identical driver circuit for its switches. A fundamental sinusoidal PWM method (Figure 2) was utilized to activate the design. The constructed MLI circuit incorporates both equal and unequal voltage sources, resulting in symmetric and asymmetric configurations. The pulses required for the switches are developed by utilizing a sine wave signal as a reference, along with a comparator to assess the reference wave with a gain, and a relational and logic circuit. These four components are depicted in Figure 2, as illustrated a sine wave serves as the reference. The reference wave's amplitude is set at 11 V, and it is chosen based on the positive and zero levels necessary for the MLI. This reference wave is fed into the comparator, and the comparator's output is then sent to the relational and logic circuit blocks. Here the relational operators are employed to compare the levels that need to be selected. For each level, a pair of relational operators and an AND gate is utilized to produce the pulses for the switches.

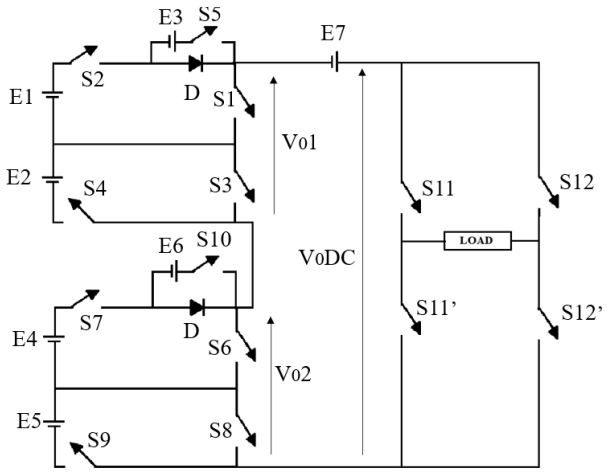


Figure 1. 15/33 level symmetric/asymmetric MLI

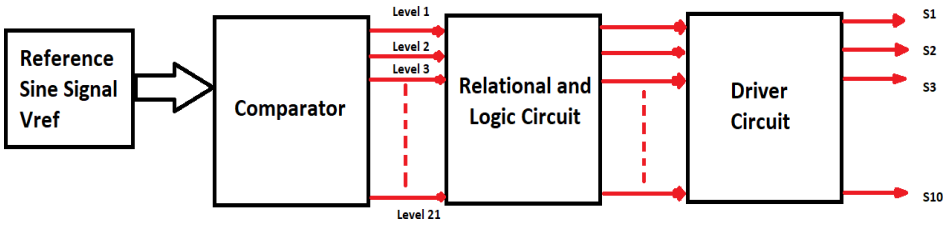


Figure 2. Generation of switching pulse (control circuit)

The working manner of 15 level symmetric (Figure 3) and 33 level asymmetric MLI is discussed here:

- Mode 1 – During this, S1, S3, S6, S8, S11, and S12 are turned 'on' and this path flow does not include any voltages since this mode gives the zero level which creates 0 V across the load.
- Mode 2 – During this, 'S1, S4, S6, S8, S11, and S12' are turned 'on' and the path flow includes sources E7, which create 10 V across the load.
- Mode 8 – During this, S5, S2, S4, S7, S9, S10, S11, and S12 are turned 'on' and the path flow includes sources E7 + E3 + E2+ E1+ E5+ E4+ E6, which create 70 V across the load.

Similarly, the negative voltage steps are produced with same switching concept in the basic unit with turn on state S12 and S11'.

Also, asymmetric voltage steps are generated by fixing the DC voltage as E1 = E2 = E3 = E7 = VDC, E4 = E5 = E6 = 4 VDC. To understand the switching of asymmetric inverter, here the working manner of the negative voltage generation is discussed:

- Mode 32 – During this, 'ON' state switches are S2, S4, S7, S9, S10, S11, S12, and the path flow includes sources E7 + E6 + E2+ E1+ E5+ E4, which create -60 V across the load and
- Mode 33 – During this, S2, S4, S5, S7, S9, S10, S12, and S11 are turned 'on' and the path flow includes sources E7 + E3 + E6 + E2+ E1+ E5+ E4, which create -64 V across the load.

In the design shown in Figure 1, the amplitudes of the voltage sources are E1 = .. = E7 = VDC, n ≥ 1. The highest value of load voltage and level count is given as (1)-(4).

$$V_0 = (3n + 1)\, V_{dc} \tag{1}$$

$$N_{level} = (6n + 3) \tag{2}$$

$$N_{switch} = (5n + 4) \tag{3}$$

$$N_{driver} = (5n + 4) \tag{4}$$

For the asymmetric topology, the DC sources are unequal as E1 = E2 = E3 = E7 = VDC, E4 = E5 = E6 = 4 VDC. The highest value of load voltage and level count is given as (5)-(8).

$$V_0 = (12n - 8)\, V_{dc} \tag{5}$$

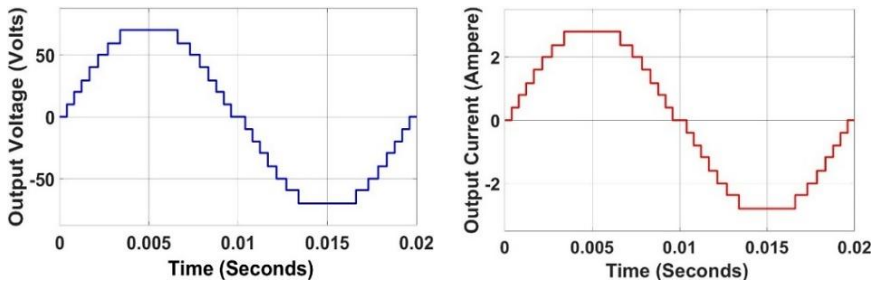
$$N_{level} = (24n - 15) \tag{6}$$

$$N_{switch} = (5n + 4) \tag{7}$$

$$N_{driver} = (5n + 4) \tag{8}$$

3. DISCUSSION OF RESULTS FROM SIMULATION STUDY

The circuit depicted in Figure 1 is designed using MATLAB/Simulink, and it is capable of generating 15 output levels when the DC source values are selected as E1 = .. = E7 = 10 V, and the designed inverter is tied with a resistive load of 25 Ω and output frequency as 50 Hz. The output waveform for R load is shown in Figures 3(a) and 3(b), and it is seen that 15 levels are achieved. The peak load voltage obtained is 70 V, with the output current is 2.8 A, and the THD obtained is 6.60%. The FFT analysis for the R load is shown in Figure 4, which gives the harmonics present in the load voltage.



(a) (b)

Figure 3. FFT-15-level MLI - R load: (a) load voltage and (b) load current

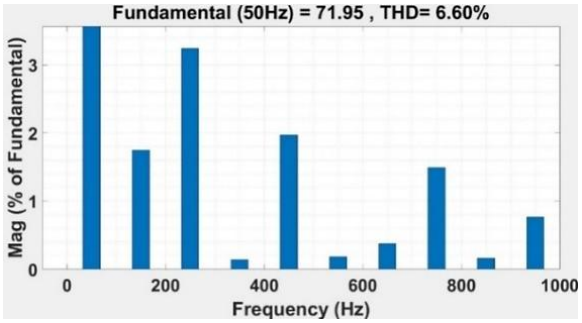


Figure 4. FFT-15-level MLI - R load

Similarly, the simulation work for 33 level inverter is carried out by tying the inverter with an impedance load of R = 25 Ω, L = 80 mH. For this inverter, the input voltages are selected as E1 = E2 = E3 = E7 = 4 V, E4 = E5 = E6 = 16 V. The output waveform for RL load is shown in Figures 5(a) and 5(b) from which it can be seen that we have achieved 33 levels, and the output peak voltage obtained is 64 V, the output current is 2.0 A and the THD of voltage obtained is 3.39%, respectively. The FFT analysis for the RL load is shown in Figure 6, which gives the harmonics in output voltage.

Further, the 33-level inverter is tied with an induction motor load, and the circuit specifications for the motor are given in Table 1, where the entire main winding and auxiliary winding impedance are specified. The induction machine (IM) considered is a 4 pole machine with power rating of 0.5 HP, and the input voltages are selected as E1 = E2 = E3 = E7 = 20 V, E4 = E5 = E6 = 80 V. Therefore, the 33-level is capable of producing ±320 V at the load terminal, and it is shown in Figure 7(a). The observed load torque is shown in Figure 7(b), and the main winding current is observed as ±6.9 A, which is shown in Figure 7(c), and speed is shown in Figure 7(d), respectively. The FFT analysis for the circuit tied with an induction motor load of 33-level inverter is done, and the voltage THD is obtained as 4.05 %. The designed inverter with IM load is subject to variable torque of 2 Nm at 3 seconds and 2.5 Nm at 6 seconds; the speed variations are observed and shown in Figure 7(e).

Considering the basic cycle, the output voltage is allowed to transition just once between neighboring levels. In the simulation analysis, a modulation index (M_a) of 1 is chosen for both 15-level symmetric and 33-level asymmetric inverter. If the modulation index exceeds one, the inverter moves into the over-modulation zone. This results in a quasi-square waveform at the load terminals, thus increasing THD. In addition, the performances of the proposed configurations are evaluated at modulation indices of 1.0 and 0.6, as depicted in Figure 8. For M_a = 0.6, the output shows fewer voltage steps compared to M_a = 1.0. For M_a = 1.0 all output voltage levels are distinctly achieved. This concludes that the inverter performs satisfactorily under various modulation indices (MI).

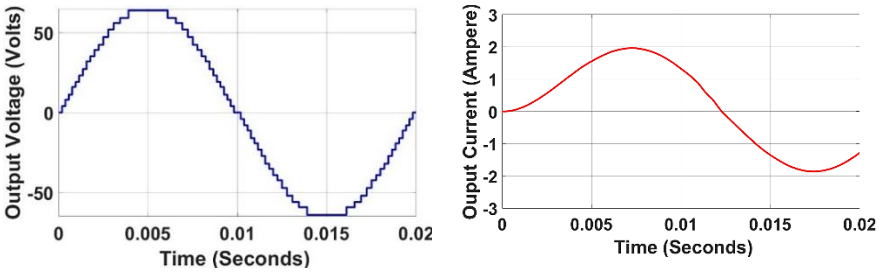


Figure 5. Load waveforms of 33 level asymmetric MLI: (a) load voltage and (b) load current

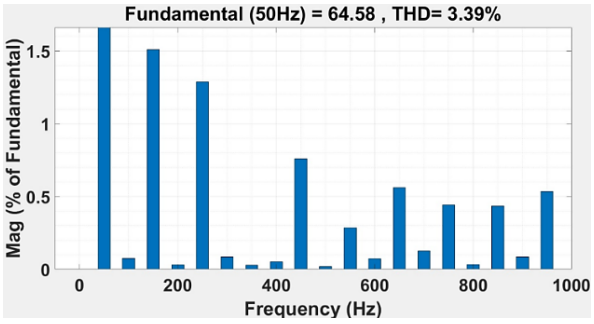


Figure 6. FFT- 33 level MLI – RL load

Table 1. Design parameters of IM load

Sl No	Parameter	Values
1	Power rating	0.5 HP
2	Rated speed	1480 RPM
3	Number of poles	4
4	Voltage rating	239 V
5	Current rating	7.2 A
6	Rated torque	2.4 Nm
7	Frequency	50 Hz

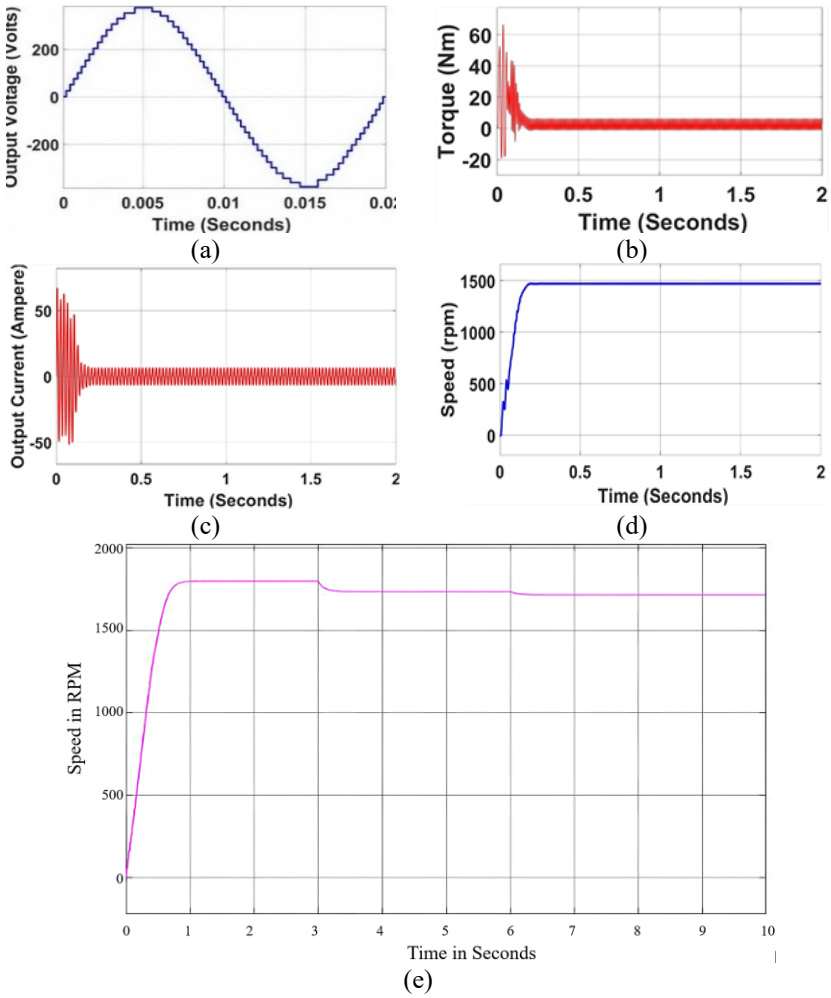


Figure 7. Load waveforms of 33 level asymmetric MLI fed to IM load: (a) IM load of 33-level inverter (voltage), (b) IM load of 33-level inverter (load torque), (c) IM load of 33-level inverter (main winding current), (d) IM load of 33-level inverter (speed), and (e) IM with variable load torque with speed change

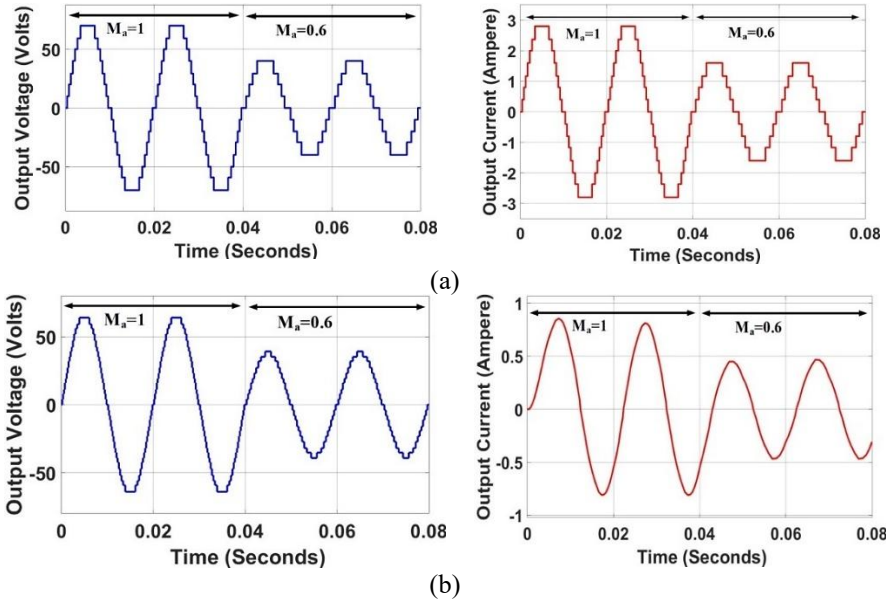


Figure 8. Change in MI-load waveforms: (a) 15 level MLI and (b) 33 level MLI

3.1. Assessment of parameters associated with the referred MLIs

The MLIs referenced from [14]-[19] were evaluated alongside the proposed converter (Pr) based on the number of switches, driver circuits, and DC voltage sources required to generate the specified voltage steps at the output. Additionally, the count of switches in the 'ON' state was analyzed. The parameters associated with these MLI circuits, along with those of the proposed third framework, are summarized in Table 2, and 'c' represents the number of cascading sections.

Table 2 has been expanded into graphical representations, with plots illustrated in Figures 9(a)-9(d). Figure 9(a) compares the references [14]-[19] based on the parameters N_{step}vsN_{switch}. Figure 9(b), which depicts the relationship between the number of driver circuits and voltage level generation, shows that the third framework requires fewer driver circuits than existing topologies. The topology examined in [15]-[19] requires a higher number of DC voltage sources than the proposed topology to achieve similar voltage levels at the output, as evidenced by Figures 9(c) and Table 2.

Table 2. Assessment of parameters associated with the referred MLIs

Reference No	N_{step}	N_{switch}	N_{driver}	$N_{on,sw}$	N_{source}	THD	Efficiency	TSV	No of capacitor & diode
[14]	15^c	$9c$	$9c$	$3c$	$2c$	-	95.7	40 V_{dc}	2C & 4D
[15]	$2(4^c-1)+1$	$7c+2$	$7c+2$	$2c+2$	$3c$	2.81	95.74	160 V_{dc}	-
[16]	$2(8^c)-1$	$12c$	$11c$	$5c$	$2c$	3	96.4	21.5 V_{dc}	3C & 3D
[17]	$2(3^c)-1$	$3c+4$	$3c+4$	$3c$	$2c$	1.88	95.56	-	-
[18]	$9c$	$9c$	$9c$	$4c$	$4c$	13.52	-	24 V_{dc}	-
[19]	$24c+1$	$16c$	$11c$	$3c$	$4c$	-	-	84 V_{dc}	-
Pr	$(24^c)-15$	$5c+4$	$5c+4$	$3c$	$3c$	3.39	96.25	19 V_{dc}	-

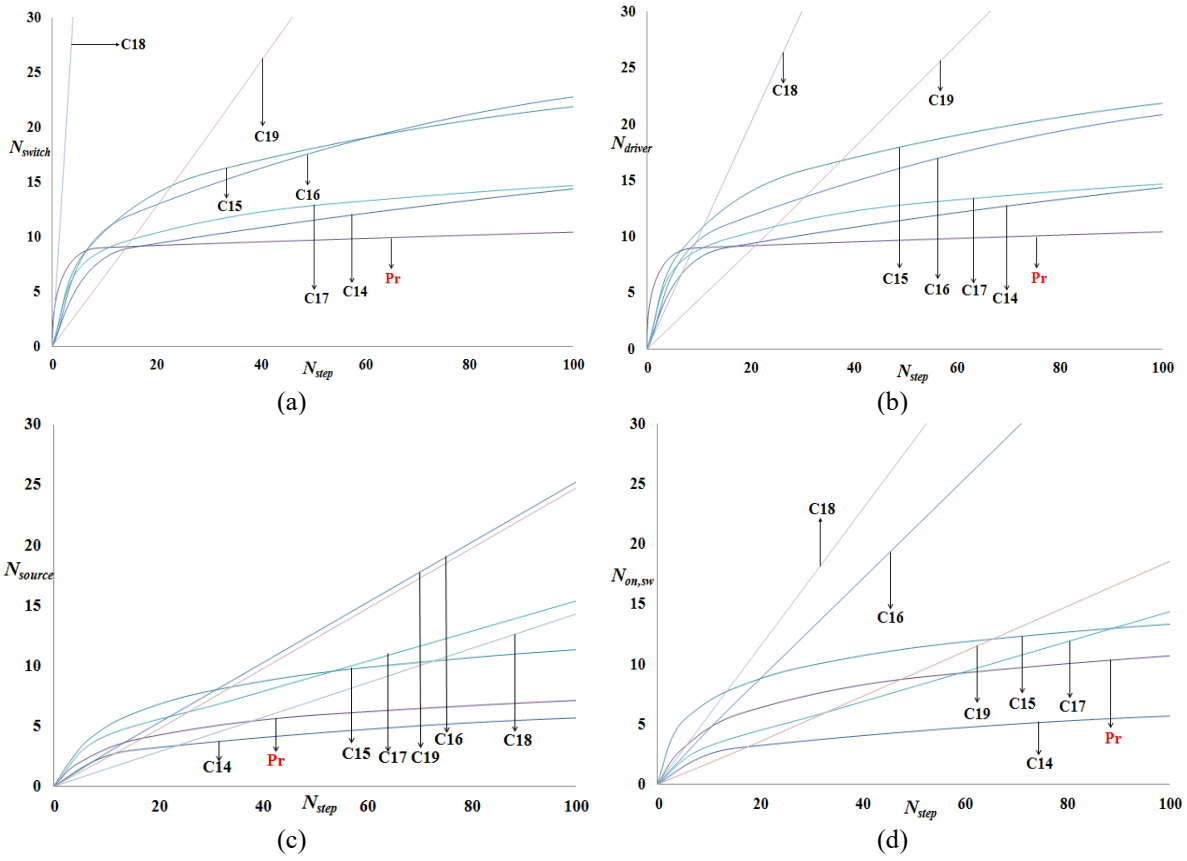


Figure 9. Assessment of parameters: (a) N_{step} vs N_{switch}, (b) N_{step} vs N_{driver}, (c) N_{step} vs N_{source}, and (d) N_{step} vs $N_{on,sw}$

This reduction contributes to both a smaller inverter size and lower cost. The plot in Figure 9(d) reveals that the proposed circuit achieves an optimal number of switches in the 'ON' state compared to other topologies. Based on this comparison, it can be concluded that the proposed MLI design shown in Figure 1, demonstrates superior performance compared to the other topologies analyzed. The newly suggested MLI

design was evaluated against existing configurations from references [14]-[19], concentrating on aspects like the number of switches, driver circuits, DC sources, and active switches during operation. These comparisons, as outlined in Table 2 and depicted in Figures 9(a)-9(d), underscore the proposed inverter's efficiency in terms of component usage. The provided Table 2 compares various MLI designs based on THD, efficiency, TSV, and the number of passive components used, such as capacitors and diodes.

Among the listed works, the lowest THD was observed in topology 17 (1.88%), whereas the proposed design (Pr) recorded a THD of 3.39%. However, the proposed inverter excels in efficiency, achieving the highest value of 96.25%, which is superior to other designs [14] (95.7%) and [16] (96.4%). In terms of TSV, the proposed structure operates at a lower value of 19 Vdc, reducing the voltage stress on the components. Unlike the works in [14] and [16], which require additional passive elements (2C & 4D and 3C & 3D, respectively), the proposed design avoids the use of extra capacitors and diodes, resulting in a simpler and more compact structure. This makes it an effective and efficient solution for inverter application. With a low THD of 3.39% and a high efficiency of 96.25%, the proposed MLI presents a more practical and high-performance alternative to existing configurations.

4. DISCUSSION OF RESULTS FROM REAL TIME IMPLEMENTATION

The input pulses for 15/33 level symmetric and asymmetric MLI are generated by FPGA controller. Here, for controller unit FPGA SPARTAN 6 is being used. The controller is coded using VHDL program based on the algorithm of fundamental frequency method. The input pulses are taken to the driver circuit for all the switches from S1 to S14. The hardware implementation of the 15-level symmetric MLI and 33-level asymmetric MLI is carried out using DC sources, FPGA controller unit and the driver circuit. The FPGA used to generate the gate pulse for the switches. The DC supply is split into 5 V and 15 V for FPGA SPARTAN 6 controller section and driver circuit (TLP250_DR), respectively. The program is dumped into the controller section, and using driver circuit the connections will be given to the IGBT's (15N120NDS_224) of 15 level symmetric and 33 level asymmetric MLI.

4.1. 15-level symmetric MLI for resistive and reactive load

The 15 level MLI is implemented in hardware (Figure 10) for feeding resistive load. The input voltage for 15 level multilevel inverter is implemented using symmetric DC sources where E1 = E2 = E3 = E4 = E5 = E6 = E7 = 10 V, load resistance value is kept as 25 Ω. The maximum output voltage is observed to be ±70 V, and output current is 2.8 A. The 15-level MLI load voltage and current waveform are shown in Figures 11 and 12. The 15 level MLI is implemented in hardware for feeding variable resistance load. The load resistance is decreased from 70 Ω to 40 Ω during the operation and change in load waveform with output current of 1 A to 1.75 A is shown in Figure 13.

4.1.1. Efficiency calculation of a 15-level inverter

The cause of the conduction loss (P_{cl}) in7 power switches are due to its internal resistance R_{in} during their on-state, and P_{cl} can be computed using (9).

$$P_{cl} = \sum_{j=1}^{14} R_{in}\ {I_{Out}}^2 \tag{9}$$

Turn-on power loss ($P_{swl,ON}$) and turn-off power loss ($P_{swl,OFF}$) are switching losses that constitute from the overlap of current and voltage across the switches during the transition of switching states, and it is computed from 10 to 13.

$$P_{swl,ON} = fs \int_0^{t_{on}} v(t)i(t)dt = fs(\frac{-Vb(t-t_{on})}{t_{on}}) \left(\frac{I_{out}}{t_{on}}t\right) dt = \frac{1}{6} fs\ V_{bl} I_{out} t_{on} \tag{10}$$

$$P_{swl,OFF} = fs \int_0^{t_{off}} v(t)i(t)dt = fs(\frac{-Vb(t-t_{off})}{t_{on}}) \left(\frac{I_{out}}{t_{off}}t\right) dt \tag{11}$$

$$P_{swl} = P_{swl,ON} + P_{swl,OFF} \tag{12}$$

$$P_{swl} = \sum_{j=1}^{14} fsj * Vbj * Iout * (ton + toff) \tag{13}$$

The cumulative power losses (P_{pl}) and efficiency are expressed as (14) and (15).

$$P_{pl} = P_{cl} + P_{swl} \tag{14}$$

$$\eta = \frac{P_o}{P_o + P_{pl}} [(P_o) \text{ is obtained from } V_{rms} * I_{rms}] \quad (15)$$

From the above equations, the efficiency of the 15 level MLI is obtained as 96.22% for 200 Ω resistive load.

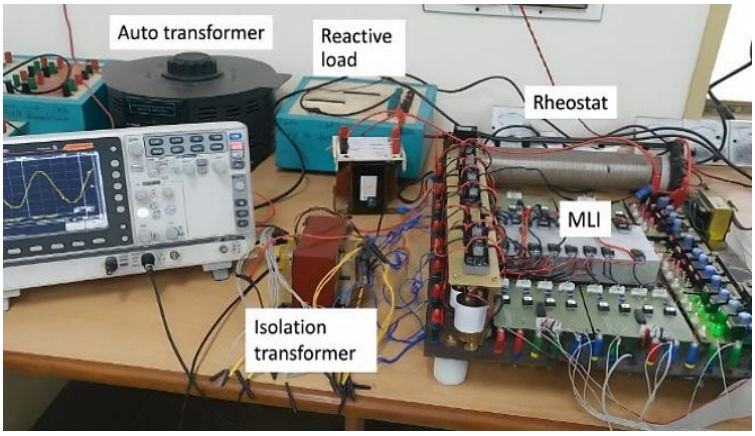


Figure 10. Hardware 15-level MLI

Figure 11. Output voltage - 15-level MLI – R load

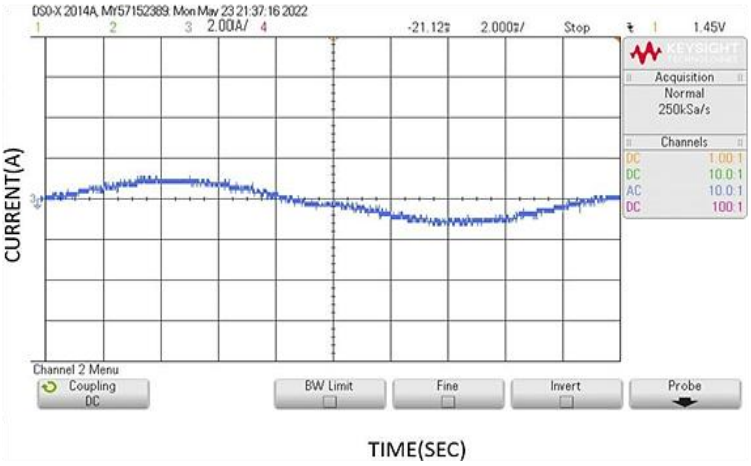


Figure 12. Output current- 15-level MLI – R load

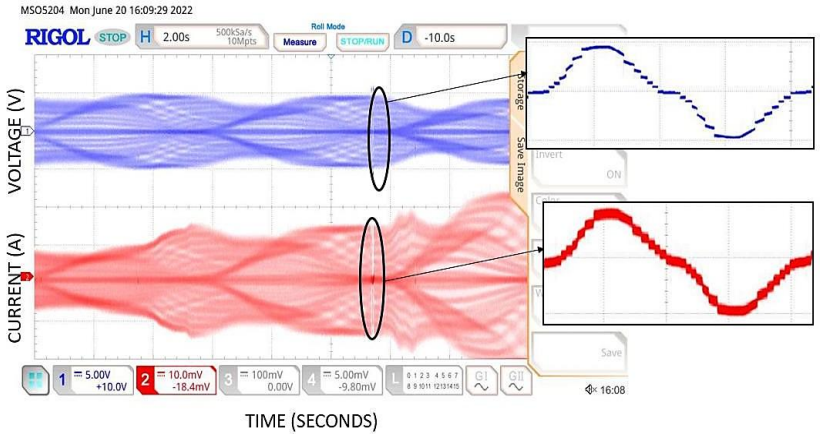


Figure 13. Load waveform - 15-level MLI-variable R load

4.2. 33-level asymmetric MLI for resistive and reactive load

The hardware implementation of 33 level MLI for reactive load (R = 25 Ω and inductance value at L = 80 mH) is shown in Figure 14. The maximum output voltage, current, and load THD are obtained as ±64 V, 2.0 A, and 4.22%, respectively. The 33 level MLI load voltage and current plots for the RL load are shown in Figure 15.

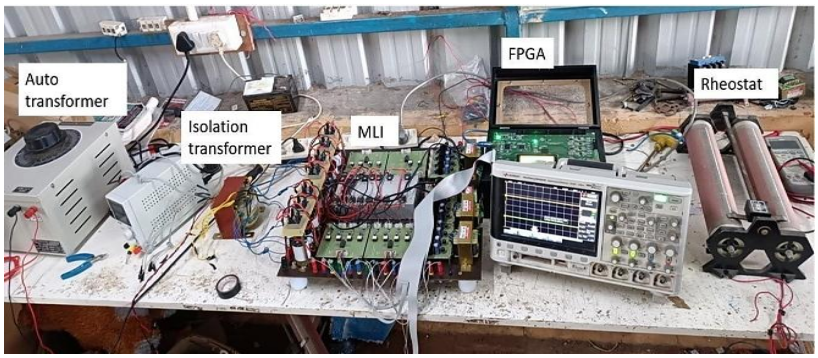


Figure 14. Hardware implementation - 33-level MLI

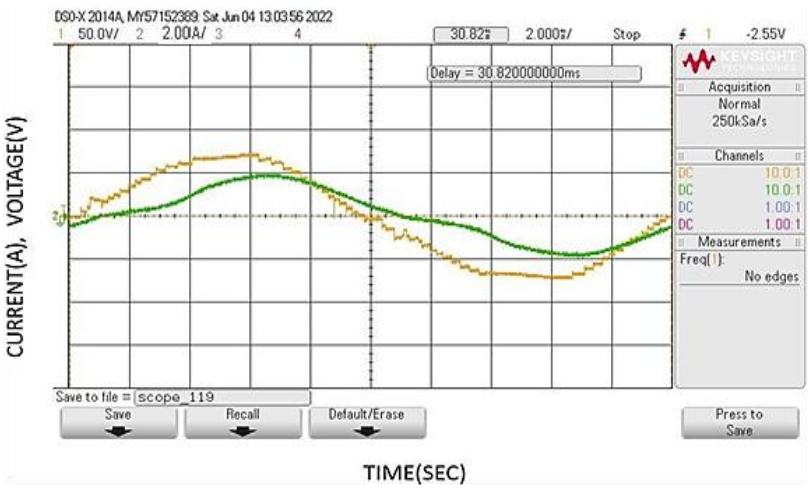


Figure 15. Load waveforms - 33-level MLI - RL load

The 33 level MLI is implemented in hardware for feeding variable RL load and the load resistance is decreased from 60 Ω to 40 Ω, and the inductance value is kept constant at 120 mH. The variation in the load waveform with observed values of 1.06 A to 1.6 A is shown in Figure 16. The implementation of 15-level symmetric and 33-level asymmetric multilevel inverters (MLIs) was carried out using an FPGA SPARTAN 6 controller, which generated gate signals through VHDL programming. For the 15-level MLI, uniform 10 V DC sources were employed, resulting in a peak output of ±70 V across resistive, RL, and variable loads, with a THD of 6.61%, 6.54%, and an efficiency of 96.22%. The 33-level MLI utilized unequal voltage sources of 4 V and 16 V, producing an output of up to ±64 V. It achieved lower THD values of 4.38% and 4.22% for resistive and RL loads, respectively. The load current adjusted with changes in resistance and impedance, confirming the system's flexibility and performance.

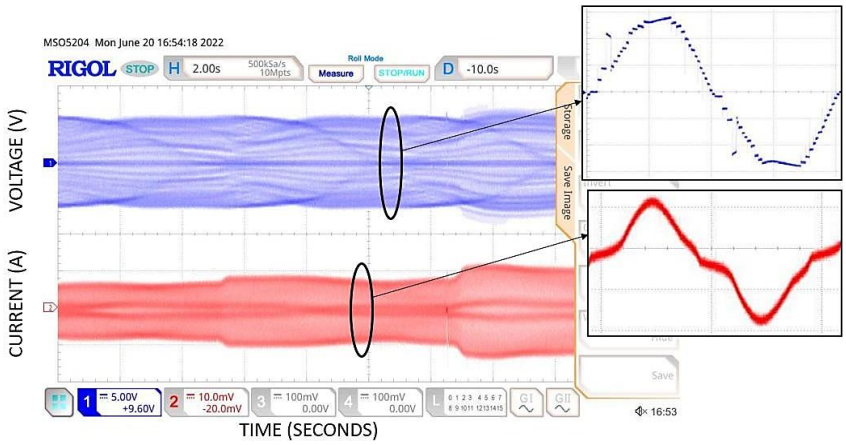


Figure 16. Load voltage and current waveform – 33-level MLI - variable Z load

5. CONCLUSION

The current work focuses on the design, simulation, and real-time implementation of two multilevel inverter topologies. The first topology utilizes symmetric DC sources to generate a 15-level output voltage, while the second topology employs asymmetric DC sources to achieve a 33-level output. The performances of the inverters are evaluated under variable load conditions, including fixed and variable R and Z loads, as well as an induction motor through MATLAB/Simulink. Real-time work of inverter is performed using SPARTAN 6 processor and it is tested for variable and fixed loading conditions. The results of the real time inverters are presented, and harmonic presence in load waveforms of 15 level symmetric and 33 level asymmetric for R and RL loads are given as 6.54% and 4.22%, respectively. The comparative analysis proves that the presented topology performs better than the referred works. Also, it is seen that the generation of higher voltage steps in the inverter leads to reduction in harmonic presence in the load waveforms. The proposed inverter design will be implemented to support the renewable energy integrations.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

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