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Design and Implementation of Three Phase Reversing Voltage Multilevel Inverter

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ABSTRACT

This paper examines how a Reversing voltage multilevel inverter (RVMLI) strategy is enforced to develop multilevel inverter fulfilment. This approach has been used SPWM-PD technique to regulate the electrical inverter. It desires numerous less range of carrier signals to deliver gate pulses of switches. Increasing within the levels during this strategy aid in reduction of output voltage harmonics expeditiously and improves power quality at output of the electrical inverter. It wants a lowered quantity of total switches, which is in a position to decreases of switching losses in this process. The Three-phase reversing voltage multilevel inverter of 7- level and 9- level is accomplished for R-load and R-L load and Three Phase Induction Motor. A reversing voltage multilevel inverter of 7- level and 9- level simulation is intended and developed. Mat lab/Simulink outcome is awarded to validate the proposed scheme.

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1. INTRODUCTION

At present world, the requirement of using power electronic devices in each equipment and applications is essential. Whereas advanced power converters are creating a mark on the market of the world. Whereas Inverters subject almost always famed for changing a Dc provide to Ac deliver. The output of the inverter has to be compelled to maintain a close to sinusoidal for economical functioning as load systems. In traditional inverters, the harmonic content is also decreased with aid of making use of varied modulation techniques. However, thanks to limitations on the rating of power electronic switches the output powers of the traditional inverters area unit confined to low-power applications. So, multilevel inverters are preferred for medium and high power ratings, which provides to arise from the output power and additionally results of increasing from the output waved shapes nearly sinusoidal and decrease of whole harmonic distortion. During operation of multilevel inverter as the number of levels will increases from the output voltage that improves power quality and it reduces the harmonic content. To overcome multilevel inverter (MLI) Strategy problems like, using a number of switches to perform the power conversion, difficult PWM Controlling techniques like SPWM SV PWM, SHE-PWM, increased a number of elements and voltage corresponding difficulties[1]. Whereas power applications, such a thing is UPS, PV systems, HVDC, FACTS etc., best appropriate to reversing voltage multilevel inverter[2]. However, multi winding transformers manufacturing is expense and design are tough for using in high power applications[3]. A novel 4-level inverter strategy is introduced[4]. It capable of producing an even number of levels, but not zero level. The above issues are lowered by way of a replacement method referred to as reversing voltage multilevel inverter process. For the period of this technique, that is dependable for generating every positive polarity waveform and negative polarity waveforms by way of reversing voltage multilevel inverter[5]. The reversing voltage multilevel inverter desires much less quantity of switches and devices, it needs most effective half the carriers for

generating pulses of switches to utilizing PD-SPWM control technique have been developed for the duration of this paper.

Advantages:

- It simply extended to higher levels by adding middle stages.
- It uses isolated Dc supplies and thus no voltage levelling issues.
- It uses fewer elements in comparison to Conventional multilevel inverters
- It simply solely needs half of carrier for SPWM controller.
- It will simply apply for three-phase applications

2. DESCRIPTION OF REVERSING VOLTAGE MULTILEVEL INVERTER

The Reversing voltage multilevel inverter that includes of two parts, specifically level generation parted and polarity generation parted. The waveforms of resultant voltage in the positive sign are obtained by using High-frequency switches to the extent Level generation part. The waveforms of resultant voltage are acquired by Low-frequency switches both sign of positive or negative within the polarity generation part. For getting resultant output voltage levels at a specific line frequency, each level generation part and polarity generation part is principal and predominant. Switching transition and switching power dissipation could also be lowered by way of identifying the switching modes unique averting the un-known as for voltage levels within the time of switching cycle. Totally different switching modes in producing the desired levels. The output voltage levels are generated with the aid of authorised switching sequences. The switching sequence of switches modes are chosen for levels respectively. This strategy is redundant and versatile within the switching sequence. The last word output voltage level is that the add of voltage sources.

2.1. Seven-Level Reversing Voltage Multilevel Inverter

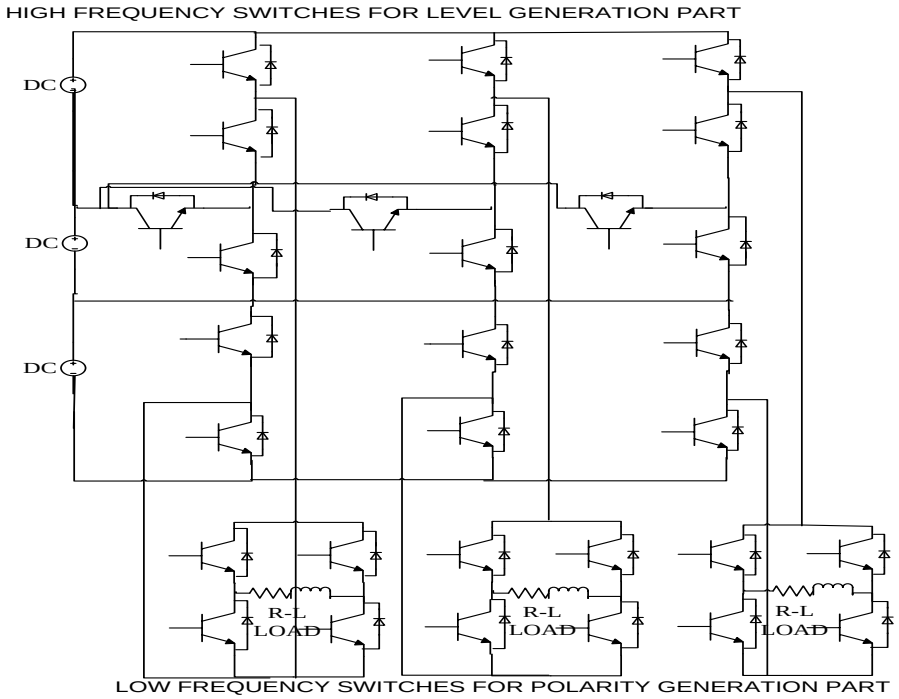


Figure 1. Reversing voltage multilevel inverter for three phases connected to the R-L load.

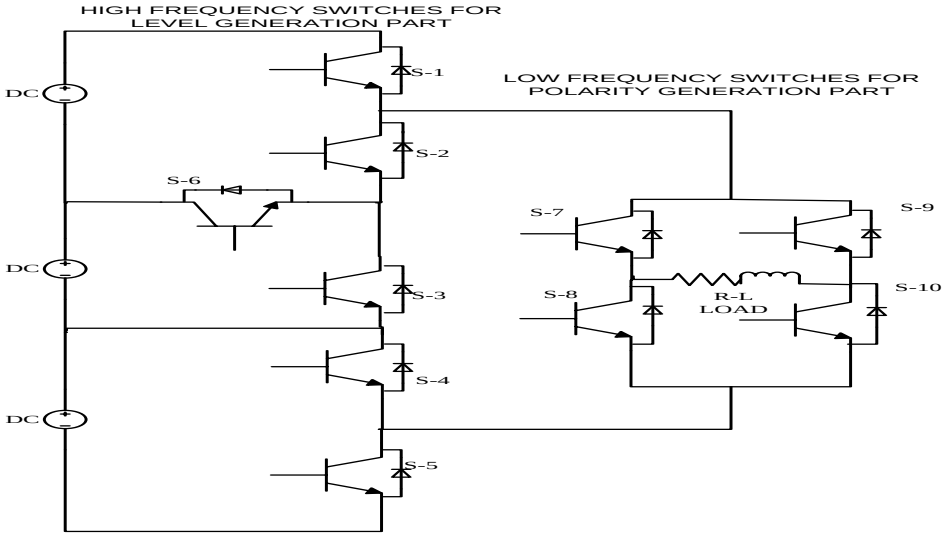


Figure 2. Reversing voltage 7-level inverter for single phase leg.

Table 1. Switching function for voltage output seven level generations

DC Voltage Level	Mode-1 Operation	Mode-2 Operation
0	2,3,4	
1	2,3,5	2,4,6
2	1,4	2,6,5
3	1,5	

Operation of reversing voltage 7-level inverter:

The switching approach of reversing voltage 7-level inverter. The switching modes to get distinct voltage levels are

- When switches 2-3-4 is on, output waveform produces voltage level 0 V Dc,
- When switches 2-3-5 is on, output waveform produces voltage level +1 V Dc,
- When switches 1-4 is on, output waveform produces voltage level +2 V Dc,
- When switches 1-6 is on, output waveform produces voltage level +3 V Dc.

This presents a seven-level inverter utilizing reversing voltage strategy. A seven-level inverter requires 10 switches and 3 dc energy sources to form a circuit and to generate the output voltage as shown in figure2. Switching of high frequency is having phase disposition pulses and switching of low frequency may have pulses of the line frequency (50 Hz) then, the resultant output voltage is fed to the load. The association of switches commencing from S_1 to S_{10} that are in single-phase leg is got by means of operation of reversing voltage multilevel inverter of 7-level as shown in a figure. The high-frequency switches are used to produce two positive half of cycles with in line frequency. With the assistance of full bridge converter, the second cycle of High-Frequency Bridge will also be converted into a negative half cycle. In an effort to urge alternating waveform, the requirement of a full bridge converter is crucial. With the assistance of full bridge converter, we will be able to cut down the amount of switches to 12 to 10 such switch losses could also be diminished. In reversing voltage 7-level inverter, with a purpose to curb switches it want an improved full bridge converter. As soon as involving substitute obtainable multilevel inverters strategy, this reversing voltage multilevel inverter strategy, requires much less quantity of switch devices. It plays a consequential role of the potency of an overall converter.

2.2. Nine Level Reversing Voltage Multilevel Inverter

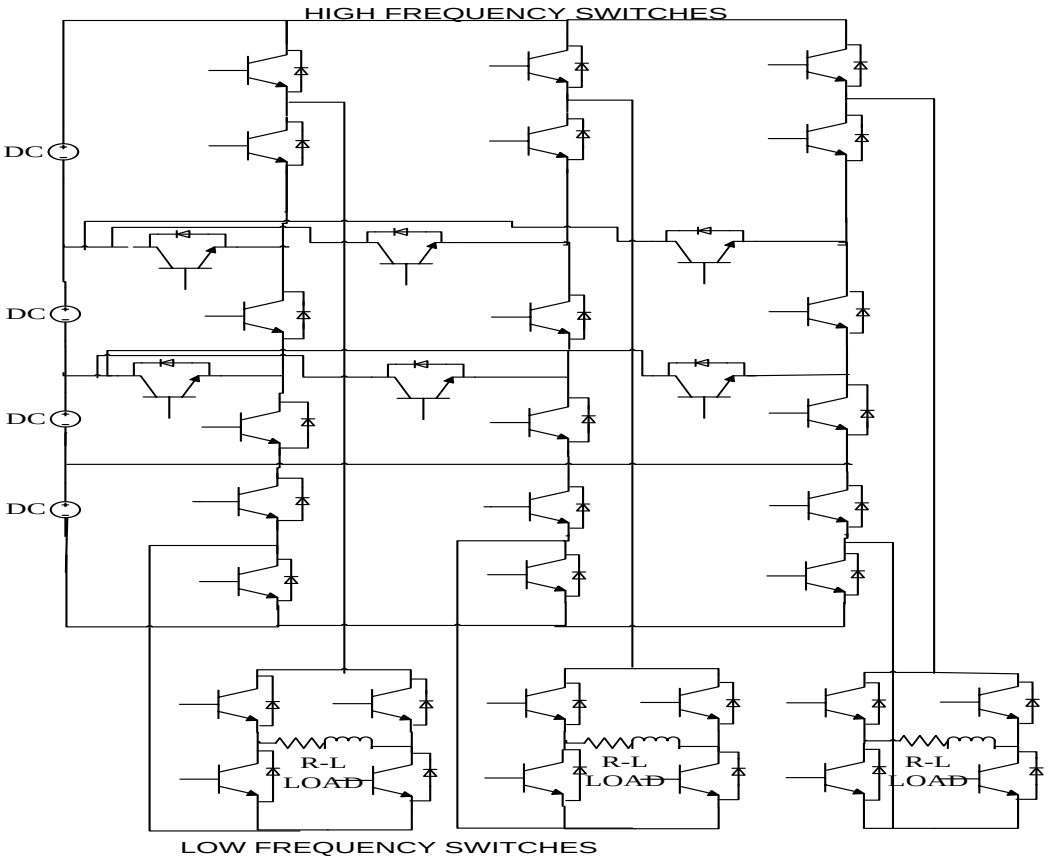


Figure 3. Reversing voltage multilevel inverter for three phases connected to the R-L load.

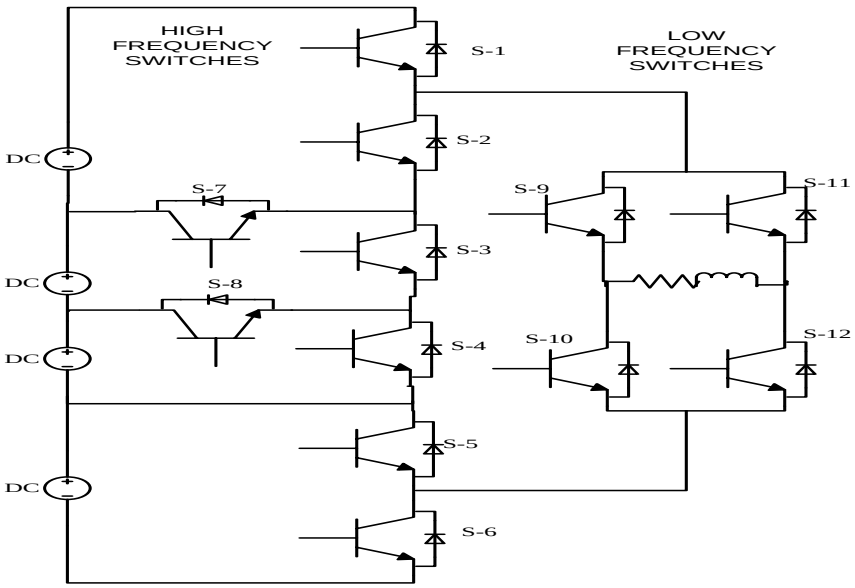


Figure 4. Reversing voltage 9- level inverter for single phase leg**.**

Table-2 Switching function for voltage output 9- level generation

DC Voltage level	Mode-1 Operation	Mode-2 operation
0	2,3,4,5	
1	2,3,4,6	
2	2,3,6,8	2,7,5
3	1,5	2,7,6
4	1,6	

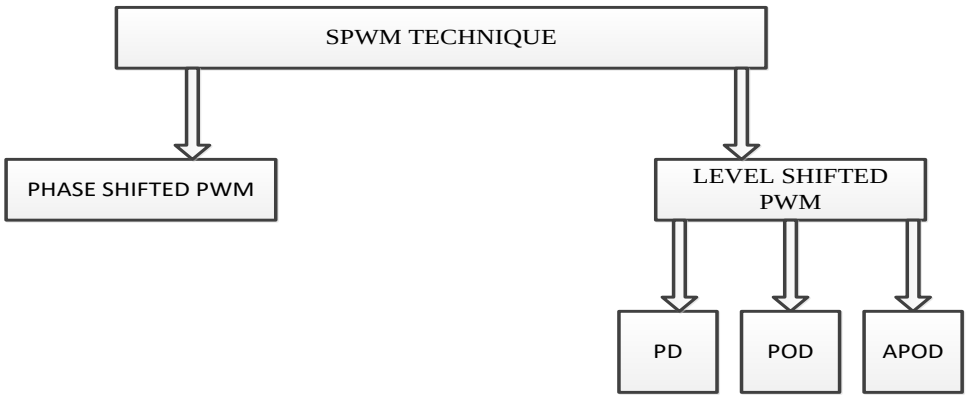
This presents a nine-level inverter utilizing reversing voltage strategy. A nine-level inverter requires 12 switches and 4 dc energy sources to form a circuit and to generate the output voltage as shown in figure4. The harmonic content material of the output voltage waveform decreases because the quantity of output voltage increases.

Operation of reversing voltage 9-level inverter:

The switching approach of reversing voltage 9-level inverter. The switching modes to get distinct voltage levels are

1. When a switch 2-3-4-5 is on, output waveform produces voltage level 0 V Dc,
2. When a switch 2-3-4-6 is on, output waveform produces voltage level +1 V Dc,
3. When a switch 2-3-6-8 is on, output waveform produces voltage level +2 V Dc,
4. When switches 1-5 is on, output waveform produces voltage level +3 V Dc.
5. When switches 1-6 is on, output waveform produces voltage level +4 V Dc.

3. DESCRIPTION OF PHASE DISPOSITION TECHNIQUE



In SPWM, a sinusoidal waveform is related to a carrier waveform to get gate pulses of the switches to an inverter. N-level output desires N-1 carrier per the common multilevel inverter. Quantity of wanted carriers decreased to $\frac{(N-1)}{2}$ simplest by using exploitation right number of levels earned in deliberate reversing voltage multilevel inverter method. Control procedures for the multilevel inverter are based on line and high frequency switching. Completely different PWM techniques are 1. SPWM 2. SVPWM 3. SHE-PWM techniques are in most cases used. The SPWM technique is wide used considering of a couple of advantages.

- Simple implementation
- Low harmonic content
- Less switching losses.

The level shifted modulation technique consists of three schemes

- Each carrier is in phase with each other in Phase Disposition (PD) technique.
- Each carrier waveform is 180-degree phase oppositions to its neighbour in Alternative Phase Opposition Disposition (APOD) technique.
- If the carrier waveform is above and below the point of zero references then the waveform of carrier waveform is modified to 180 degrees in Phase Opposition Disposition (APOD) technique.

In order to urge the desired controlled gate pulses for deliberate circuits of making use of phase disposition method of SPWM technique. Throughout this reversing voltage multilevel inverter, we need like most effective three carrier waveforms that are compared with the only single sinusoidal waveform within the positive part of the one cycle, Whenever an intersection takes place between the carrier and sinusoidal there's a formation of pulses in that area. We tend to create three pulses at that intersection part of the area. The produced pulses are changed into substitute pulses of making use of not operation (like once switch is on then it produces alternative is off), then we are inclined to get the desired switching pulses and fed to the six switches to the level generation part. Ultimate pulses of a full bridge converter is created by the pulse generator is employed to get pulses of the polarity generation part.

The formula is applied to PD-SPWM in reversing voltage multilevel inverter

The frequency modulation index

$$M_f = {F_c}/{F_m} \tag{1}$$

The amplitude modulation index

$$M_a = {v_m}\Big/{\frac{(n-1)}{2} v_c} \tag{2}$$

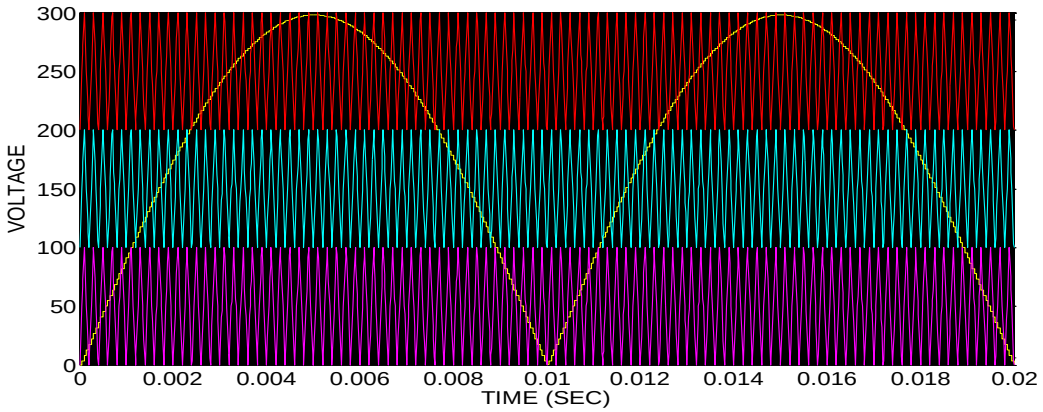


Figure 5. (A) 3-carrier waveform.

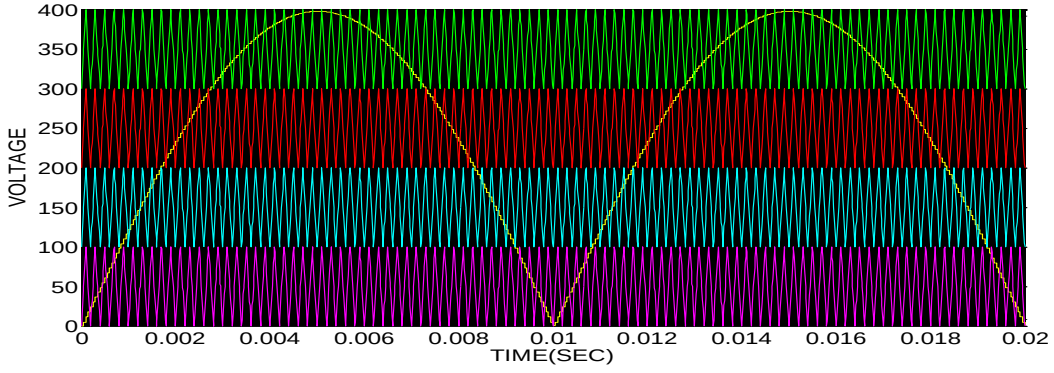


Figure 5. (b) 4-carrier waveform.

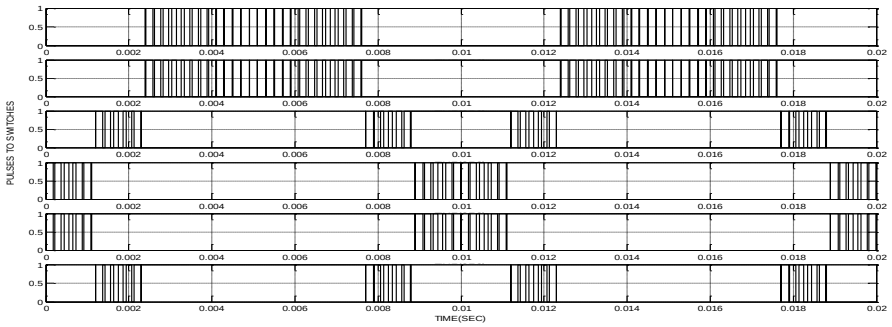


Figure 6. (a) Gate pulses to switches for 7-level.

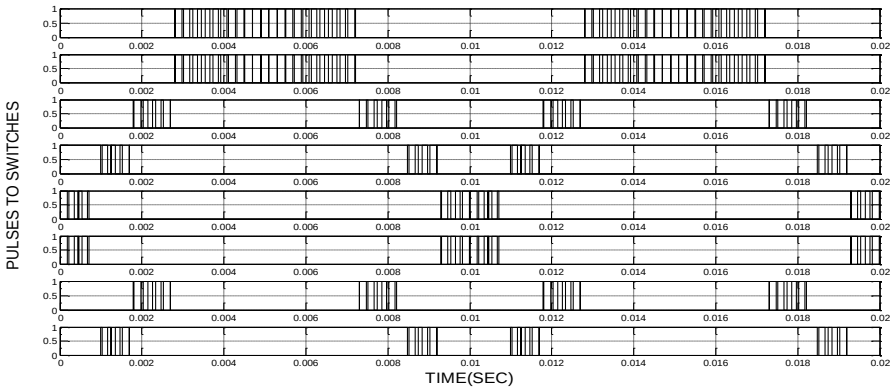


Figure 6. (b) Gate pulses to switches for 9- level.

4. IMPLEMENTATION OF THREE PHASES REVERSING VOLTAGE SEVEN LEVEL AND NINE LEVEL INVERTER

Table-3 Comparison and number of different multilevel inverter strategies for three-phase

strategies	DC MLI	FCMLI	CDMLI	RV MLI
Switches ,diodes	$6(n-1)$	$6(n-1)$	$6(n-1)$	$3((n-1)+4))$
Diodes	$3(n-1)$ $(n-2)$	0	0	0
Dc bus capacitor/isolated supplies	$(n-1)$	$(n-1)$	$(n-1)$	$\frac{(n-1)}{2}$
Flying capacitor	0	$\frac{3}{2}(n-1)$ $(n-2)$	0	0
Over-all numbers	$(n-1)$ $(3n+7)$	$\frac{1}{2}(n-1)$ $(3n+20)$	$\frac{27}{2}(n-1)$	$\frac{(13n+35)}{2}$

Design parameters for three phase reversing voltage 7- level inverter and 9-level inverter

FOR 7-LEVEL INVERTER:

Input Dc voltage V Dc =300 V
Reference (sinusoidal) switching frequency (F m) = 50 Hz
Carrier (triangular) switching frequency (F c) = 5 kHz
Three phase load = R= 10 Ω; L = 15 MH
Output Voltage=600 V p-p
LC Filter = L=10 MH; C= 20 µF

FOR 9-LEVEL INVERTER:

Input Dc voltage V Dc =400 V
Three phase load = R= 10 Ω; L = 15 MH
Output Voltage=800 V p-p
LC Filter = L=10 MH; C= 20 µF

Table-4 Induction motor parameters

Voltage	400 V
Current	5.78 A
Horsepower	5.36 H.P
Frequency	50 Hz
Speed	1430 rpm

5. MAT LAB CIRCUIT DIAGRAM DESIGN AND SIMULATION RESULTS

The outcome of simulation of urged technique of three phase 7-level and 9-level of reversing voltage multilevel inverter are finished by victimization MATLAB 2009b/Simulink. Add of DC inputs voltage sources is adequate to voltage output waveforms during this strategy. From FFT analysis in Powergui block will recognize the THD of voltage output and current output values. The simulation diagrams of three phase reversing voltage multilevel inverter are developed for 7- level inverter and 9-level inverter, we are likely to get the voltage and current output waveforms, torque and speed waveforms is produced for the loads R, R-L and induction motor. The output voltage and current waveforms that are shaped within the staircase type.

In every 7-RVMLI and 9-RVMLI, we can convert staircase type into sine waveform by including filters at the output of reversing voltage multilevel inverter. There are higher advantages by means of utilizing filters we are able to lessen the harmonics, make stronger the lifetime of the equipment, performance and potency are high, power factor can also be high. During this reversing voltage multilevel inverter, have a tendency to make use of Butterworth filter which is the low pass second order filters and LC filter is positioned at the output of an inverter. The output load to produce required resultant waveforms of voltage and current in a sinusoidal form. Simulation outcome of the proposed strategy of reversing voltage multilevel inverter is performed by utilizing mat-lab.

5.1. Three Phase 7-Level Reversing Voltage Multilevel Inverter

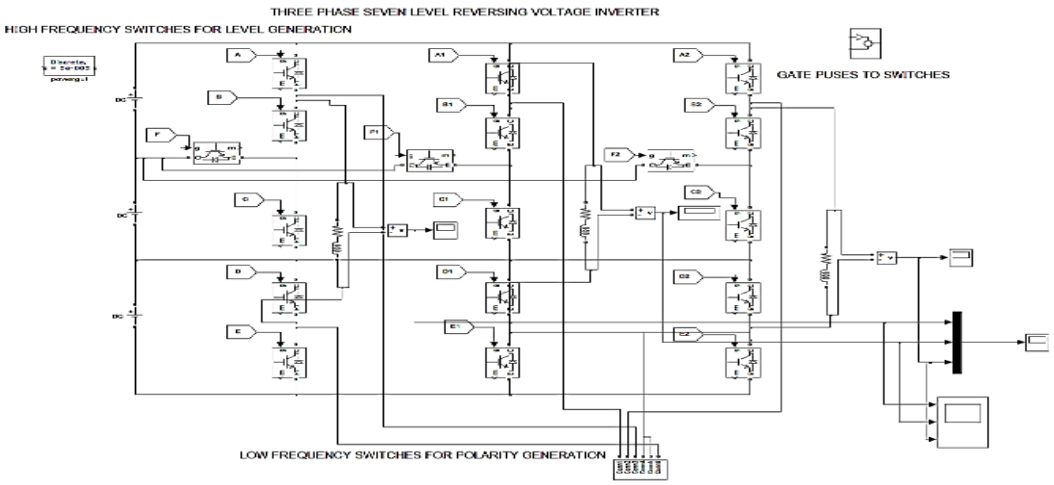


Figure7 (a). Level generation part

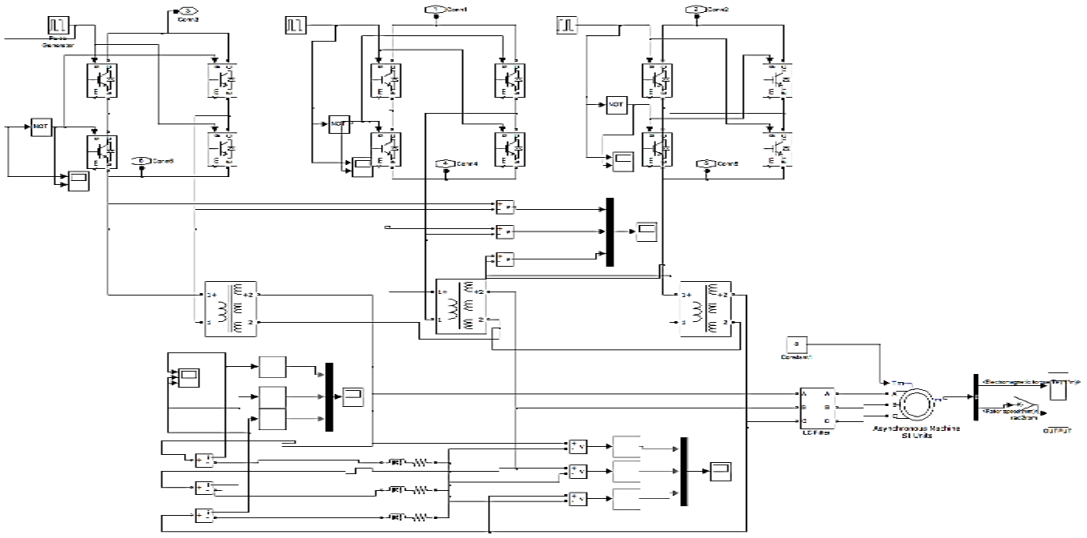


Figure 7 (b). Polarity generation part

From above figures 7(a) for level generation part, 7(b) for polarity generation part. Simulink diagram of 7-level three phase reversing voltage multilevel inverter is designed.

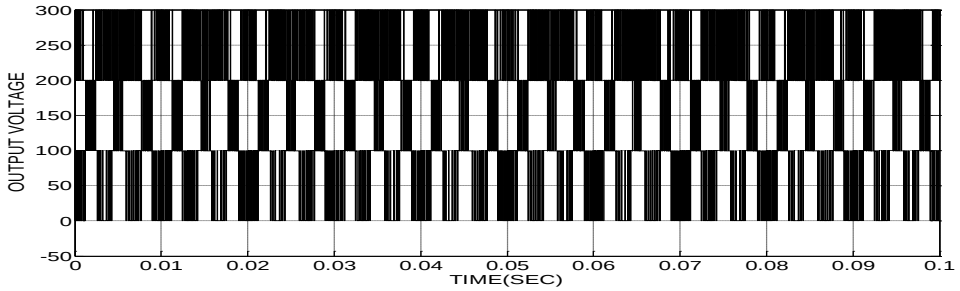


Figure 8 (a). Voltage Output waveforms of 3-phase 7-level reversing voltage multilevel inverter.

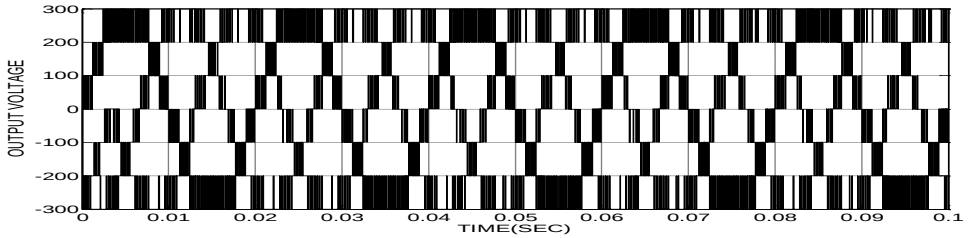


Figure 8 (b). Voltage Output waveforms of 3-phase 7-level reversing voltage multilevel inverter.

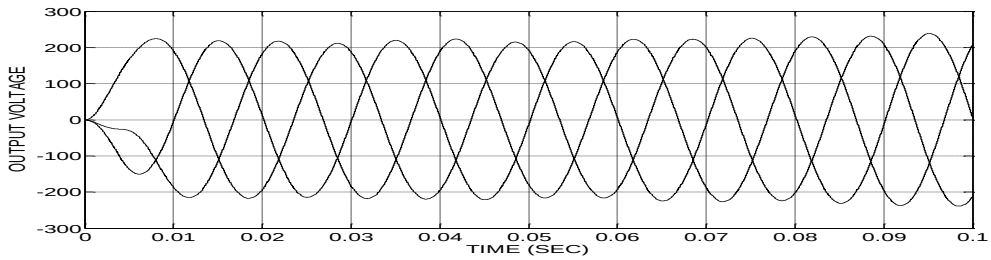


Figure 9 (a). Voltage Output waveform for 7-Level R-L load and for induction motor.

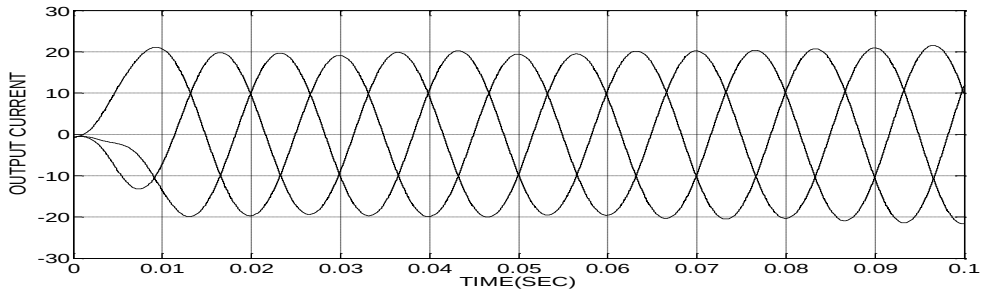


Figure 9 (b). Current output waveforms for 7-Level R-L load and for induction motor.

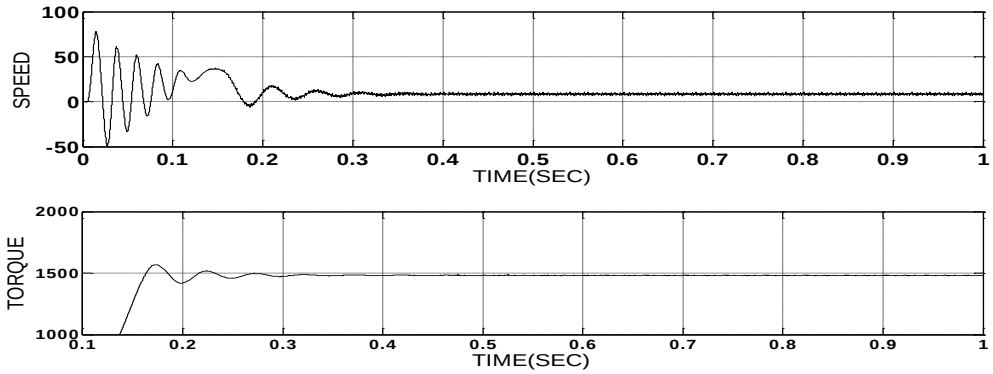


Figure 10. Torque and Speed structures waveform.

The circuit diagram constructed in Mat lab/Simulink of three phase RVMLI strategy for 7-level is simulated for different loads R, R-L and Induction motor we get the voltage and current, speed and torque output waveforms are shown in the above figures.

5.2. Three phase 9-Level Reversing Voltage Multilevel Inverter

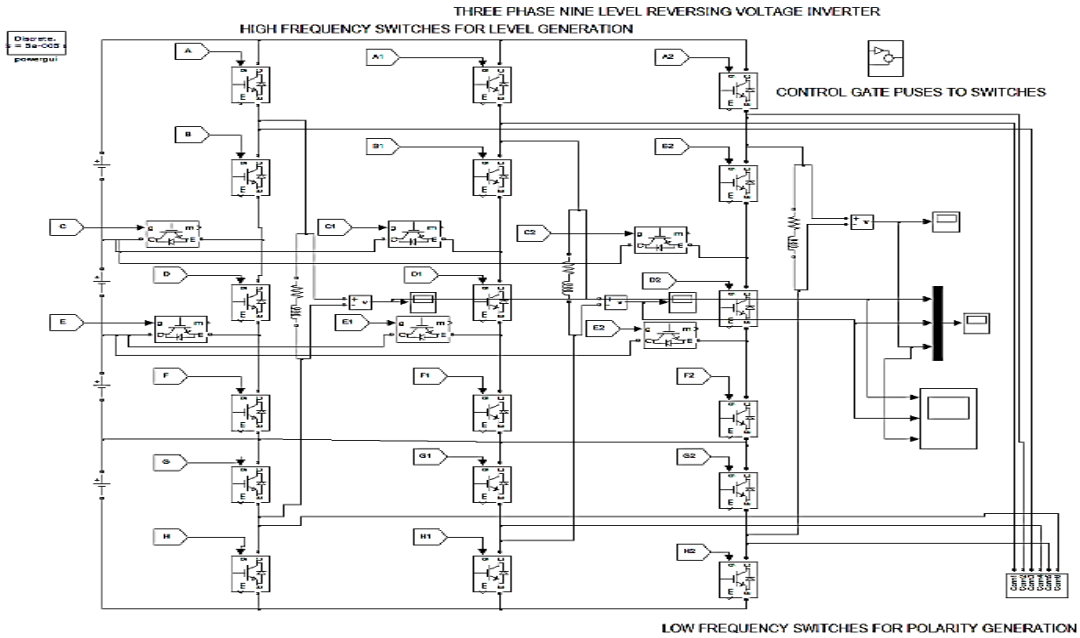


Figure 11 (a). Level genration part

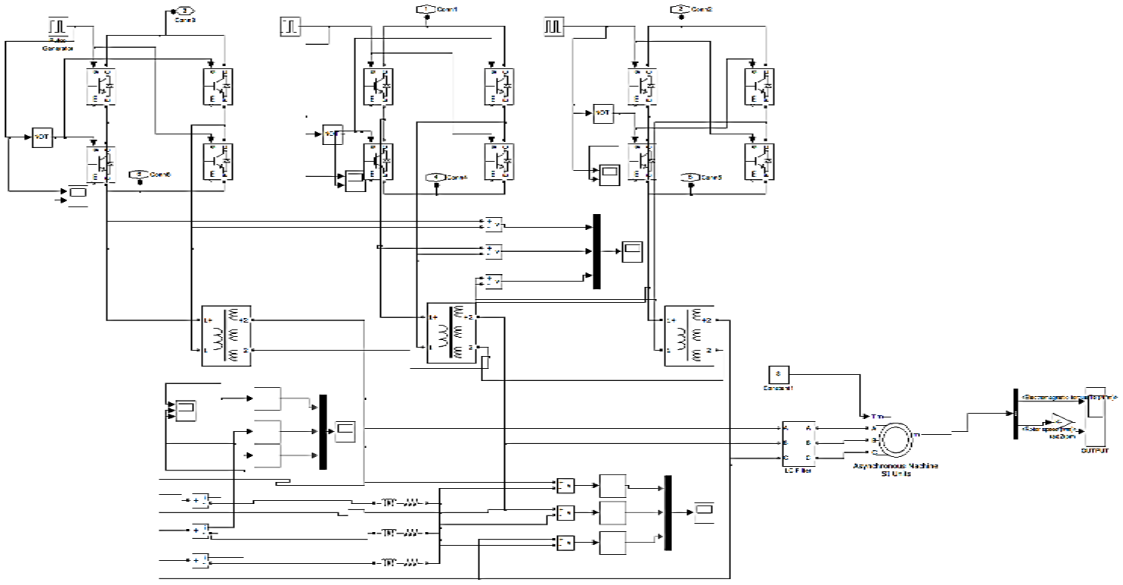


Figure 11 (b). polarity generation part

From above figures 11(a) for level generation part 11(b) for polarity generation part. Simulink diagram of 9- level three phase reversing voltage multilevel inverter is designed.

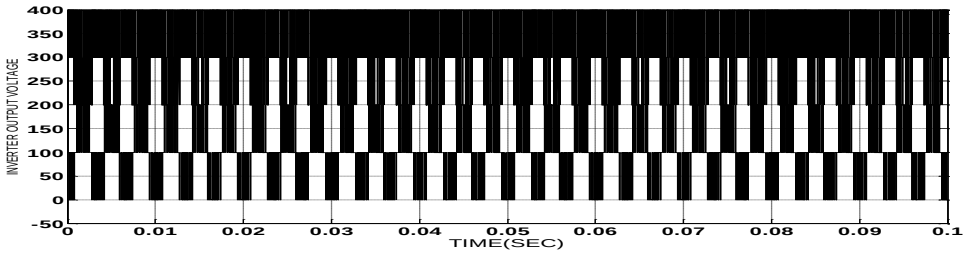


Figure 12(a). Voltage Output waveforms of 3-phase 9-level reversing voltage multilevel inverter.

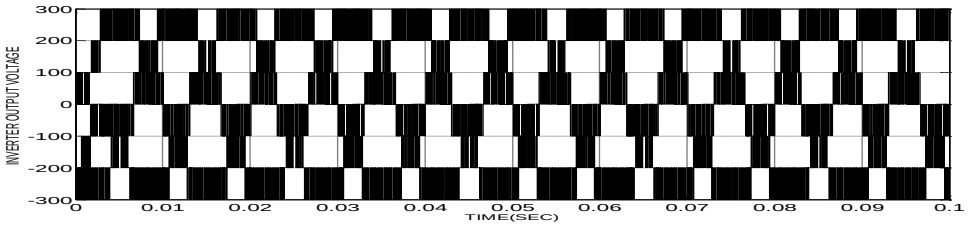


Figure 12(b). Current Output waveforms of 3-phase 9-level reversing voltage multilevel inverter.

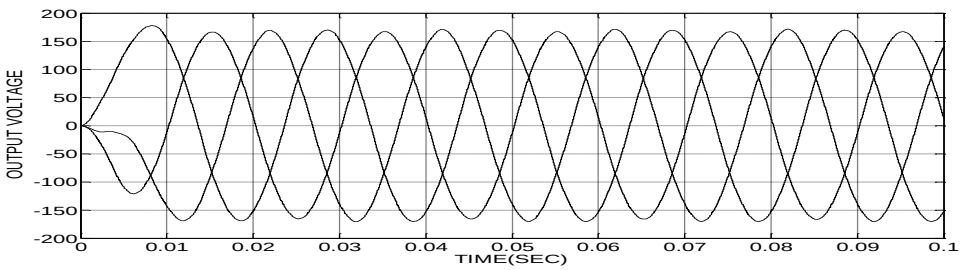


Figure 13 (a). Voltage Output waveform for 9-Level
R-L load and for induction motor.

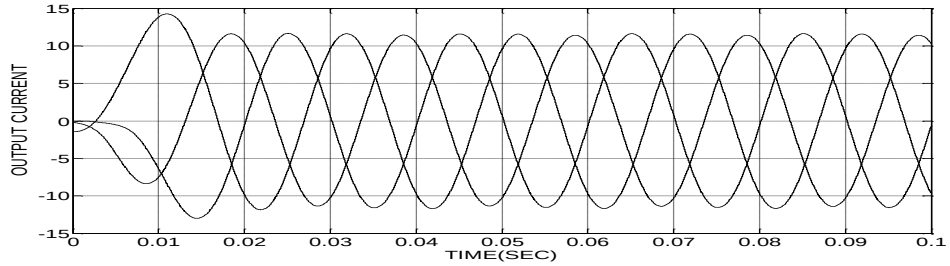


Figure 13 (b). Current output waveforms for 9-Level
R-L load and for induction motor.

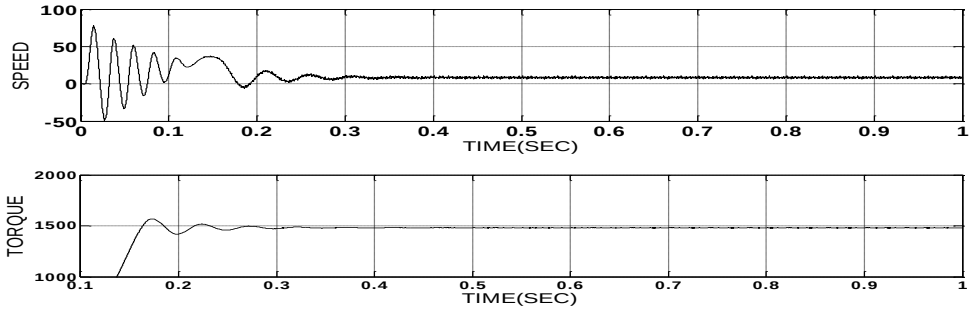


Figure 14. Torque and Speed structures waveform

The circuit diagram constructed in Mat lab/Simulink of three phase RVMLI strategy for 9-level is simulated for different loads R, R-L and Induction motor we get the voltage and current, speed and torque output waveforms are shown in the above figures.

5.3. THD Values For 7 and 9-Level Three Faze Reversing Voltage Multilevel Inverter

Table -5 Voltage Output and current output THD for R-Load before and after filter.

RVMLI	VOLTAGE OUTPUT(V)	THD (%)	CURRENT OUTPUT(I)	THD (%)
7-LEVEL	298	18.10	28.81	2.00
AFTER FILTER 7-LEVEL	286.1	2.00	28.62	2.00
9-LEVEL	391.3	16.30	36.02	1.64
AFTER FILTER 9-LEVEL	361.2	1.64	36.02	1.64

Table -6 Voltage Output and current output THD for Induction motor before and after filter.

RVMLI	VOLTAGE OUTPUT(V)	THD (%)	CURRENTOUTPUT(I)	THD (%)
7-LEVEL	298	18.09	23.48	0.67
AFTER FILTER 7-LEVEL	274.5	13.80	23.24	0.67
9-LEVEL	391.5	16.17	30.97	0.77
AFTER FILTER 9-LEVEL	340.4	11.17	30.8	0.77

6. CONCLUSION

A brand new strategy of a multilevel inverter is developed in the course of this paper. It has several enticing qualities when compared with alternative multilevel inverters. It can produce voltage output in a staircase type into fewer disturbances as a result of this, voltage derating stress on the switches gets diminished, electromagnetic interference are additionally reduced. Bearing strain on the motor is diminished

by minimizing common mode voltage within the multilevel inverter. It attracts input currents with fewer disturbances. It will be extended for a maximum number of levels to the implementation of the work. Performance and as a result, the resultant output response is excessive provided that the specified switching frequency and constarined losses are obtained. From the comparison of reversing voltage strategy of three phase 7- level multilevel inverter and 9- level multilevel inverter, it shows that whole harmonic distortion outcome indicates that growing to levels at output voltage waved shapes decreased the harmonics contents at the output. Throughout this paper, simulation results are presented for three phase 7- level multilevel inverter, 9- level multilevel inverter of reversing voltage strategy.

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