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FPGA based fault tolerant scheme on four switch voltage source inverter

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ABSTRACT

This paper presents an efficient methodology to detect the fault occurrence and its tolerance of four switch voltage source inverter in a single Xilinx Spartan 3E Field Pro-grammable Gate Array (FPGA). The merit of this proposed system reduces the time period between fault existence and its isolation with four switches in two legs instead of six switches in three legs so as to minimize the switching losses, accuracy, and better recovery time. The FPGA platform supports the run-time reconfiguration of control functions and algorithms directly in hardware and meets hard real-time performance criteria in terms of timings for SVPWM generation, fault detection time and fault tolerance time. Simulation and Experimental results of this proposed system is demonstrated and verified.

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1. INTRODUCTION

Three phase voltage source inverters (VSI) are primary power components of many industrial applications like electrical machine drive, uninterruptible power system (UPS) and active power filter. VSI combined with three phase induction motor [5, 10] is used in the application of AC electrical machine drives. In the past years, three phase voltage source inverters composed of three legs with six semi-conductor devices have been used for variable speed AC motor drives [12-14, 16]. But in recent trends a new advance technology, three phase voltage source inverters with four switches [17] are very popular in the applications of power electronics. Because it consists of only a four switches in two legs and third leg is DC link capacitor [7] voltage. The cost due to less number of switches, reduction in switching losses and less chances of destroying the power switches, four switch voltage source inverters (FSVSI) are preferred over six switch voltage source inverters.

Fault is uncertainty and malfunction which leads to sudden failure or breakdown. Due to abnormal condition, a fault occurs in any system is unbelievable and it has to be isolated. To control the fault and maintain safety and reliability, the fault tolerant control (FTC) is necessary to investigate the fault occurrence and its isolation. FTC has three important schemes.

- Fault identification
- Fault isolation
- Controller scheme

In fault identification, scheme offers identification of fault , that means it investigates where the fault occurs in the processing system. Previously many papers have been published [1,4] for fault detection

methods. Investigation of the six switch voltage source pulse-width modulation (PWM) inverter system for induction motor drives on various fault modes by Kastha and Bose[3].

In fault isolation, the switching fault may be an open circuit fault or short circuit fault in the system, FTC plans and recommends an isolation process for particular fault. For example, in case of short circuit fault, isolation can be achieved by fast acting fuses.

In mathematical modeling when a fault occurs, the parameters or variables are deviated from the normal system and reaches to unstable region. Controller scheme (FTC) [3-5] is to control those variables to drive the process to maintain the desired response by designing a suitable controller. To design any system, that should be stable system and the time between fault occurrence and its isolation should be minimized so as to the system runs continuously. FTC provides a suitable controller which has to modify the parameters and the system goes to stable system. In recent years, the following controllers are used for fault tolerant schemes

- PI controlled scheme
- Fuzzy controlled scheme
- FPGA controller scheme

The above controllers are used to detect and isolate the fault which occurs in any one of the switches in the proposed inverter and also reduces or minimizes the time between the fault occurrence and its isolation. All controllers generate necessary gate pulses for triggering the power switches in FSVSI.

Recently high switching frequency power semiconductor devices such as IGBT are used for developing high frequency pulse width modulation techniques. In order to reduce the harmonics, THD, noise and better dynamic response, space vector pulse width modulation (SVPWM) is better choice for producing required gate pulses and control the output voltage. SVPWM [18] is also developing the vector durations of voltage space vectors.

Previously PI and Fuzzy control algorithms [19] were used for fault time recovery. Nowadays, FPGA controller [1,2] is used in fault tolerant scheme for better time recovery and accuracy. Many papers have been published about the fault tolerant schemes with fault detection time. Recently S.Karimi,P.Poure and S.Saadate proposed a fast power switch failure detection scheme for three phase with normal three leg voltage source inverters, in which minimization of the time interval was in the fraction of microseconds.

2. FAULT TOLERANT TOPOLOGY

Figure 1 shows a fault tolerant topology for a four switch voltage source inverter [6-9,11]with three phase load. This proposed inverter scheme is composed of three legs with four switches (S_1 toS_4) in two legs and two dc-link capacitors in third leg. In addition to that auxiliary leg (fourth leg), which is formed by two more switches (S_5 and S_6) acts as a replacing leg and two triac switches as connecting switches between inverter switching legs and auxiliary leg. When fault occurs at the any one of the switches in the inverter, the proposed system detects and isolates the faulty leg. The isolation is implemented by removing the gate signal for the particular faulty switch and triggers the corresponding bidirectional triac switch (either T_1or T_2).

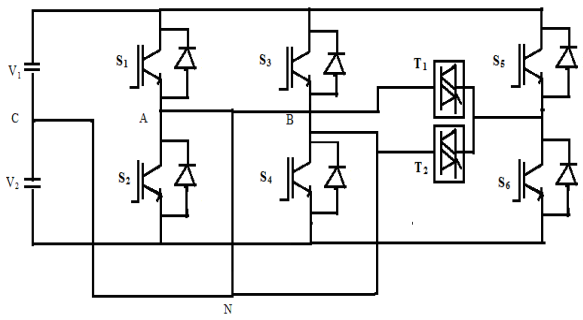

Figure 1. FSVSI fault tolerant topology

If any fault occurs at any one of the power switches in main circuit, an auxiliary leg which consists of two switches replaces that faulty leg through concerned bidirectional triac switch and the operation continues during the fault existence. For example if fault occurs in S_1 or S_2, then triggering pulses given to the both switches are removed and auxiliary leg (S_5 and S_6) replaces and acts as main leg by triggering the bidirectional switch T_1

According to space vector modulation analogy, components of αβ of the voltage vectors from abc voltages by clark's transformation can be written as (1)

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

Where phase voltages are defined by (2)

$$V_a = \frac{1}{3}(2V_{a0} - V_{bo}); V_b = \frac{1}{3}(2V_{b0} - V_{a0}); V_c = -\frac{1}{3}(V_{a0} + V_{b0}) \quad (2)$$

In space vector pulse width modulation, there are four possible space vectors for main circuit power switches and two vectors for auxiliary leg power switches. In four vector analogy, each voltage space vector is displaced by 90^0. in αβ plane. The representation of different switching functions and space vectors shown in Table 1.

Table 1. Switching functions and Voltage vectors

S_1	S_3	$V=V\alpha+jV_\beta$
0	0	$V_1 = \frac{V_{dc}}{3}e^{j\frac{2\pi}{3}}$
1	0	$V_2 = 2\frac{V_{dc}}{3}e^{j\frac{\pi}{6}}$
1	1	$V_3 = \frac{V_{dc}}{3}e^{j\frac{\pi}{3}}$
0	1	$V_4 = 2\frac{V_{dc}}{3}e^{j\frac{5\pi}{6}}$

3. SPACE VECTOR MODULATION AND PWM GENERATION

SVPWM produces necessary pulses for the switching functions S_1 and S_3 within the specified sampling period. During the fault conditions, there are six sectors and four voltage vectors. Switching patterns for sectors I, V, VI are shown in Figure 2. Switching patterns for sectors II, III, IV are shown in Figure 3.

3.1. Pulse patterns for switching in the proposed method.

According to space vector modulation

$$V * T = v_1\, t_1 + v_2\, t_2 + v_3 t_3 + v_4\, t_4 \quad (3)$$

After algebraic simplification time weights are

$$T = t_x + t_y + t_z \quad (4)$$

Voltage space vectors for each sector is given in Table.2

Table 2. Sectors and Vectors

Sector	Vector
I,V,VI	V_1, V_2, V_3
II,III,IV	V_1, V_3, V_4

Sector I

$$t_x = t_{23f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \quad (5)$$

$$t_y = t_{3f} = \frac{\sqrt{3}}{\pi} MT_s \ sin(\alpha) \quad (6)$$

$$t_z = t_{of} = \ T_s/2 - t_{23f} - t_{3f} \quad (7)$$

$$t_{2m} = \frac{t_{23f}}{2} \qquad t_{3m} = \frac{t_{23f}}{2} \quad (8)$$

$$t_{3z} = \frac{t_{of}}{2} \ ; \ t_{1z} = \frac{t_{of}}{2} \quad (9)$$

$$t_{V1} = t_{1z} \quad (10)$$

$$t_{V2} = t_{2m} \quad (11)$$

$$t_{V3} = t_{3f} + t_{3m} + t_{3z} \quad (12)$$

Sector II

$$t_x = t_{3f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \quad (13)$$

$$t_y = t_{34f} = \frac{\sqrt{3}}{\pi} MT_s \ sin(\alpha) \quad (14)$$

$$t_z = t_{of} = \ T_s/2 - t_{3f} - \ t_{34f} \quad (15)$$

$$t_{3m} = \frac{t_{34f}}{2} \ ; \ t_{4m} = \frac{t_{34f}}{2} \quad (16)$$

$$t_{3z} = \frac{t_{of}}{2} \ ; \ t_{1z} = \frac{t_{of}}{2} \quad (17)$$

$$t_{V1} = t_{1z} \quad (18)$$

$$t_{V4} = t_{4m} \quad (19)$$

$$t_{V3} = t_{3f} + t_{3m} + t_{3z} \quad (20)$$

Sector III

$$t_x = t_{34f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \quad (21)$$

$$t_y = t_{41f} = \frac{\sqrt{3}}{\pi} MT_s \ sin(\alpha) \quad (22)$$

$$t_z = t_{of} = T_s/2 - t_{34f} - t_{41f} \quad (23)$$

$$t_{3m} = \frac{t_{34f}}{2} \qquad t_{4m} = \frac{t_{34f}}{2} + \frac{t_{41f}}{2} \quad (24)$$

$$t_{1m} = \frac{t_{41f}}{2} \quad ; \quad t_{1z} = \frac{t_{of}}{2} \; ; \quad t_{3z} = \frac{t_{of}}{2} \quad (25)$$

$$t_{V1} = t_{1z} + t_{1m} \quad (26)$$

$$t_{V4} = t_{4m} \quad (27)$$

$$t_{V3} = t_{3m} + t_{3z} \quad (28)$$

Sector IV

$$t_x = t_{41f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \quad (29)$$

$$t_y = t_{1f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\alpha) \quad (30)$$

$$t_z = t_{of} = T_s/2 - t_{41f} - t_{1f} \quad (31)$$

$$t_{4m} = \frac{t_{41f}}{2} \qquad t_{1m} = \frac{t_{41f}}{2} \quad (32)$$

$$t_{3z} = \frac{t_{of}}{2} \quad ; \quad t_{1z} = \frac{t_{of}}{2} \quad (33)$$

$$t_{V1} = t_{1f} + t_{1z} + t_{1m} \quad (34)$$

$$t_{V4} = t_{4m} \quad (35)$$

$$t_{V3} = t_{3z} \quad (36)$$

Sector V

$$t_x = t_{1f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \quad (37)$$

$$t_y = t_{12f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\alpha) \quad (38)$$

$$t_z = t_{of} = T_s/2 - t_{1f} - t_{12f} \quad (39)$$

$$t_{1m} = \frac{t_{12f}}{2} \quad ; \quad t_{2m} = \frac{t_{12f}}{2} \quad (40)$$

$$t_{3z} = \frac{t_{of}}{2} \quad ; \quad t_{1z} = \frac{t_{of}}{2} \tag{41}$$

$$t_{V1} = t_{1f} + t_{1z} + t_{1m} \tag{42}$$

$$t_{V2} = t_{2m} \tag{43}$$

$$t_{V3} = t_{3z} \tag{44}$$

Sector VI

$$t_x = t_{12f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\frac{\pi}{3} - \alpha) \tag{45}$$

$$t_y = t_{23f} = \frac{\sqrt{3}}{\pi} MT_s \sin(\alpha) \tag{46}$$

$$t_z = t_{of} = T_s/2 - t_{23f} - t_{12f} \tag{47}$$

$$t_{1m} = \frac{t_{23f}}{2} \quad ; t_{2m} = \frac{t_{12f}}{2} + \frac{t_{23f}}{2} \quad t_{3m} = \frac{t_{23f}}{2} \tag{48}$$

$$t_{3z} = \frac{t_{of}}{2} \quad ; \quad t_{1z} = \frac{t_{of}}{2} \tag{49}$$

$$t_{V1} = t_{1z} + t_{1m} \tag{50}$$

$$t_{V2} = t_{2m} \tag{51}$$

$$t_{V3} = t_{3m} + t_{3z} \tag{52}$$

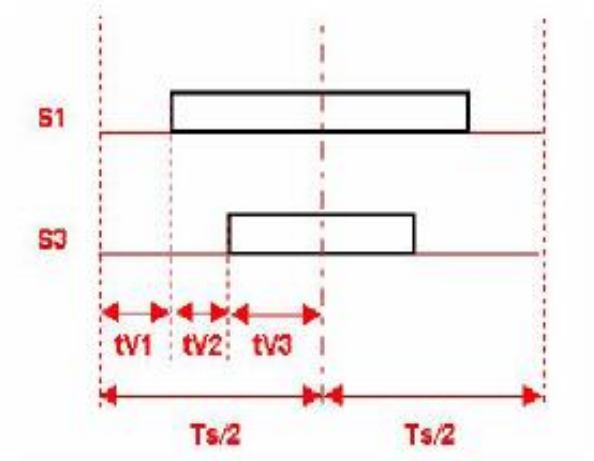

Figure 2. Pulse patterns for sectors I, V, VI

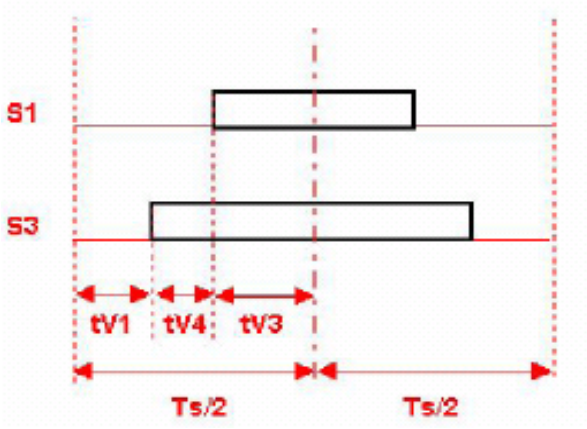

Figure 3. Pulse patterns for Sectors II, III, IV

4. FPGA CONTROL ALGORITHM

The Field Programmable Gate Array (FPGA) can be reprogrammed depending upon the requirement of the user. It provides instant manufacturing turnaround and negligible prototype costs which makes it suitable for embedded system design.
The sequence of steps followed when implementing PWM Generator design on FPGA. These steps are discussed in detail here.

4.1. Design Entry

This is the first step of implementing a design on FPGA. In this step, the VHDL (Very High Speed Integrated Chip Hardware Description Language) code of PWM Generator Architecture was written using software Xilinx ISE 14.1.

4.2. RTL Simulation

The next step is RTL simulation. For this simulation VHDL Test bench was written for PWM Generator architecture and simulation was seen in Xilinx ISE Simulator.

4.3. Design Synthesis

The VHDL code of PWM Generator is then synthesized using Xilinx XST and the synthesis process is used for optimizing the design architecture selected. The resulting netlist is saved to NGC file. After design synthesis, that report is generated which gives information about how many logic blocks used and what device utilization of the design architecture synthesized. It basically maps the behavioral design to gate level design.

4.4. Design Implementation

In this design, there are three steps involved to implement FPGA.

- Translating
- .Mapping
- Placing and Routing

Before translating the design, User Constrained File (UCF) is written to assign pin configuration of the FPGA to the SVPWM Generator I/O‟s. Translate merges together this UCF file and netlist generated after synthesis into Xilinx design file. Mapping is done to fit the design into the available resources of target device i.e. FPGA. and finally Design Implementation is Placing and Routing which places the logic blocks of the design into FPGA and route them together. So that they occupy minimum area and meet timing requirements. This operation produces NCD output file.

4.5. Xilinx Device (FPGA) Programming

In this programming, the process tab of Xilinx ISE which converts the NCD file generated after routing to BIT file. It produces a bitstream for Xilinx Device (FPGA in this case) configuration. BIT file is used for programming the FPGA.

Provide a statement that what is expected, as stated in the "Introduction" chapter can ultimately result in "Results and Discussion" chapter, so there is compatibility. Moreover, it can also be added the prospect of the development of research results and application prospects of further studies into the next (based on result and discussion).

5. SIMULATION RESULTS

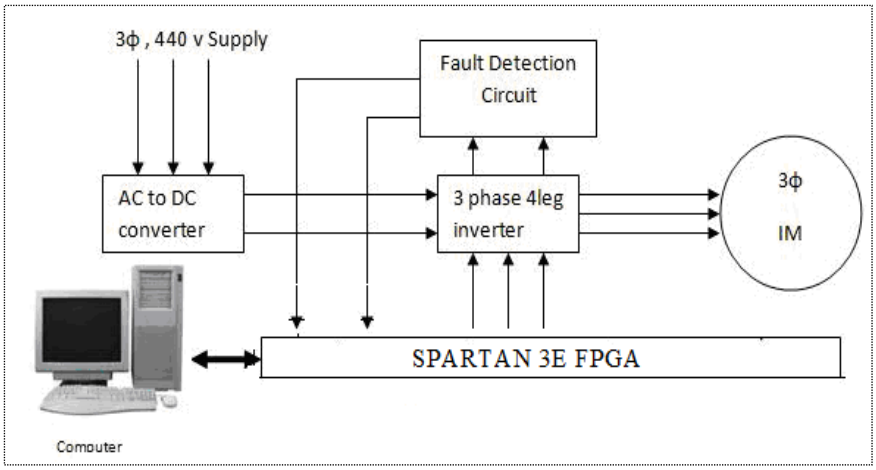

Figure 4. Experimental setup diagram for the scheme

Figure 4 shows an experimental setup for the proposed scheme. SPARTAN 3E FPGA can be used for simulating the results of triggering pulses to all power switches, line to neutral voltage waveforms and fault detection and isolation wave forms . The simulation results of SVPWM wave forms and fault detection wave form are shown in Figure 5 and Figure 6. The figure of SPARTAN 3E FPGA and device utilization is shown in Table 3 and Table 4.

Table 3 Project status

Fault_VSI_top Project Status (07/12/2013 - 08:45:49)	
Project File:	Fault_tolerant_VSI.ise
Module Name:	Fault_VSI_top
Target Device:	xc7a100t-3csg324
Product Version:	ISE 14.1
Design Goal:	Balanced
Design Strategy:	Xilinx Default (unlocked)
Environment:	System Settings

Table 4 Device utilization

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	428	126800	0%
Number of Slice LUTs	686	63400	1%
Number of fully used LUT-FF pairs	255	859	29%
Number of bonded IOBs	13	210	6%
Number of BUFG/BUFGCTRLs	1	32	3%

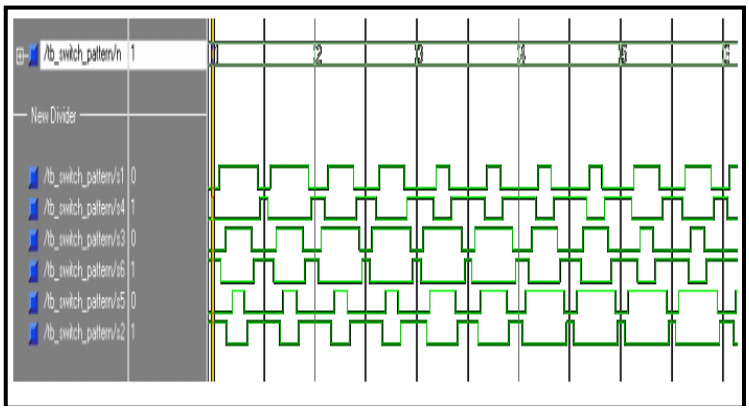

Figure 5. Simulation SVPWM wave forms of 3 ph IM

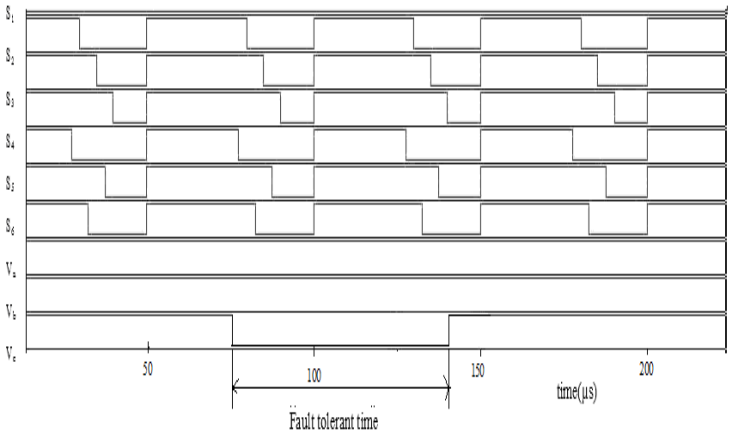

Figure 6. Simulation of pulse wave forms of six switches and fault tolerant time

6. EXPERIMENTAL RESULTS

Experimental setup related to Figure 4 is shown in Figure 7. It has FPGA kit, power module and drivers and three phase induction motor. FPGA gets the values of V_a, V_b and V_c i.e. after calculation V_{ref} for SVPWM generation. This algorithm is executed in FPGA and produces PWM signals outputs. The SVPWM signals from FPGA act as switching signals for IGBT's of VSI are represented in Figure 10. Experimental line to neutral voltages of 3 ph IM are shown in Figure 8. Observation of fault detection and isolation can be obtained from Tektronix DSO with 4 input channels as shown in Figure 10.

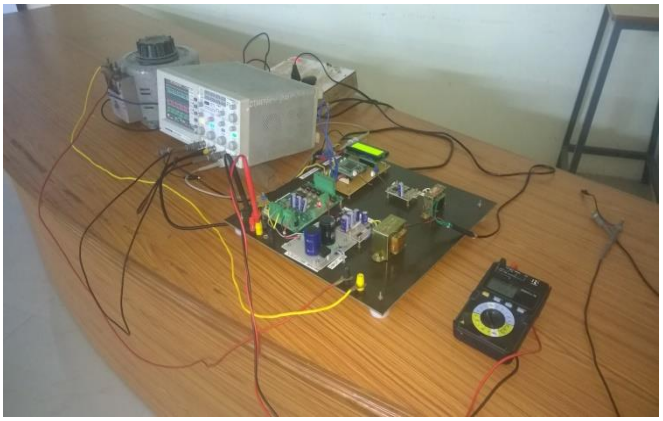

Figure 7. Experimental set up for FSVSI

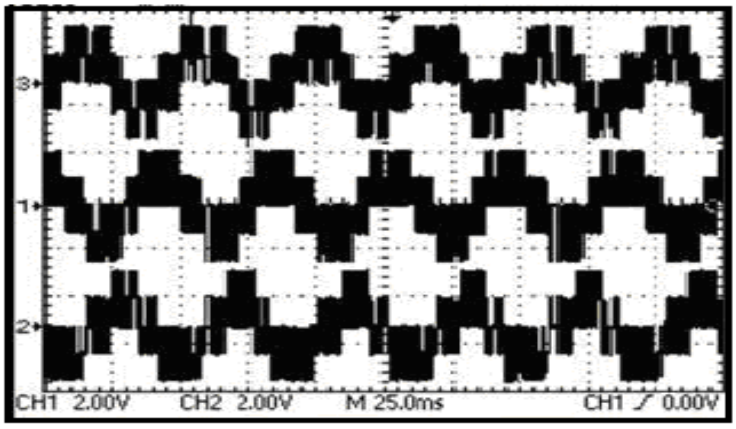

Figure 8. Experimental line to neutral voltages of 3 ph IM

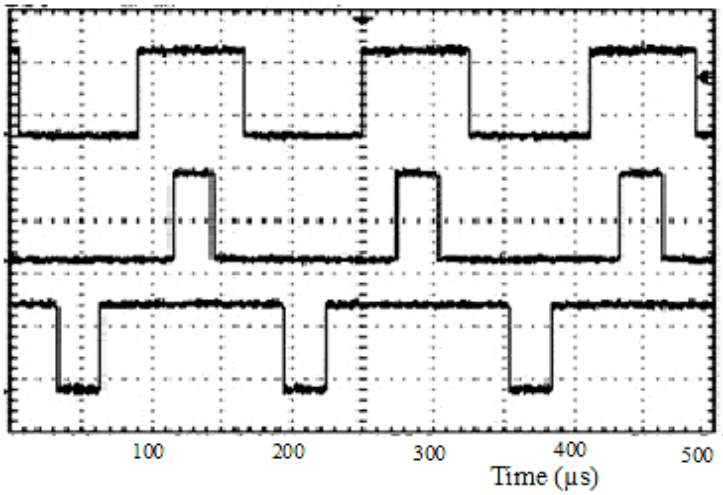

Figure 9. SVPWM signals

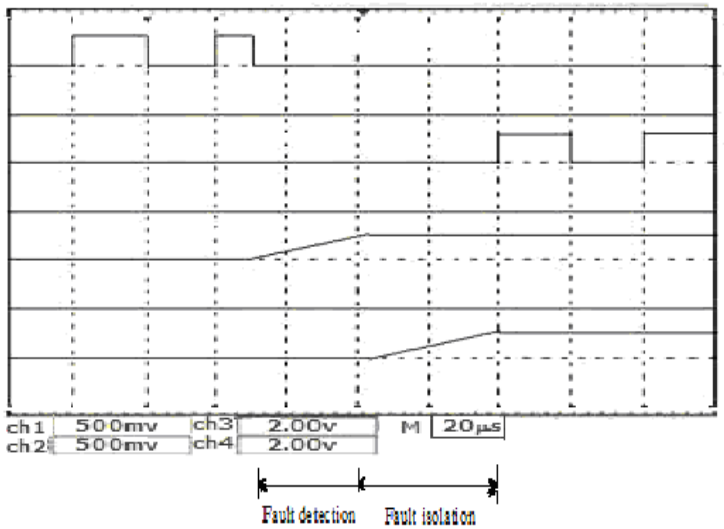

Figure 10. Experimental fault detection and isolation

Figure 10 shows experimental results for 200 µs (10 divisions, 20 µs each) in which switching pulse for faulty leg, triggering pulse for triac switch connected to faulty switch, the fault detecting signal and the fault isolating signal are generated. First channel wave form represents triggering pulse produced by SVPWM to trigger the switch S_1 in which the fault is generated at 75 µs ,Second channel represents gate pulse for Triac at which the fault is isolated by 140 µs . Third signal represents fault detecting a signal for finding the fault detection by 25µs. Fourth signal represents fault isolating signal which isolates the fault by 40 µs. So the total fault tolerant time is 65 µs. Thus both experimental and simulation result is verified.

7. RESULTS AND DISCUSSIONS

FPGA based fault tolerant control on four switch voltage source inverter was investigated in both simulation and experiments through the respective software and hardware. In this scheme, first step was the implementation of fault tolerant topology of FSVSI at the time of fault existence. Next, space vector modulation was proposed to produce the necessary gate signals for the switching devices in the FSVSI. Third step was design of FPGA controller for controlling and minimizing the fault tolerant time between fault occurrence and its isolation. In the discussion of the results, the scheme was successfully conducted and the fault tolerant time was 65 µs.

In the previous research, fault tolerant topology for six switch three phase voltage source inverter was implemented and minimum tolerant time was 25 ms for PI controller based and 15 ms for Fuzzy based schemes. But in this paper, switching fault is isolated or recovered at 65 µs. So this system is the best among the previous methods.

8. CONCLUSION

This paper presents a new scheme of fault tolerant control in four switch voltage source inverter based on space vector pulse width modulation for three phase load. The proposed system uses FPGA controller which isolates the VSI power switch faults and minimizes the time interval between the fault occurrence and its isolation. The characteristics of three phase load are determined at fault conditions. Simulation results show that occurrence of faults can be effectively diagnose with minimum tolerant time. The simulation results and experimental results of the proposed system are compared and verified and it concludes the characteristics, overshoot and tolerant time of this scheme is better than six switch three phase VSI .

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He obtained a bachelor degree (B.E) and master's degree (M.E) from Government college of technology, Coimbatore. He got Ph.D from Annauniversity, Chennai, and Tamilnadu, India. His research area is power electronics and drives, control systems and fault tolerant control.He has 18 years of experience in teaching and 6 years in the research.