Performance evaluation of novel 9-level RSMLI topology for grid-tied solar-PV system

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ABSTRACT

The shortage of traditional fossil fuels like coal, petrol and natural-gas are increased day-by-day, fulfills the most of energy demand. Most of engineers are trying to maximize the energy demand by employing renewable energy with existing micro-grid system. Owing to merits, the solar-PV system plays a significant alternative among all other renewable energy sources due to abundant and virtuous nature. For grid-tied solar-PV system, the cascaded H-bridge multilevel inverter is the most significant over the classical 2-level inverter due to provision of isolated input DC sources. But the cascaded H-bridge topology is designed for limited voltage levels due to its larger number of switches for higher voltage levels, high cost, large-size, and more weight. To alleviate these demerits, a reduced-switch multilevel inverter has been generally preferable for higher voltage levels. In this work, a novel 9-level reduced-switch multilevel inverter (RSMLI) topology has been proposed by utilizing low number of switching devices. The performance of proposed novel 9-level RSMLI topology has been verified in grid-tied solar-PV system by using MATLAB/Simulink tool, simulation results are presented with attractive comparisons.

Keywords: DC-DC boost converter Micro-grid system Reduced-switch multilevel Solar-PV arrays Total harmonic distortions

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1. INTRODUCTION

At present, the solar-PV plants can produce bulk electrical energy which is fed to existing micro-grid for ease of controlling by employing maximum-power point tracking (MPPT) algorithm [1]–[4]. Moreover, it is highly fragile because of various solar-PV cells are connected as series or parallel to generate rated power to drive the requisite demand. The power of solar-PV system is varies during varying temperature and irradiance levels, for extraction of maximum power an incremental-conductance MPPT algorithm has been employed [5]–[7]. The obtained solar-PV energy is directly connected to standalone grid system by using advanced power conversion devices. It consists of DC-DC boost converter and DC-AC inverter modules.

In recent days, the classical 2-level or 3-level square-wave inverter modules are replaced with multilevel inverter (MLI) topologies for medium-voltage and high-power industrial and domestic applications [8]. Among the classical square-wave inverters, the MLI topologies offer favorable merits such as good quality RMS voltage, reduced common-mode voltage, low dv/dt stress, low harmonic profile, low switching stress and increased efficiency, etc. In general, the MLI topology generates staircase output voltage at load terminals from several input DC sources by regulating the switching action of respective switches using feasible switching pulses [9].

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The block diagram of grid-integrated solar-PV system is depicted in Figure 1. To alleviate these demerits, a reduced-switch multilevel inverter (RSMLI) has been generally preferable for higher voltage levels [10]–[15]. According from various literature studies, a single-phase 5-level RSMLI topology is proposed in [16], by using 7 switches for medium-voltage applications without using any transformers. A new single-stage solar-PV integrated 7-level MLI topology is explored in [17], for standalone applications by using 12 switches and without any extra clamping circuits. A single-phase 7-level RSMLI topology is proposed by using 6 switches employing a solar-PV connected multi-output DC-DC converter [18] is depicted in Figure 2.

But this topology is not suitable for higher voltage levels because it requires more high frequency transformers in DC-DC converter which increases the size and cost of overall topology. Bhanutej et al. [19], a novel 9-level RSMLI topology is proposed by using 11 switches for reducing the harmonic profile in a standalone micro-grid system. In fact, these MLI topologies are controlled by using regular sinusoidal pulse-width modulation (PWM) techniques such as phase-shift PWM and level-shift PWM techniques [20]–[25]. But it requires more carrier signals for generation of required voltage levels which increases the complex drive circuitry. Based on above problem statement, the major objective of this work is proposing the novel RSMLI topology for grid-tied solar-PV system with fewer switching devices and it doesn’t requirement of any high frequency transformers. In this work, a novel 9-level RSMLI topology has been proposed by utilizing 7 switches and controlled by novel reduced-carrier PWM technique. The performance of proposed novel 9-level RSMLI topology with RCPWM technique has been verified in grid-tied solar-PV system by using MATLAB/Simulink tool, simulation results are presented with attractive comparisons.

![Figure 1. Block diagram of grid integrated solar-PV system](image1)

![Figure 2. Conventional 7-level RSMLI topology using high-frequency transformer circuit](image2)

2. PROPOSED 9-LEVEL RSMLI TOPOLOGY FOR GRID-TIED SOLAR-PV SYSTEM

Figure 3 shows the block diagram of proposed 9-level RSMLI topology. It consists of various elements such as input DC sources, IGBT switches, and resistive or inductive loads. Generally, it requires \((n-2)\) operating switches named as \(S_{d1}, S_{d2}, S_{d3}, S_{d4}, S_{d5}, S_{d6},\) and \(S_{d7}\), respectively. Also, \((n-1)/2\) input DC sources named \(V_{dc1}, V_{dc2}, V_{dc3}\) and \(V_{dc4}\) as for energizing the proposed 9-level RSMLI topology to attain total 4 \(V_{dc}\) output voltage at load terminals. The synthetization of various output voltage \(V_o\) levels at load terminals
is comprising of 9 voltage levels such as 0V\(_{dc}\), +V\(_{dc}\), +2V\(_{dc}\), +3V\(_{dc}\), +4V\(_{dc}\), and -V\(_{dc}\), -2V\(_{dc}\), -3V\(_{dc}\), -4V\(_{dc}\), respectively. The mathematical relations of proposed 9-level RSMLI topology is illustrated as:

- Required number of switches (\(N_s\)):
  \[ N_s = (n - 2) \]  
  (1)

- Required number of DC sources (N\(_{DC}\)):
  \[ N_{DC} = \frac{(n-1)}{2} \]  
  (2)

- Required number of possible operating modes (Nm)
  \[ N_m = 2 \left( \frac{n-1}{2} \right) + 1 \]  
  (3)

- Required number of voltage levels (VO) at output node
  \[ V_O = (n_{DC} \times 2) + 1 \]  
  (4)

The switching states of proposed 9-level RSMLI topology are illustrated in Table 1. In that, “1” expresses the ON-state of respective switch and “0” expresses the OFF-state of respective switch, accordingly. In fact, the proposed RSMLI topology is controlled by using reduced-carrier PWM technique; it requires low carrier signals for generation of required 9-voltage levels which decreases the complex drive circuitry over the phase-shifted pulse-width modulation (PSPWM) and level-shifted multicarrier modulation (LSPWM) techniques. For generation of 9-voltage levels, the proposed RSMLI technique requires only 1 sinusoidal reference signal \(V_{ref}\) with a frequency of 50 Hz. And also, 4 triangular carrier signals are needed such as \(V_{c1}\), \(V_{c2}\), \(V_{c3}\) and \(V_{c4}\), with the carrier frequency of 3050 Hz which are vertically disposed and slight variations in magnitude of carrier signals. The switching pattern and switching pulses of proposed RCPWM technique is depicted in Figures 4 and 5.

The feasible switching pattern is processed based on possible mathematical expressions which are stated in (5).

\[
\begin{align*}
S_{d1} &= D \cdot E \\
S_{d2} &= (A \cdot \bar{E}) \\
S_{d3} &= (\bar{A} \cdot E) + (D \cdot \bar{E}) \\
S_{d4} &= (\bar{A} \cdot \bar{E}) + E \\
S_{d5} &= (C \cdot E \cdot \bar{D}) + (A \cdot \bar{E} \cdot \bar{B}) \\
S_{d6} &= B \cdot \bar{C} \\
S_{d7} &= (C \cdot \bar{D} \cdot E) + (A \cdot E \cdot \bar{B})
\end{align*}
\]  
(5)
The overall schematic diagram of proposed 9-Level RSMLI topology with RCPWM technique for grid-tied solar-PV system is shown in Figure 6.

Table 1. Switching states of proposed 9-level RSMLI topology

<table>
<thead>
<tr>
<th>Mode</th>
<th>Load voltage ($V_o$)</th>
<th>Switching states</th>
<th>$S_{da1}$</th>
<th>$S_{da2}$</th>
<th>$S_{da3}$</th>
<th>$S_{da4}$</th>
<th>$S_{da5}$</th>
<th>$S_{da6}$</th>
<th>$S_{da7}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level-1</td>
<td>0 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Level-2</td>
<td>$V_{ds}$</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Level-3</td>
<td>2 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Level-4</td>
<td>3 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Level-5</td>
<td>4 $V_{ds}$</td>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Level-6</td>
<td>-$V_{ds}$</td>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Level-7</td>
<td>-2 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Level-8</td>
<td>-3 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Level-9</td>
<td>-4 $V_{ds}$</td>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 4. Switching pattern

Figure 5. Switching states
3. MATLAB/SIMULINK RESULT AND DISCUSSION

3.1. Performance of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique

The performance of proposed novel 9-level RSMLI topology has been verified in R-load, RL-load and grid-tied solar-PV system by using MATLAB-Simulink tool, simulation results are presented with attractive comparisons. The specifications and values of proposed topology is illustrated in Table 2. Figure 7 (see in Appendix) shows the simulation results of proposed Solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage of 115 V during steady-state condition; a slight change in applied illumination implies the starting transient response occurred in solar-PV voltage of 240 V. The solar-PV current of 43 A and a slight change in applied illumination implies the starting transient response occurred in solar-PV power of 10.1 kW and solar-PV power of 5 kW during steady-state condition to drive the R-load system as depicted in Figure 7(a). The obtained solar-PV voltage of 115 V is converted into high step-up voltage DC output voltage of 230 V, with a current of 21 A and output power of 4.8 kW as depicted in Figure 7(b), by using front-end DC-DC boost converter to energize the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage at load terminals with a voltage of 230 V and the load current of 21 A, respectively as depicted in Figures 7(c) and 7(d). The IGBT switches in novel 9-level RSMLI topology are switched-ON/OFF by using proposed RCPWM technique. The total harmonics distortions (THD) spectrum of 9-level output voltage under R-load is measured as 14.09% and the THD spectrum of 9-level output current under R-load is measured as 14.09%, respectively as depicted in Figures 7(e) and 7(f).

Table 2. System specifications and values of proposed topology

<table>
<thead>
<tr>
<th>S. No</th>
<th>Specifications</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Solar-PV voltage</td>
<td>V_{pv}-115 V (peak), I_{pv}-45 A, P_{spv}-5 kW</td>
</tr>
<tr>
<td>2</td>
<td>DC-DC converter</td>
<td>V_{in}-115 V, V_{DC}-230 V, L-21 A, P_{in}-4.8 kW, L_{link}-0.33 mH, C_{link}-148µF</td>
</tr>
<tr>
<td>3</td>
<td>Input DC-link capacitors</td>
<td>V_{in}-230 V, V_{aDC}=1480 µF</td>
</tr>
<tr>
<td>4</td>
<td>Load Impedance</td>
<td>R-load R-11 Ω, RL-Load R-11 Ω, L-0.0169 mH</td>
</tr>
<tr>
<td>5</td>
<td>Switching frequency</td>
<td>f-3050 Hz</td>
</tr>
<tr>
<td>6</td>
<td>Micro-grid system</td>
<td>V_{grid}=230 V, I_{grid}=20 A, P_{grid}=4.6 kW</td>
</tr>
</tbody>
</table>
3.2. Performance of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique

Figure 8 (see in Appendix) shows the simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage of 115 V during steady-state condition; a slight change in applied illumination implies the starting transient response occurred in solar-PV voltage of 240 V. The solar-PV current of 43 A and a slight change in applied illumination implies the starting transient response occurred in solar-PV power of 10.1 kW and solar-PV power of 5 kW during steady-state condition to drive the R-load system as depicted in Figure 8(a). The obtained solar-PV voltage of 115 V is converted into high step-up voltage DC output voltage of 230 V, with a current of 21 A and output power of 4.8 kW as depicted in Figure 8(b), by using front-end DC-DC boost converter to energize the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage at load terminals with a voltage of 230 V and the sinusoidal load current of 21 A, respectively as depicted in Figures 8(c) and 8(d). The IGBT switches in novel 9-level RSMLI topology are switched-ON/OFF by using proposed RCPWM technique. The THD spectrum of 9-level output voltage under RL-load is measured as 14.09% and the THD spectrum of sinusoidal output current under RL-load is measured as 1.33%, respectively as depicted in Figures 8(e) and 8(f). Thus, the THD spectrum of sinusoidal load current is well within IEEE-519/2014 standards.

3.3. Performance of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique

Figure 9 (see in Appendix) shows the simulation results of proposed Solar-PV powered novel 9-level RSMLI topology under grid-connected system using RCPWM technique. The proposed novel 9-level RSMLI topology has been energized by obtained solar-PV voltage which energizes the DC-link capacitors of proposed novel 9-level RSMLI topology. Based on available DC-link voltage, the novel RSMLI topology produces the 9-level staircase voltage (before LCL filter) is depicted in Figure 9(a) and single-phase grid voltage at grid terminals (after LCL filter) is measured with a voltage of 230 V and the sinusoidal single-phase grid current of 22.5 A is depicted in Figures 9(b) and 9(c). The grid current is in-phase with the grid voltage which represents the unity power-factor at grid terminals in depicted in Figure 9(d). The THD spectrum of grid voltage and grid current under grid-connected system is measured as 0.02% and 1.29%, respectively as depicted in Figures 9(e) and 9(f). Thus, the THD spectrum of grid voltage and grid current is well within IEEE-519/2014 standards. The THD comparisons of proposed 9-level RSMLI topology under R-load, RL-load and grid-connected system are illustrated in Table 3. The comparison of number of switching devices required for generation of 9-Level voltage under classical MLI topologies and proposed RSMLI topology is illustrated in Table 4. In that, the proposed novel 9-level RSMLI topology requires very less switching devices and no need of any high frequency transformer which reduces the size, cost and complex control circuitry.

| Table 3. THD comparisons of proposed 9-level RSMLI topology under R-Load, RL-load, and grid-connected system |
|-------------------------------------------------|-----------------|-----------------|
| Proposed 9-Level RSMLI Topology under R-Load   | 14.09%          | 14.09%          |
| Proposed 9-Level RSMLI Topology under RL-Load  | 14.09%          | 1.33%           |
| Proposed 9-Level RSMLI Topology under Grid Connected System | 0.02%          | 1.29%           |

| Table 4. Comparison of number of switching devices required for generation of 9-level voltage under classical MLI topologies and proposed RSMLI topology |
|-------------------------------------------------|-----------------|-----------------|-----------------|
| Topologies switching devices                  | Classical 9-Level MLI Topologies | Conventional 9-Level RSMLI Topology | Proposed 9-Level RSMLI Topology |
|                                                | DCMLI Topology  | FCMLI Topology  | CHBMLI Topology |                         |
| Main IGBT Switches                            | 16              | 16              | 16              | 10                        |
| Input DC Sources                              | 8               | 8               | 8               | 4                         |
| Clamping Diodes                               | 56              | 0               | 0               | 0                         |
| Balancing Capacitors                          | 0               | 28              | 0               | 0                         |
| Body Diodes                                   | 16              | 16              | 16              | 7                         |
| High Frequency Transformers                   | 0               | 0               | 0               | 0                         |

4. CONCLUSION

The design and operation of proposed novel 9-level RSMLI topology has been evaluated and highly recognized for standalone R-load, RL-load and grid-connected system under the same voltage-power
specifications. Over the classical 9-level MLI topologies, the key merits of proposed RSMLI topology have fewer switches, compact size, good quality RMS voltage, low harmonic content, reduced common-mode voltage, low dv/dt stress, low switch losses, and increased efficiency. And also, the proposed RCPWM technique requires only carriers for generation of required switching pulses to novel RSMLI topology among the PSPWM and LSPWM techniques, which reduces the computational delay and complex gate-pulse generation unit, etc. Therefore, the proposed novel RSMLI topology requires very less switching devices and no need of any high frequency transformers which reduces the size, cost and complex control circuitry.

APPENDIX

Figure 7. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique: (a) solar-PV input voltage, current, and power and (b) output DC-link voltage, current and power
Figure 7. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under R-load using RCPWM technique: (c) 9-level output voltage, (d) 9-level output current, (e) THD spectrum of 9-level output voltage, and (f) THD spectrum of 9-level output current (continued)
Figure 8. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique: (a) solar-PV input voltage, current, and power, (b) output DC-link voltage, current, and power, and (c) 9-level output voltage
Figure 8. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under RL-load using RCPWM technique: (d) sinusoidal output current, (e) THD spectrum of 9-level output voltage, and (f) THD spectrum of sinusoidal output current (continued).

Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (a) 9-level output voltage.
Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (b) single-phase grid voltage, (c) grid current, and (d) grid voltage and current (in-phase) (continued)
Figure 9. Simulation results of proposed solar-PV powered novel 9-level RSMLI topology under grid connected system using RCPWM technique: (e) THD spectrum of grid voltage and (f) THD spectrum of grid current (continued)

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